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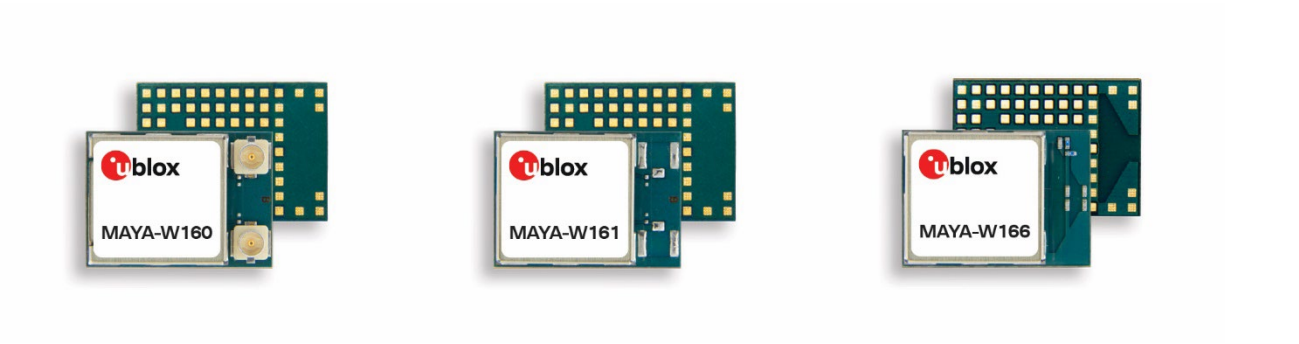
MAYA-W1 series

Host-based multiradio modules with Wi-Fi 4 and Bluetooth®

Data sheet



Abstract

This technical data sheet describes MAYA-W1 series short range modules with dual-band Wi-Fi 4 and Bluetooth. Designed for a wide range of industrial applications, this range of ultra-compact, cost-efficient, host-based multiradio modules includes product variants that are supplied with or without internal antenna. Integrated with a MAC/Baseband processor and RF front end components, MAYA-W1 modules connect to a host processor through SDIO and High-Speed UART interfaces.

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This document applies to the following products:

Product name	**Type number**	**Product status**
MAYA-W160	MAYA-W160-00B-00	Mass production
MAYA-W161	MAYA-W161-00B-00	Mass production
MAYA-W161	MAYA-W161-00C-00	In development
MAYA-W166	MAYA-W166-00B-00	Mass production
MAYA-W166	MAYA-W166-01B-00	Mass production

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1 Functional description

1.1 Overview

The MAYA-W1 series comprises ultra-compact, multiradio modules with Wi-Fi 4 and Bluetooth®, including variants with or without an internal antenna. MAYA-W1 series supports IEEE 802.11a/b/g/n Wi-Fi standards delivering up to 150 Mbps data throughput. With dual-band, 2.4 / 5 GHz and 40 MHz channel width, the modules can work as a station with different types of AP, as a simple access-point, in P2P communication, or as a combination of these. MAYA-W1 supports both Bluetooth classic (BR/EDR) and Bluetooth LE, including long-range PHY. MAYA-W166-00B modules include an internal antenna with an optional sharp SAW filter. The module comes with RF calibration and MAC address available in the on-board OTP memory.

The modules are developed for reliable, high-demanding, industrial devices and applications that demand high performance. MAYA-W1 modules are qualified against Bluetooth Core 5.2.

Radio type approvals for Europe (RED), Great Britain (UKCA), United States (FCC), Canada (ISED), Japan (MIC), and South Korea (KCC) are completed.

1.2 Product features

Radio features	Description
Wi-Fi Standards	Wi-Fi 4 IEEE 802.11a/b/g/n
Wi-Fi frequency bands	2.4 GHz, channel 1-13 5 GHz, channel 36-165
Bluetooth	Bluetooth 5.2 specification support Bluetooth LE and Bluetooth BR/EDR
Antennas	MAYA-W160: 2 U. FL connectors
	MAYA-W161: 2 antenna pins
	MAYA-W166-00B: 1 embedded PCB antenna
	MAYA-W166-01B: 1 antenna pin
Software features	
Security	WPA3, WPA2, WPA2 and WPA mixed mode
RF calibration and MAC addresses	Available in on-board OTP memory
Wi-Fi operational modes	Station, Access-Point, Wi-Fi direct, or combination of these
Driver support	Free drivers for Linux and Android RTOS (with certain types of NXP MCUs)
Interfaces	
Wi-Fi	SDIO 3.0 (4-bit, up to 100 MHz clock)
Bluetooth	4-wire high-speed UART, HCI transport layer PCM/I2S for audio
Other	GPIOs
Package	
Dimensions	10.4 x 14.3 x 1.8 mm
Mounting	Soldering, 86 pins (LGA)
Environmental data, quality & reliability	
Operating temperature	Professional grade: -40 °C to +85 °C Standard grade: 0°C to +70°C
MSL-level	4
RoHS and REACH compliance	Yes
Electrical data	
RF power supply	3.0–3.6 VDC, 1.8 VDC
I / O power supply	3.3 VDC or 1.8 VDC
Certifications and approvals	
Type approvals	Completed: Europe (RED), Great Britain (UKCA), US (FCC), Canada (ISED), South Korea (KCC), Japan (MIC) Other country certification: On request
Bluetooth qualification	v5.2 (Bluetooth BR/EDR and Bluetooth LE)
Support Products	
EVK-MAYA-W161	Evaluation kit for MAYA-W160 or MAYA-W161
EVK-MAYA-W166	Evaluation kit for MAYA-W166-00B
Product variants	
	See Ordering information

Table 1: MAYA-W1 series product features

1.3 Block diagram

Four versions of MAYA-W1 are available: MAYA-W161 with two antenna RF pins, MAYA-W160 with two U.FL connectors, MAYA-W166-00B with a single internal antenna, and MAYA-W166-01B with a single antenna pin.

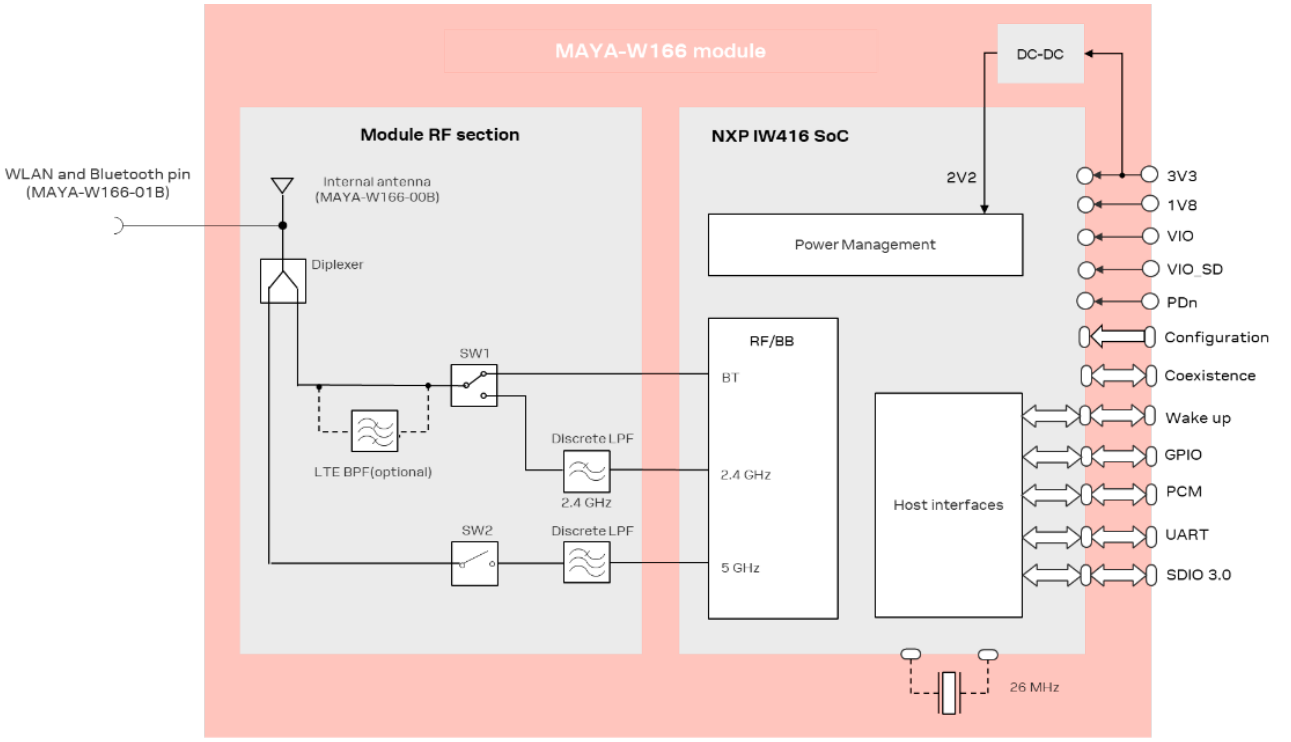


Figure 1: Block diagram of MAYA-166

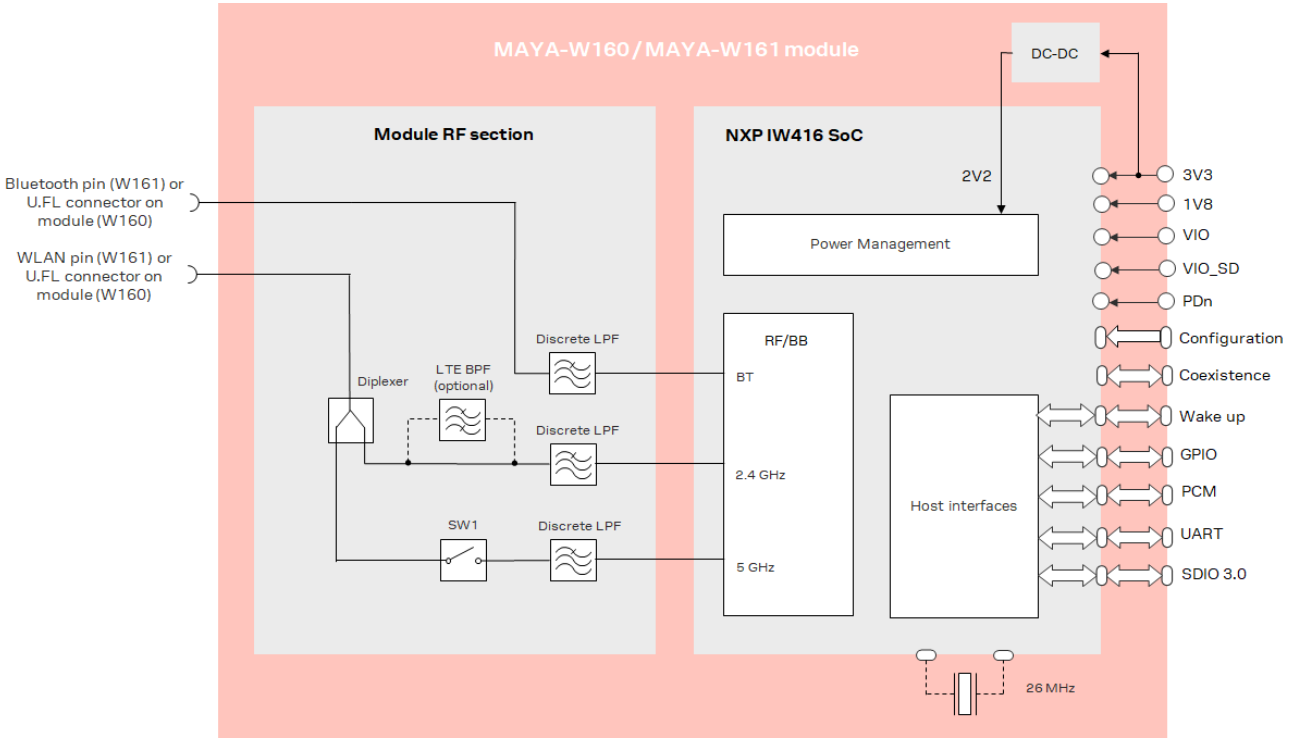


Figure 2: Block diagram of MAYA-161 or MAYA-160

1.4 Product description

MAYA-W1 series comprises ultra-compact Wi-Fi front-end modules with an SDIO host interface and module outline of only 14.3 x 10.4 mm. The module supports Wi-Fi IEEE 802.11a/b/g/n and Bluetooth 5.2 and is developed for reliable, high-demanding, industrial devices and applications. Based on the NXP IW416 chipset, MAYA-W1 includes an integrated MAC/Baseband processor and RF front-end components.

The MAYA-W1 series offers three different antenna solutions:

- MAYA-W160 has two U.FL connectors for connecting external antennas and supports switching antenna diversity for Wi-Fi using a control signal for an external antenna switch. It includes an integrated discrete filter in the 2.4 GHz band (optional LTE filter for improved coexistence with LTE bands 7, 38, 40 and 41) and 5 GHz band.
- MAYA-W161 has two antenna pins for connecting external antennas and supports switching antenna diversity for Wi-Fi using a control signal for an external antenna switch. It also includes a discrete filter in the 2.4 GHz band (with optional LTE filter for improved coexistence with LTE bands 7, 38, 40 and 41) and 5 GHz band. This module is available in Professional and Standard grades.
- MAYA-W166-00B includes an internal niche antenna and integrated discrete filter in the 2.4 GHz band (with optional LTE filter for improved coexistence with LTE bands 7, 38, 40 and 41) and 5 GHz band. The internal antenna uses antenna technology licensed from Abracon.
- MAYA-W166-01B has a single antenna pin for connecting an external antenna and supports switching antenna diversity for Wi-Fi using a control signal for an external antenna switch. It also includes an integrated discrete filter in the 2.4 GHz band (optional LTE filter for improved coexistence with LTE bands 7, 38, 40 and 41) and 5 GHz band.

1.5 Supported features

- Integrated highly effective antenna, antenna pin, or U. FL connectors
- Extended operating temperature range of -40 °C to +85 °C for professional grade module, and 0 °C to +70 °C for standard grade module
- Selectable 1.8 V or 3.3 V IO levels
- Simultaneous Wi-Fi and Bluetooth operation with dual antenna configuration
- Shared 2.4 GHz Wi-Fi and Bluetooth operation with single antenna or antenna pin (MAYA-W166)
- Wi-Fi/Bluetooth coexistence support

1.5.1 Wi-Fi features

- Supports Wi-Fi 4, IEEE 802.11 a/b/g/n
- Dual-band 2.4 GHz and 5 GHz
- Single stream 802.11n with 20 and 40 MHz channel width
- Data rate up to 150 Mbps (MCS7)
- 802.11n short and long guard interval
- Dynamic frequency selection (radar detection)
- Power saving features
- SDIO 3.0 device interface
- Security: WPA3, WPA2, WPA2 and WPA mixed mode
- Wi-Fi Standards IEEE 802.11d/e/h/i/k/r/u/v/w
- Supports simultaneous station, access point and P2P modes
- Supports up to eight stations in AP mode

1.5.2 Bluetooth features

- Dual-mode Bluetooth LE and Bluetooth BR/EDR
- Bluetooth 5.2 specification support
- Bluetooth Class 1 and Class 2 operation
- High-speed UART host interface with standard HCI transport layer
- Bluetooth LE 2 Mbit/s PHY
- Bluetooth LE Long-Range PHY
- I2S and PCM interface for voice applications
- Encryption (AES) support
- Bluetooth LE Broadcaster, Observer, Central, and Peripheral roles
- Bluetooth LE link layer topology (connects to 16 links)
- Bluetooth LE Privacy 1.2
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length and Advertising Extension

1.6 Reserved MAC addresses

MAYA-W1 series modules have four consecutive MAC addresses that are unique for each module variant. The first two of these four addresses are configured during production.

The first address is used for the Bluetooth communication, while the second address is configured for Wi-Fi communication. The Data Matrix Code shown on the product label includes the Bluetooth MAC address. See also Product labeling. The remaining two MAC addresses are not used in the manufacturing configuration but are reserved for module usage.

MAC address	Assignment	Last two bits of MAC address	Example
Module1, address 1	Bluetooth	00	*D4:CA:6E:44:00:04*
Module1, address 2	Wi-Fi	01	D4:CA:6E:44:00:05
Module1, address 3	(free for use)	10	D4:CA:6E:44:00:06
Module1, address 4	(free for use)	11	D4:CA:6E:44:00:07
Module2, address 1	Bluetooth	00	*D4:CA:6E:44:00:08*
Module2, address 2	Wi-Fi	01	D4:CA:6E:44:00:09
Module2, address 3	(free for use)	10	D4:CA:6E:44:00:0A
Module2, address 4	(free for use)	11	D4:CA:6E:44:00:0B

Table 2: MAC address assignment

2 Interfaces

2.1 Interface configuration

The hardware state at power-on can differ depending on the pin multiplexing and strap settings. The state of the hardware is determined by the pin state at power-on after the boot code finishes and before the firmware download begins.

To set a configuration bit to 0, attach a 50–100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

MAYA-W1 supports two configuration pins, CONFIG[0] and CONFIG[1], for selecting the host interface configuration, as shown in Table 3. Additional configuration pins are supported to set configuration parameters following a hardware reset, as described in Table 4. Configuration pins revert to normal function after boot-up.

CONFIG[1]	CONFIG[0]	Wi-Fi host i/f	Bluetooth host i/f
1	0	SDIO	UART
Others		Reserved	Reserved

Table 3: Firmware boot options

Configuration bits	Pin name	Configuration function
CON[9]	GPIO[1]	Reserved Set to 111
CON[8]	UART_RTSn/GPIO[11]	
CON[7]	UART_CTSn/GPIO[8]	
CON[5]	RF_CNTL3_P	Reserved. Set to 1
CON[1]	CONFIG[1]/RF_CNTL2_N	Firmware boot options
CON[0]	CONFIG[0]/RF_CNTL0_N	No hardware impact Software reads and boots accordingly. See also Table 3.

Table 4: Configuration pins

2.2 Host interfaces

MAYA-W1 has two high-speed host interfaces:

- SDIO 3.0 device interface for Wi-Fi
- UART interface for Bluetooth

The host interfaces for Wi-Fi and Bluetooth are selected using the configuration pins described in Table 3.

2.2.1 SDIO interface

MAYA-W1 supports an SDIO device interface that conforms to the industry standard SDIO 3.0 specification, including default speed (25 MHz), high-speed (50 MHz), SDR12/25/50 (12/25/50 MB/s), and DDR50 (50 MB/s) modes. The interface supports 1-bit SDIO and 4-bit SDIO transfer modes at full clock range up to 100 MHz for SDR50. All mandatory SDIO commands are supported.

In 4-bit SDIO mode, data is transferred on all four data pins (**SD_DAT**[3:0]). The interrupt pin is not available for exclusive use as it is utilized as a data transfer line. If the interrupt function is required, special timing is required to provide interrupts. The 4-bit SDIO mode provides the highest data transfer possible with speeds up to 50 MB/s in SDR50 mode.

The pull-up resistors required for the SD interface on **SD_CMD**, **SD_DAT** [3:0] must be provided by the host. In accordance with SDIO v2.0 specifications, the value of resistors should be between 10–100 kΩ.

33 Ω in-line resistors can be required to help with signal integrity. The SDIO signals levels are selectable according to the **VIO_SD** 1.8/3.3 voltage levels. See also Power supply interfaces.

Table 5 describes the required pins for the SDIO interface.

Pin name	I/O type	1-bit mode	4-bit mode
SD_DAT[0]	I/O	DATA: Data line	Data line 0
SD_DAT[1]	I/O	IRQ: Interrupt	Data line 1
SD_DAT[2]	I/O	RW: Read Wait	Data line 2
SD_DAT[3]	I/O	N/C: Not used	Data line 3
SD_CMD	I/O	Command line	Command line
SD_CLK	I	Clock input	Clock input

Table 5: SDIO interface pin description

2.2.2 Default speeds, high speed modes

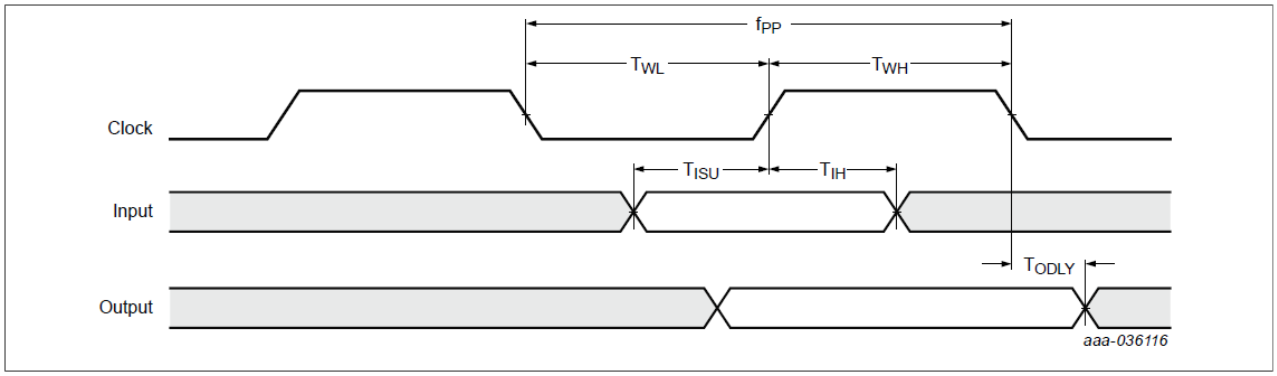


Figure 3: SDIO protocol timing diagram - default speed mode

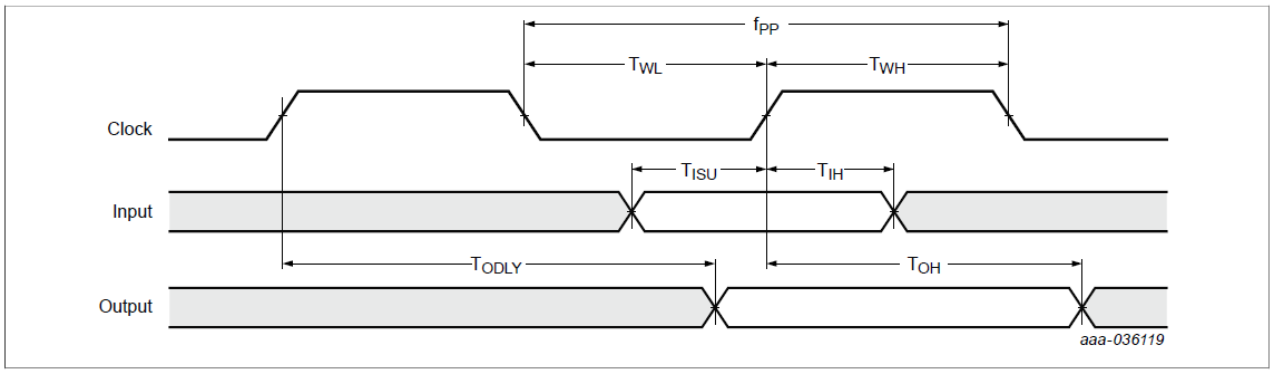


Figure 4: SDIO protocol timing diagram – high speed mode

Table 6 describes the SDIO timing data for the default and high-speed modes with SDIO clock running at 25 MHz or 50 MHz. The **VIO_SD** power pin must be supplied at 3.3 V.

Symbol	Parameter	Condition	MIn	Typ	Max	Unit
f_{pp}	Clock frequency	Default speed	0	-	25	MHz
		High speed	0	-	50	MHz
T_{WL}	Clock low time	Default speed	10	-	-	ns
		High speed	7	-	-	ns
T_{WH}	Clock high time	Default speed	10	-	-	ns
		High speed	7	-	-	ns
T_{ISU}	Input setup time	Default speed	5	-	-	ns
		High speed	6	-	-	ns
T_{IH}	Input hold time	Default speed	5	-	-	ns
		High speed	2	-	-	ns
T_{ODLY}	Output Delay Time	Default speed	-	-	14	ns
		High speed	-	-	14	ns
T_{OH}	CL≤40 pF (1 card)	Default speed	2.5	-	-	ns
		High speed	-	-	-	ns

Table 6: SDIO timing data – default and high-speed modes

2.2.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Table 7 describes the SDIO timing data for the SDR12/25/50 modes with SDIO clock running at up to 100 MHz. The **VIO_SD** power pin must be supplied at 1.8 V.

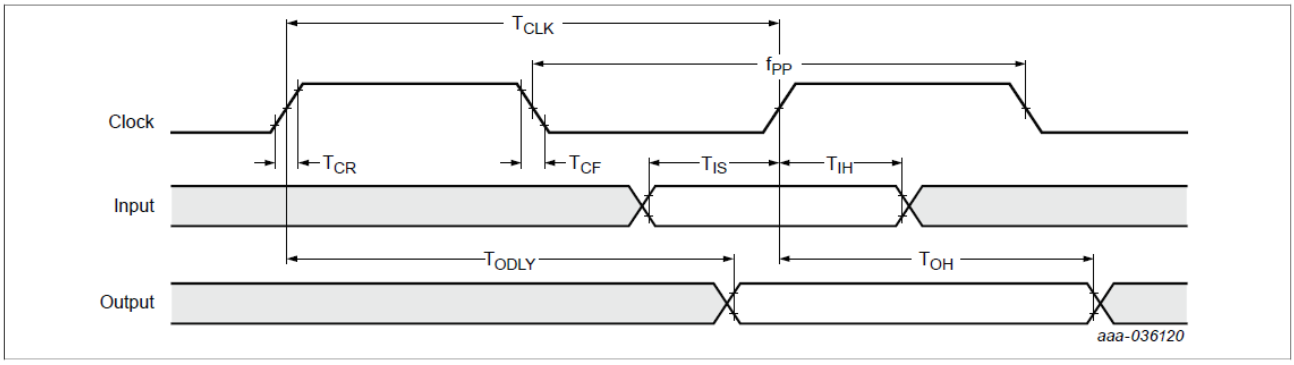


Figure 5: SDIO protocol timing diagram – SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{pp}	Clock frequency	SDR 12/25/50	25	–	100	MHz
T_{IS}	Input setup time	SDR 12/25/50	3	–	–	ns
T_{IH}	Input hold time	SDR 12/25/50	0.8	–	–	ns
T_{CLK}	Clock time	SDR 12/25/50	10	–	40	ns
T_{CR} ,T_{CF}	Rise time, fall time T_{CR} ,T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR 12/25/50	–	–	0.2*T_{CLK}	ns
T_{OLDY}	Output delay time $C_L \leq 30$ pF	SDR 12/25/50	–	–	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR 12/25/50	1.5	–	–	ns

Table 7: SDIO timing data – SDR12, SDR25, SRD50 modes (up to 100 MHz) (1.8V)

2.2.4 DDR50 mode (50 MHz) (1.8V)

Table 8 describes the SDIO timing data for the DDR50 mode with SDIO clock running at 50 MHz. The **VIO_SD** power pin must be supplied at 1.8 V.

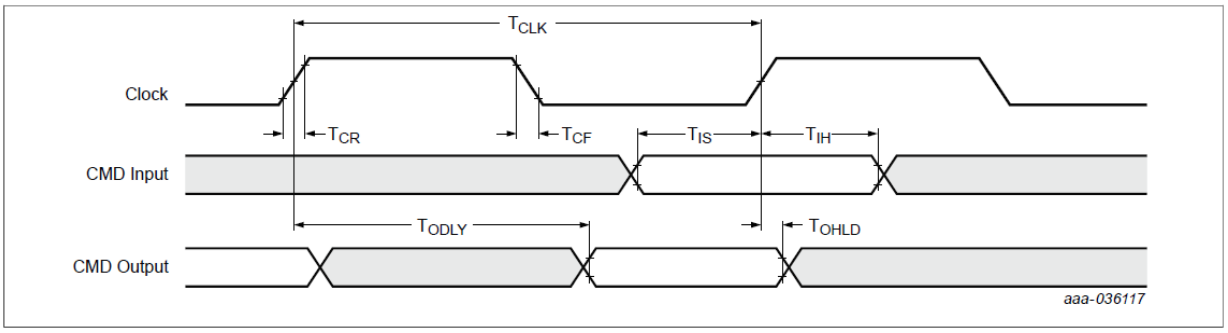


Figure 6: SDIO CMD timing diagram – DDR50 mode (50 MHz)

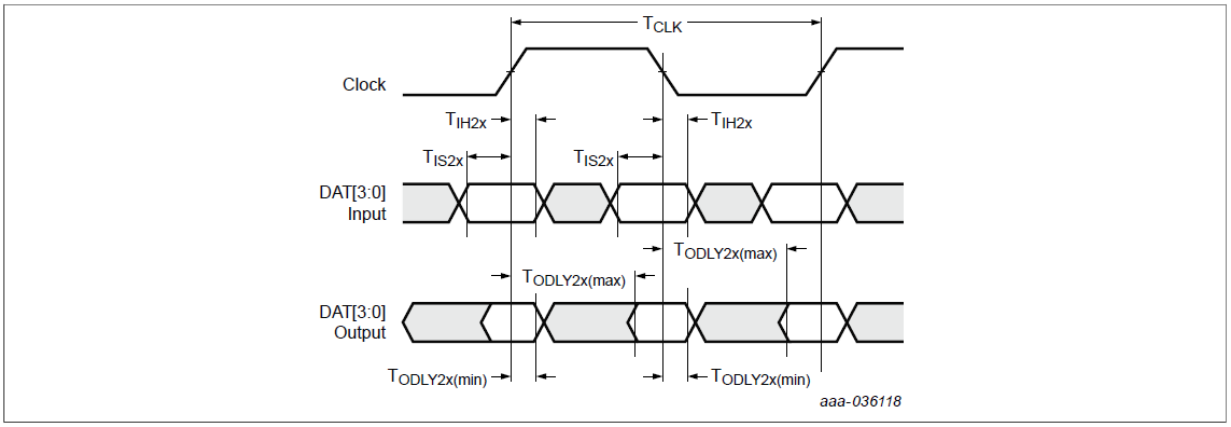


Figure 7: SDIO DAT[3:0] timing diagram – DDR50 mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR 50	20	–	–	ns
T_{CR} ,T_{CF}	Rise time, fall time T_{CR} ,T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR 50	–	–	0.2*T_{CLK}	ns
Clock duty	–	DDR 50	45	–	55	%
CMD input (with reference to rising clock edge)						
T_{IS}	Input setup time C_{CARD} = 10 pF (1 card)	DDR 50	6	–	–	ns
T_{IH}	Input hold time C_{CARD} = 10 pF (1 card)	DDR 50	0.8	–	–	ns
CMD output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode $C_L \leq$ 30 pF (1 card)	DDR 50	–	–	13.7	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{OHLD}	Output hold $C_L \geq 15$ pF (1 card)	DDR 50	1.5	–	–	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time $C_{CARD} \leq 10$ pF (1 card)	DDR 50	3	–	–	ns
T_{IH2x}	Input hold time $C_{CARD} \leq 10$ pF (1 card)	DDR 50	0.8	–	–	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode $C_L \leq 25$ pF (1 card)	DDR 50	–	–	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time $C_L \geq 15$ pF (1 card)	DDR 50	1.5	–	–	ns

Table 8: SDIO timing data – DDR50 mode (50MHz)

2.2.5 SDIO internal pull-up and pull-down specifications

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance		60	90	120	kΩ

Table 9: SDIO internal pull-up and pull-down specifications

2.3 Antenna interfaces

The MAYA-W1 series supports either an internal antenna (MAYA-166-00B) or external antennas connected through an antenna pin or U. FL connectors (MAYA-W161, MAYA-160 or MAYA-W166-01B).

To prevent mutual interference with LTE bands, MAYA-W1 includes an optionally integrated, high-performance 2.4 GHz SAW LTE band pass filter.

2.3.1 Internal antenna

MAYA-W166-00B has an internal niche (embedded) 2.4 / 5 GHz antenna that is specifically designed and optimized for the MAYA form factor.

⚠ The **RF_ANT0** and **RF_ANT1** signals are not available on the solder pins of MAYA-W166-00B module, and no antenna diversity functionality is available for this variant.

2.3.2 External RF antenna interface

MAYA-W160, MAYA-W161 and MAYA-W166-01B are equipped with either single/dual RF (ANT) pins or U.FL connectors that have a 50 Ω characteristic impedance for use with an external antenna. The antenna signal supports both Tx and Rx.

The external antenna can be an SMD antenna (or PCB integrated antenna) mounted on the host board. An antenna connector for use with an external antenna through a coaxial cable can also be considered. The use of a cable antenna can be necessary if the module is mounted in a shielded enclosure, such as a metal box or cabinet.

MAYA-W1 is tested and approved for use with single- and dual-band antennas. For the list of antennas that are pre-approved for use with MAYA-W1, see the system integration manual [2].

MAYA-W160, MAYA-W161, and MAYA-W166-01B also support a switching antenna diversity solution with an external antenna switch. The switch is controlled by the **RF_CNTL3_P** signal from the MAYA-W1 module. For more information about antenna switch design, see also the MAYA-W1 series system integration manual [2].

2.4 Power supply interfaces

The DC power for MAYA-W1 series modules is supplied through **3V3**, **1V8**, **VIO** and **VIO_SD** pins.

The separate **VIO** pin enables integration of MAYA-W1 in either 1.8 V or 3.3 V applications – without the need for level converters.

VIO_SD is used for digital 1.8 V/3.3 V SDIO power supply.

2.5 Power mode interfaces

MAYA-W1 series modules support external power management control through the Power Down signal, **PDn**.

2.5.1 Power down

For applications that do not use Wi-Fi and Bluetooth, the device can be put into a low-leakage mode of operation using one of the following methods:

- **PDn** pin: The power-down state provides the lowest leakage mode of operation. Assert **PDn** low to enter power-down. This condition must be met to enter a power-down state.
- All rails powered off: Alternatively, **3V3**, **1V8**, **VIO** and **VIO_SD** can be powered off. In this case, the state of the **PDn** pin becomes irrelevant.

During power-up the **PDn** should follow the **1V8** power rail.

2.5.2 Sleep

A deep sleep mode in MAYA-W1 is used to reduce power consumption. **WLAN_DEV_WAKE** and **BT_DEV_WAKE** are optional out-of-band wake-up pins to wake up the transceiver from sleep mode.

2.6 Power up sequence timing

The module power-up sequence can be initiated by applying the respective voltage to the **3V3/1V8/VIO/VIO_SD** supply pins and deasserting **PDn** (logic level 1). Firmware download is required every time **PDn** signal is asserted.

Figure 8 shows the recommended power-up sequences of a MAYA-W1 series module. During the power up of MAYA-W1 series modules, **VIO/VIO_SD** should be applied at the same time or after **3V3**. Once the internal Switched Mode Power Supply (SMPS) has stabilized to 90%, this takes up to 0.55 ms, **1V8** can be applied followed by deasserting **PDn**.

PDn is ideally held low during start up and released when the power is stable, or later when the module must be turned on. **PDn** is powered by the **1V8** voltage domain and is connected through a 10 kΩ pull up resistor to **1V8**.

Optionally, the **PDn** pad can be left unconnected so that it follows **1V8** through the pull up resistor. In which case, the power down mode is not accessible and a further full-power cycle must be made to reset the module.

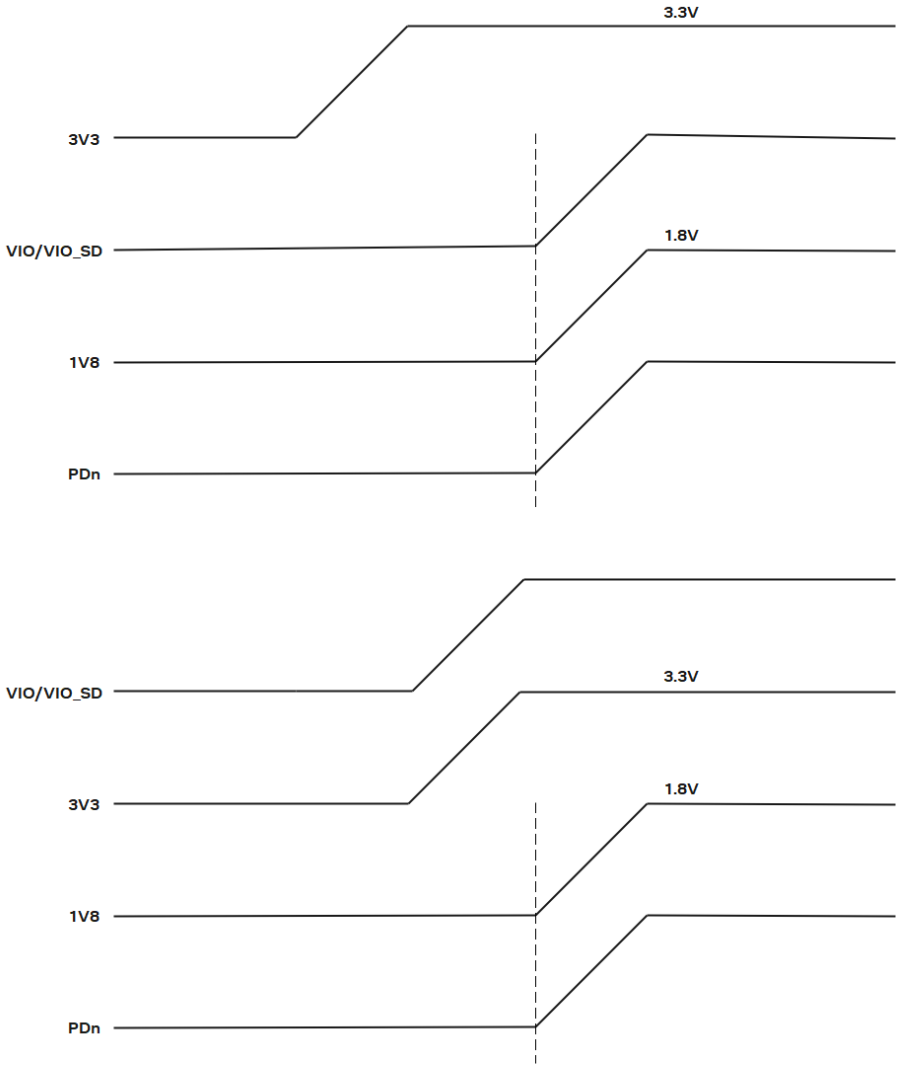


Figure 8: Different power-up sequences for MAYA-W1 module

☞ Power down mode is entered through **PDn** assertion by the host. **PDn** must be asserted for a minimum of 100 ms for correct reset.

2.7 GPIOs

MAYA-W1 supports 15 GPIO pins. On power-up and reset, the GPIO pins assume a high-impedance tristate. The UART, PCM and JTAG interfaces can be assigned to the GPIO pins. After initialization firmware is downloaded and the pads are programmed in line with the functionality of the GPIOs. See also Pin assignment.

For information describing what GPIOs are used for the interfaces, see also UART, PCM/I2S audio interfaces, External coexistence interface and JTAG. All other used GPIOs are described in the Pin definition.

2.8 UART

The chipset supports a high-speed host interface for Bluetooth operation. The baud rate is adjustable from 1200 bps to 3.0 Mbps. The acceptable deviation from the UART Rx target baud rate is ±3%. The UART supports RX/TX pins and modem control functions **CTS**, **RTS**, **DSR** and **DTR**. Table 10 describes the chipset pins for the UART interface.

Pin name	I/O type	Description	GPIO pin multiplexing
UART_CTSn	I	Active low clear-to-send input signal	GPIO[8]
UART_SIN	I	Serial input signal	GPIO[9]
UART_SOUT	O	Serial output signal	GPIO[10]
UART_RTSn	O	Active-low request-to-send signal	GPIO[11]
UART_DSRn	I	Active-low data-set-ready signal	GPIO[12]
UART_DTRn	O	Active-low data-terminal-ready signal	GPIO[13]

Table 10: Bluetooth UART interface description

☞ Although the MAYA-W1 pinout supports only a 4-wire UART interface, **DSR** and **DTR** functionality can be accessed through the GPIO[12] and GPIO[13] pins if required.

2.9 PCM/I2S audio interfaces

The chipset supports PCM and I2C interfaces on the same pins. The interfaces connect to linear codec devices in master or slave mode.

- PCM pins shared with I2S pins
- PCM master or slave mode
- PCM bit-width size of 8 bits or 16 bits
- Up to 4 PCM slots with configurable bit width and start positions
- PCM short-frame and long-frame synchronization
- I2S master and slave modes for I2S, MSB, and LSB audio interfaces
- Tri-state capability

Table 11 describes the chipset pins that connect directly to the PCM pins of MAYA-W1. With **GPIO[4]** configured as **PCM_DIN** or **I2S_DIN**, **GPIO[5]** becomes **PCM_DOUT** or **I2S_DOUT** and vice versa.

Pin name	I/O Type	Description	GPIO pin muxing
PCM_DOUT/ I2S_DOUT	O	PCM/I2S data out	GPIO[4]/GPIO[5]
PCM_DIN / I2S_DIN	I	PCM/I2S data in	GPIO[4]/GPIO[5]
PCM_CLK / I2S_BLCK	I/O	PCM/I2S clock, can be output (if master) or input (if master)	GPIO[6]
PCM_SYNC / I2S_LRCLK	I/O	PCM/I2S sync, can be output (if master) or input (if master)	GPIO[7]
PCM_MCLK / I2S_CCLK	O	Optional clock pins	GPIO[3]

Table 11: Bluetooth PCM/I2S interface description

2.9.1 Master mode

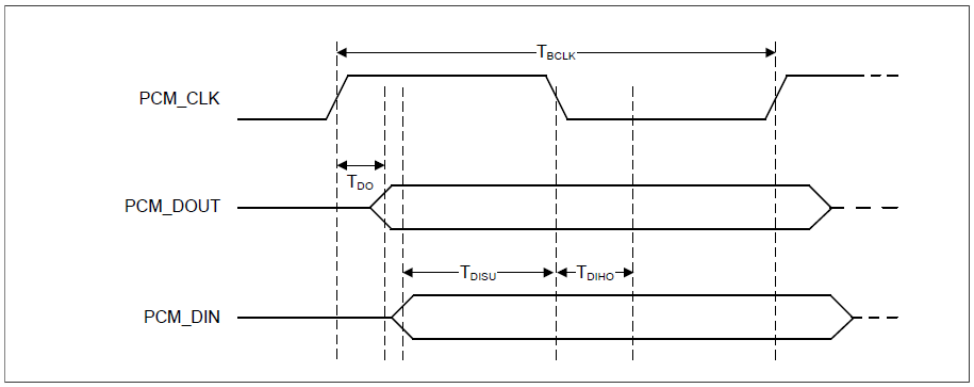


Figure 9: PCM timing specification diagram for data signals – Master mode

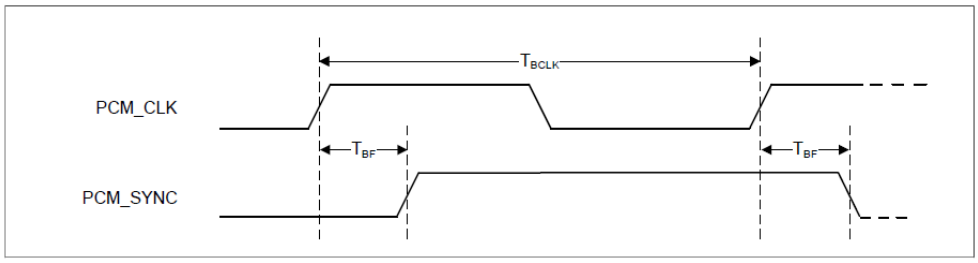


Figure 10: PCM timing specification diagram for PCM_SYNC signal – Master mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	–	–	2/2.048	–	MHz
Duty Cycle $_{BCLK}$	Bit clock duty cycle	–	0.4	0.5	0.6	–
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	–	–	3	–	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	–	–	–	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	–	20	–	–	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	–	15	–	–	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	–	–	–	15	ns

Table 12: PCM timing specification data – Master mode

2.9.2 Slave mode

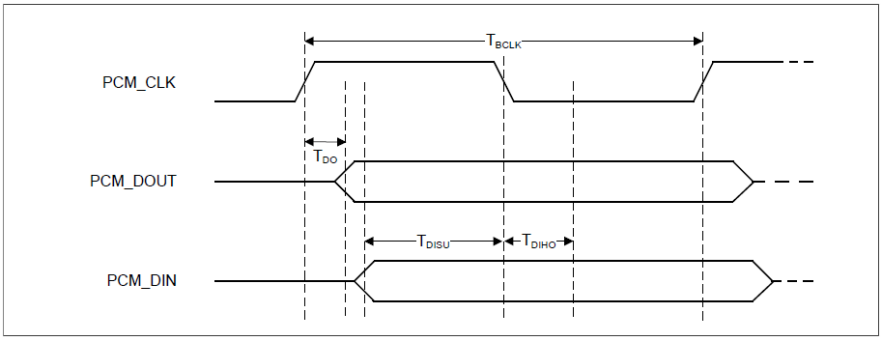


Figure 11: PCM timing specification diagram for data signals – slave mode

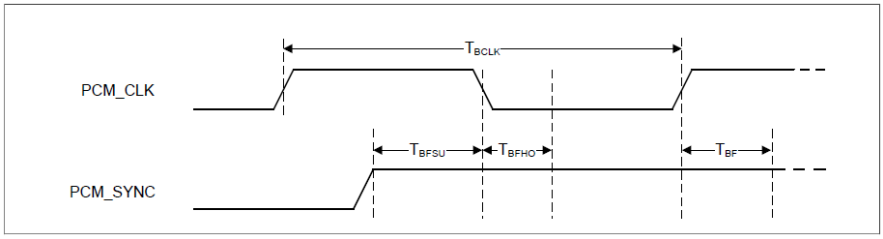


Figure 12: PCM timing specification diagram for PCM_SYNC signal – slave mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	–	–	2/2.048	–	MHz
Duty Cycle $_{BCLK}$	Bit clock duty cycle	–	0.4	0.5	0.6	–
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	–	–	3	–	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	–	–	–	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	–	15	–	–	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	–	10	–	–	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	–	15	–	–	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	–	10	–	–	ns

Table 13: PCM timing specification data – slave mode

2.10 External coexistence interface

External coexistence interfaces enable signaling between the internal radios and external co-located wireless devices for optimal performance when sharing the wireless medium. External radios can be connected to the 5-wire packet traffic arbitration interface (PTA) or the 2-wire wireless coexistence interface 2 (WCI-2). WCI-2 message format and message type comply with Bluetooth special interest group (SIG) core specification volume 7, part C.

Pin name	I/O type	Description	GPIO pin muxing
EXT_STATE	I	External radio state input signal	GPIO[1]
EXT_GNT	O	External radio grant output signal	GPIO[5]
EXT_FREQ	I	External radio frequency input signal	GPIO[4]
EXT_PRI	I	External radio input priority signal	GPIO[6]
EXT_REQ	I	Request from the internal radio	GPIO[7]
WCI_SIN	I	WCI-2 serial interface input	-
WCI_SOUT	O	WCI-2 serial interface output	-

Table 14: External coexistence interface description

2.11 JTAG

The chipset includes a JTAG test interface that is supported using the GPIO pins.

Pin name	I/O type	Description	GPIO pin multiplexing
JTAG_TCK	I	JTAG test clock	GPIO[14]
JTAG_TMS	I	JTAG controller select	GPIO[15]
JTAG_TDI	I	JTAG test data input	GPIO[2]
JTAG_TDO	O	JTAG test data output	GPIO[3]

Table 15: JTAG interface description

3 Pin definition

3.1 Pin assignment

Figure 13: MAYA-W1 series pin assignment (top view)

☞ All signal pins are mounted in a land grid array (LGA) package on the bottom side of the PCB. The **RF_ANT0** and **RF_ANT1** pins are only available on MAYA-W161 and MAYA-W166-01B.

No.	Name	I/O	Description	Alt. functions	Power Down	Power supply domain
A1	GND	-	Ground		-	
A2	1V8	-	1.8 V supply		-	1V8
A3	SD_DAT[1]	I/O	SDIO data 1		Tristate	VIO_SD
A4	SD_CLK	I	SDIO clock		Tristate	VIO_SD
A5	SD_DAT[3]	I/O	SDIO data 3		Tristate	VIO_SD

No.	Name	I/O	Description	Alt. functions	Power Down	Power supply domain
A6	VIO_SD	-	1.8 V / 3.3 V SDIO supply		Tristate	VIO_SD
A7	3V3	-	3.3 V supply		-	3V3
A8	VIO	-	1.8 V / 3.3 V I/O supply		-	VIO
A9	GND	-	Ground		-	
B1	SLP_CLK_IN	I	Sleep clock input (optional)		Tristate	1V8
B2	GND	-	Ground		-	
B3	SD_DAT[0]	I/O	SDIO data 0		Tristate	VIO_SD
B4	SD_CMD	I/O	SDIO command		Tristate	VIO_SD
B5	SD_DAT[2]	I/O	SDIO data 2		Tristate	VIO_SD
B6	WCI_SOUT	O	Coexistence serial interface		Tristate	1V8
B7	3V3	-	3.3 V supply		-	3V3
B8	GND	-	Ground		-	
B9	NC	-	Reserved for VUSB		-	
C1	NC	-	Reserved for PCIe		-	
C2	NC	-	Not Connected		-	
C4	NC	-	Reserved for I2C		-	
C5	NC	-	Reserved for I2C		-	
C6	WCI_SIN	I	Coexistence serial interface		Tristate	1V8
C8	NC	-	Not Connected		-	
C9	NC	-	Reserved for USB		-	
D1	NC	-	Reserved for PCIe		-	
D2	NC	-	Not Connected		-	
D3	CONFIG[0]	I/O	Configuration pin: CON[0]	RF control: RF_CNTL0_N	Drive low	VIO
D7	NC	-	Not Connected		-	
D8	PCM_CLK	I/O	PCM data clock	GPIO mode: GPIO[6] I2S mode: I2S_BCLK	Tristate	VIO
D9	NC	-	Reserved for USB		-	
E1	NC	-	Reserved for PCIE		-	
E2	NC	-	Not Connected		-	
E3	CONFIG[1]	I/O	Configuration pin: CON[1]	RF control: RF_CNTL2_N	Drive low	VIO
E4	GND	-	Ground		-	
E5	GND	-	Ground		-	
E7	BT_WAKE_HOST	I/O	Bluetooth to host wake-up	GPIO mode: GPIO[0]	Drive low	VIO
E8	PCM_MCLK	I/O	PCM clock signal	GPIO mode: GPIO[3] I2S mode: I2S_CCLK JTAG mode: JTAG_TDO	Tristate	VIO

No.	Name	I/O	Description	Alt. functions	Power Down	Power supply domain
E9	PCM_DIN	I/O	PCM data in	PCM mode: PCM_DOUT GPIO mode: GPIO[5] I2S mode: I2S_DOUT/I2S_DIN	Tristate	VIO
F1	NC	-	Reserved for PCIe		-	
F2	NC	-	Not Connected		-	
F3	RF_CNTL3_P	I/O	RF control	Configuration pin: CON[5] Antenna diversity: External antenna selection signal if two antennas are used. Only available on MAYA-W160, MAYA-W161, and MAYA-W166-01B	Drive high	VIO
F4	GND	-	Ground		-	
F5	GND	-	Ground		-	
F7	WLAN_WAKE_HOST	I/O	WLAN to host wake-up	GPIO mode: GPIO[1] Configuration pin: CON[9]	Tristate	VIO
F8	PCM_SYNC	I/O	PCM frame sync	GPIO mode: GPIO[7] I2S mode: I2S_LRCLK	Tristate	VIO
F9	PCM_DOUT	I/O	PCM data out	PCM mode: PCM_DIN GPIO mode: GPIO[4] I2S mode: I2S_DOUT/I2S_DIN Bluetooth to host wake-up	Tristate	VIO
G1	NC	-	Reserved for PCIe		-	
G2	NC	-	Not Connected		-	
G3	NC	-	Not Connected		-	
G4	NC	-	Not Connected		-	
G5	NC	-	Not Connected		-	
G7	GPIO[2]	I/O	GPIO	JTAG mode: JTAG_TDI	Tristate	VIO
G8	UART_SIN	I	UART serial data in	GPIO mode: GPIO[9]	Tristate	VIO
G9	UART_SOUT	O	UART serial data out	GPIO mode: GPIO[10]	Tristate	VIO
H1	NC	-	Reserved for PCIe		-	
H2	NC	-	Reserved for PCIe		-	
H3	NC	-	Not Connected		-	
H4	GND	-	Ground		-	
H5	GND	-	Ground		-	
H7	WLAN_RESET	I/O	WLAN reset	GPIO mode: GPIO[14] JTAG mode: JTAG_TCK	Tristate	VIO
H8	UART_CTSn	I	UART CTSn	GPIO mode: GPIO[8] Configuration pin: CON[7]	Drive low	VIO
H9	UART_RTSn	O	UART RTSn	GPIO mode: GPIO[11] Configuration pin: CON[8]	Drive high	VIO
J1	NC	-	Reserved for PCIe		-	
J2	NC	-	Reserved for PCIe		-	
J3	PDn	I	Power Down Signal:		-	1V8

No.	Name	I/O	Description	Alt. functions	Power Down	Power supply domain
			• 0 = power-down mode • 1=normal mode Can accept an input of 1.8 V to 4.5 V. Internal 10 kΩ pull-up to 1V8 on this pin.			
J4	NC	-	Not Connected		-	
J5	NC	-	Not Connected		-	
J7	BT_RESET	I/O	Bluetooth reset	GPIO mode: GPIO[15] JTAG mode: JTAG_TMS	Drive high	VIO
J8	WLAN_DEV_WAKE	I/O	WLAN device wake-up	GPIO mode: GPIO[13] UART mode: UART_DTRn	Drive high	VIO
J9	BT_DEV_WAKE	I/O	Bluetooth device wake-up	GPIO mode: GPIO[12] UART mode: UART_DSRn	Tristate	VIO
K1	RF_ANT0	RF	WLAN I/O (only in MAYA-W161)		-	
K2	GND	-	Ground		-	
K3	GND	-	Ground		-	
K4	GND	-	Ground		-	
K5	NC	-	Reserved for RF_ANT		-	
K6	GND	-	Ground		-	
K7	GND	-	Ground		-	
K8	GND	-	Ground		-	
K9	RF_ANT1	RF	Bluetooth I/O – in MAYA-W161 Combined Bluetooth I/O and WLAN I/O – in MAYA-W166-01B		-	
L1	GND	-	Ground		-	
L9	GND	-	Ground		-	
M1	GND	-	Ground		-	
M2	GND	-	Ground		-	
M8	GND	-	Ground		-	
M9	GND	-	Ground		-	

Table 16: MAYA-W1 series pin description

4 Electrical specifications

⚠ Stressing the device above one or more of the ratings of the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these ratings or in conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Units
3V3	Power supply voltage	0	4.2 (DC)	V
1V8	Power supply voltage 1.8 V	-	1.98	V
VIO	I/O supply voltage 1.8 V	-	2.2	V
	I/O supply voltage 3.3 V	-	4.0	V
VIO_SD	SDIO power supply voltage 1.8 V	-	2.2	V
	SDIO power supply voltage 3.3 V	-	4.0	V
$T_{STORAGE}$	Storage temperature	-40	+85	°C

Table 17: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification given in Table 17 must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD ratings

Applicability	Immunity level	Immunity level	Units
Human Body Model (HBM), ANSA/ESDA/JEDEC JS-001-2014.	±2000	±2000	V
Charged Device Model (CDM), JESD22-C101.	±500	±2000	V

Table 18: Maximum ESD ratings

4.2 Operating conditions

Symbol	Parameter	Min.	Typ	Max.	Units
3V3	Power supply voltage	2.80	-	3.60	V
1V8	Power supply voltage 1.8 V	1.71	1.80	1.89	V
VIO	I/O supply voltage 1.8 V	1.62	1.80	1.98	V
	I/O supply voltage 3.3 V	2.97	3.30	3.47	V
VIO_SD	I/O supply voltage 1.8 V	1.62	1.80	1.98	V
	I/O supply voltage 3.3 V	2.97	3.30	3.47	V
T_A	Ambient operating temperature	-40	-	+85	°C
Ripple Noise	Peak-to-peak voltage ripple on all supply lines.	-	-	30	mV

Table 19: Operating conditions

4.3 Digital pad ratings

Symbol	Parameter	VIO	Min.	Max.	Units
V_{IH}	Input high voltage	1.8 V - 3.3 V	0.7*VIO	VIO+0.4	V
V_{IL}	Input low voltage	1.8 V - 3.3 V	-0.4	0.3*VIO	V
V_{HYS}	Input hysteresis	1.8 V - 3.3 V	100	-	mV
V_{OH}	Output high voltage	1.8 V - 3.3V	VIO-0.4	-	V
V_{OH}	Output low voltage	1.8 V - 3.3 V	-	0.4	V

Table 20: DC characteristics VIO

4.4 Power consumption

4.4.1 Wi-Fi power consumption

Conditions: 25 °C, 1V8=1.8 V, 3V3=3.3 V, VIO=VIO_SD=1.8 V, SDIO-UART Host Interface configuration, SDIO 3.0 DDR50 (4-bit mode), unless otherwise specified.

Wi-Fi operation modes	3V3 (3.3V) [mA]	1V8 (1.8 V) [mA]	VIO+VIO_SD (1.8 V) [mA]
Power – save modes **Conditions:** 25 °C, nominal voltages, SDIO-UART, SDIO 3.0 10 MHz (4-bit mode)			
Power down	0.20	0.17	0.004
Wi-Fi alone enabled	0.15	0.66	0.3
Wi-Fi and Bluetooth in deep-sleep	0.15	0.68	0.3
IEEE Power Save DTIM 10 and BT deep-sleep	0.15	0.83	0.3
IEEE Power Save DTIM 5 and BT deep-sleep	0.15	0.96	0.3
IEEE Power Save DTIM 3 and BT deep-sleep	0.15	1.1	0.3
IEEE Power Save DTIM 1 and BT deep-sleep	0.15	2.1	0.3
Active transmit modes			
CCK 1Mbps, BW20, Ch6, 19 dBm	300	210	0.3
CCK 11Mbps, BW20, Ch6, 19 dBm	310	210	0.3
OFDM 54 Mbps, BW20, Ch6, 18dBm	230	205	0.3
OFDM 54 Mbps, BW20, Ch100, 18dBm	185	280	0.3
MCS0, HT20, Ch6, 16 dBm	250	210	0.3
MCS7, HT20, Ch6, 16 dBm	230	200	0.3
MCS0, HT40, Ch6, 16 dBm	240	215	0.3
MCS7, HT40, Ch6, 16 dBm	210	205	0.3
MCS0, HT20, Ch100, 16 dBm	160	290	0.3
MCS7, HT20, Ch100, 16 dBm	150	270	0.3
MCS0, HT40, Ch100, 16 dBm	155	300	0.3
MCS7, HT40, Ch100, 16 dBm	135	275	0.3
Receive modes			
CCK 11 Mbps, BW20, Ch6, -50 dBm	0.17	75	0.3
OFDM 54 Mbps, BW20, Ch6, -50dBm	0.17	83	0.3
OFDM 54 Mbps, BW20, Ch100, -50dBm	0.17	103	0.3
MCS7, HT20, Ch6, -50 dBm	0.17	80	0.3
MCS7, HT40, Ch100, -50 dBm	0.17	88	0.3
MCS7, HT20, Ch100, -50 dBm	0.17	100	0.3
MCS7, HT40, Ch100, -50 dBm	0.17	117	0.3

Wi-Fi operation modes	3V3 (3.3V) [mA]	1V8 (1.8 V) [mA]	VIO+VIO_SD (1.8 V) [mA]
Peak current (at room temperature)			
Active transmission	350	350	-
Firmware initialization	750	450	-

Table 21: Wi-Fi radio typical current consumption with different modes of operation

4.4.2 Bluetooth power consumption

Bluetooth operation modes	3V3 (3.3 V) [mA]	1V8 (1.8 V) [mA]	VIO+VIO_SD (1.8 V) [mA]
Operating modes			
Bluetooth alone (SDIO not connected)	0.15	0.16	0.08
Bluetooth classic inquiry scan	0.15	0.78	0.08
Bluetooth classic page scan	0.15	0.78	0.08
Bluetooth LE advertisement (interval = 1.28 s)	0.15	0.38	0.08
Bluetooth LE scanning (interval = 1.28 s, window = 11.25 ms)	0.15	0.68	0.08
Active transmit mode			
Bluetooth BDR DH5, 10 dBm, Ch39, 50% duty cycle	0.15	40	0.08
Bluetooth EDR 2-DH5, 7 dBm, Ch39, 50% duty cycle	0.15	37	0.08
Bluetooth EDR 3-DH5, 7 dBm, Ch39, 50% duty cycle	0.15	36	0.08
Bluetooth LE 1M PHY, PRBS9, 6dBm, Ch19, 50% duty cycle	0.15	29	0.07
Active receive mode			
Bluetooth BDR DH1, 1 Mbps, Ch39	0.15	26	0.08
Bluetooth BDR DH5, 1 Mbps, Ch39	0.15	17	0.08
Bluetooth EDR 2DH5, 2 Mbps, Ch39	0.15	17	0.08
Bluetooth EDR 3DH5, 3 Mbps, Ch39	0.15	17	0.08
Bluetooth LE 1M PHY, PRBS9, Ch19, 100% duty cycle	0.15	30	0.08

Table 22: Bluetooth typical current consumption with different modes of operation

4.5 Radio specification

4.5.1 Bluetooth

Parameter	Specification
RF Frequency Range	2.402 – 2.480 GHz
Supported Modes	Bluetooth 5.2 Bluetooth LE • LE long range • Shared RF with BR/EDR • 2 Mbps LE
Modulation	1 Mbit/s: GFSK (BR) 2 Mbit/s: π/4 DQPSK (EDR) 3 Mbit/s: 8DQPSK (EDR)
Transmit Power	Class 1 BR: +8 dBm ± 2 dB
	Class 1 EDR: +7 dBm ± 2 dB
	Bluetooth LE: +7 dBm ± 2 dB
Receiver sensitivity (typical values)	Bluetooth BR: -94 dBm ± 1.5 dB
	Bluetooth EDR: -88 dBm ± 1.5 dB
	Bluetooth LE: -95 dBm ± 1.5 dB Bluetooth LE Coded PHY: -100 dBm ± 1.5 dB

Table 23: Bluetooth radio parameters

4.5.2 Wi-Fi

MAYA-W1 series modules support dual-band Wi-Fi with 802.11a/b/g/n operation in the 2.4 GHz and 5 GHz radio bands. The module is designed to operate in only one frequency band at a time.

Parameter	Operation Mode	Specification
RF Frequency range	802.11b/g/n	2.400 – 2.500 GHz
	802.11a/n	4.900 – 5.825 GHz
Modulation	802.11b	CCK and DSSS
	802.11a/g/n	OFDM
Supported data rates	802.11b	1, 2, 5.5, 11 Mbps
	802.11a/g	6, 9, 12, 18, 24, 36, 48, 54 Mbps
	802.11n SISO	MCS0 – MCS7 (150 Mbps)
Supported channel bandwidth	802.11n	20, 40 MHz
Supported guard interval (GI)	802.11n	400, 800 ns

Table 24: Wi-Fi radio parameters

Parameter		Operation Mode	802.11 EVM limit	Specification (typ. output power tolerance ± 2 dB)
Maximum transmit power	2.4 GHz	DSSS/CCK	-9 dB	18 dBm
		OFDM, BPSK	-8 dB	18 dBm
		OFDM, QPSK	-13 dB	18 dBm
		OFDM, 16-QAM	-19 dB	18 dBm
		OFDM, 64-QAM, 3/4	-25 dB	16 dBm
		OFDM, 64-QAM, 5/6	-27 dB	16 dBm
	5 GHz	OFDM, BPSK	-5 dB	18 dBm
		OFDM, QPSK	-13 dB	18 dBm
		OFDM, 16-QAM	-19 dB	18 dBm
		OFDM, 64-QAM, 3/4	-25 dB	16 dBm
		OFDM, 64-QAM, 5/6	-27 dB	16 dBm

Table 25: Wi-Fi radio maximum transmit power parameter

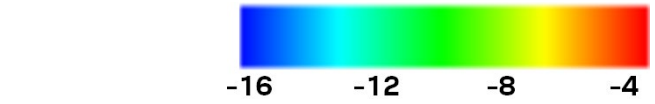
Band	Operating mode	Data rate	Bandwidth	Specification
2.4 GHz	802.11b	1 Mbps / 2 Mbps	20 MHz	-98 dBm / -94 dBm
		5.5 Mbps / 11 Mbps		-94 dBm / -90 dBm
	802.11g	6 Mbps / 9 Mbps	20 MHz	-91 dBm / -91 dBm
		12 Mbps / 18 Mbps		-91 dBm / -89 dBm
		24 Mbps / 36 Mbps		-86 dBm / -82 dBm
		48 Mbps / 54 Mbps		-78 dBm / -77 dBm
	802.11n	MCS0 / MCS1	20 MHz	-91 dBm / -90 dBm
		MCS2 / MCS3		-87 dBm / -84 dBm
		MCS4 / MCS5		-81 dBm / -76 dBm
		MCS6 / MCS7		-75 dBm / -73 dBm
		MCS0 / MCS1	40 MHz	-87 dBm / -87 dBm
		MCS2 / MCS3		-84 dBm / -82 dBm
		MCS4 / MCS5		-77 dBm / -74 dBm
		MCS6 / MCS7		-72 dBm / -71 dBm

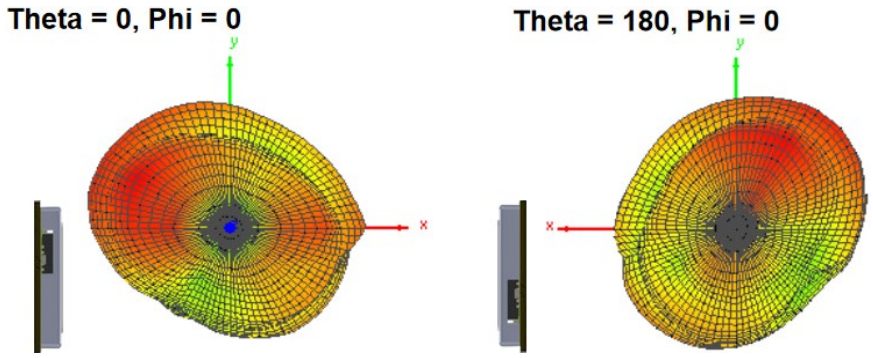
Band	Operating mode	Data rate	Bandwidth	Specification
5 GHz	802.11a	6Mbps/9Mbps	20 MHz	-90 dBm / -90 dBm
		12 Mbps/18 Mbps		-89 dBm / -87 dBm
		24 Mbps/36 Mbps		-84 dBm / -80 dBm
		48 Mbps/54 Mbps		-76 dBm / -75 dBm
	802.11n	MCS0 / MCS1	20 MHz	-90 dBm / -87 dBm
		MCS2 / MCS3		-85 dBm / -82 dBm
		MCS4 / MCS5		-79 dBm / -75 dBm
		MCS6 / MCS7		-72 dBm / -70 dBm
		MCS0 / MCS1	40 MHz	-86 dBm / -85 dBm
		MCS2 / MCS3		-82 dBm / -79 dBm
		MCS4 / MCS5		-76 dBm / -72 dBm
		MCS6 / MCS7		-70 dBm / -69 dBm

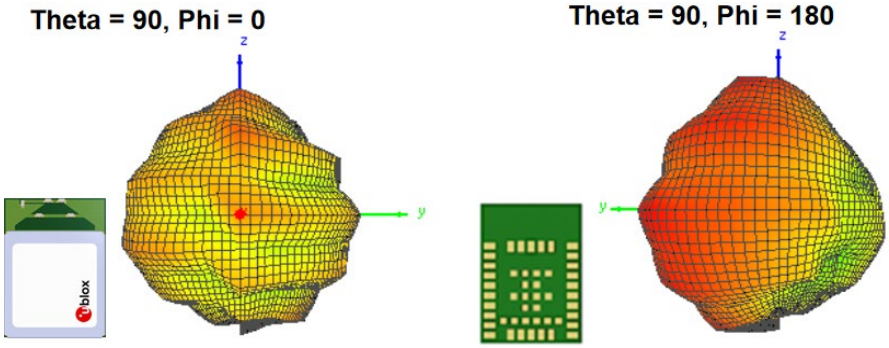
Table 26: Wi-Fi receiver characteristics

4.5.3 Antenna Radiation Patterns

The radiation patterns displayed in Table 27 and Table 28 show the radiation patterns of MAYA-W166-00B with internal PCB trace antenna for 2.44 GHz and 5.5 GHz. Table 29 shows the TRP and peak gain for the low, mid, and high channel of the 2.4 GHz and 5 GHz frequency bands.







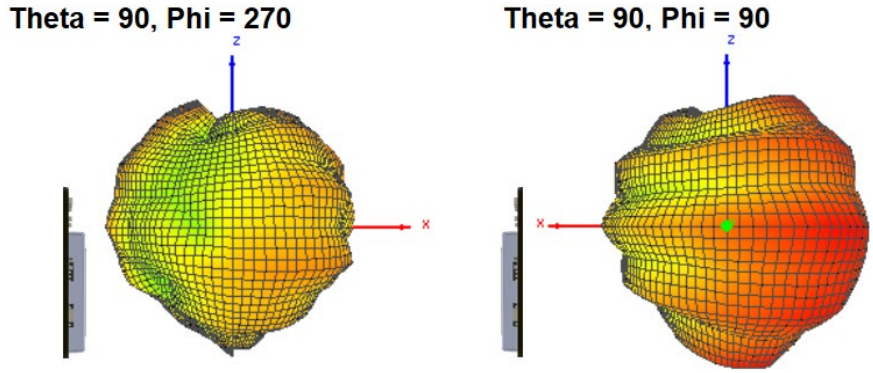
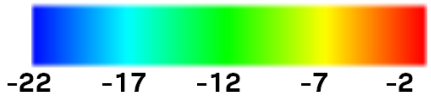
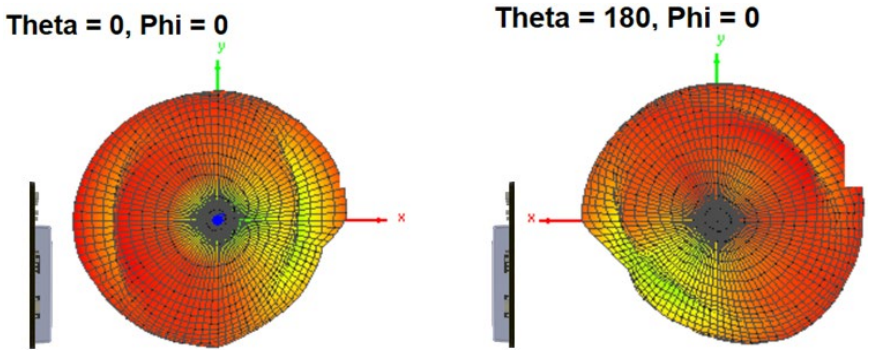
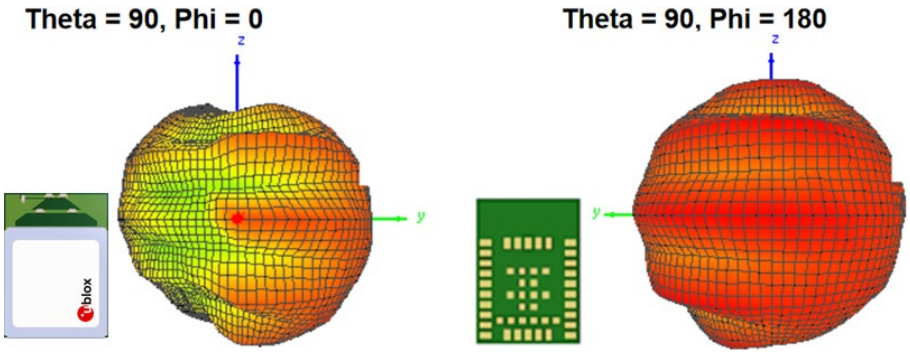


Table 27: Wi-Fi and Bluetooth antenna characteristics at 2.44 GHz







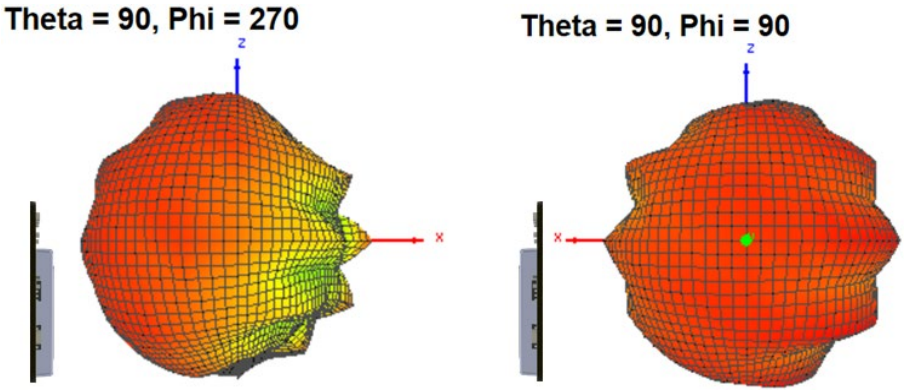


Table 28: Wi-Fi antenna characteristics at 5.50 GHz

Transmission	Measured TRP	Measured peak gain
Channel 1, 2.412 GHz	-6.80 dBm	-3.42 dBi
Channel 6, 2.437 GHz	-6.65 dBm	-4.36 dBi
Channel 13, 2.472 GHz	-7.96 dBm	-5.81 dBi
Channel 36, 5.180 GHz	-3.49 dBm	-0.87 dBi
Channel 100, 5.500 GHz	-3.66 dBm	-1.51 dBi
Channel 159, 5.795 GHz	-4.23 dBm	-2.08 dBi

Table 29: Measured radiated power and peak gain for 0 dBm transmission power

5 Software

MAYA-W1 series modules are based on the NXP IW416 chipset and the drivers and firmware required to operate the modules are developed by NXP. A firmware binary is downloaded by the host operating system driver at start-up.

The following software options are available for the MAYA-W1 module:

- Open-source Linux/Android driver (`mxm_mwifiex`) for mainstream use is available free of charge and already integrated into Linux BSP for NXP i.MX application processors
- MCUXpresso Wi-Fi/Bluetooth support for supported NXP MCUs

The software packages typically include:

- Dedicated kernel driver that binds the Wi-Fi device to the kernel. Driver sources are provided.
- Dedicated Wi-Fi firmware image that is uploaded during initialization of the Wi-Fi device.
- Dedicated Bluetooth firmware image that is uploaded during initialization of the Bluetooth device.
- Wi-Fi and Bluetooth release notes and a list of supported software features.
- Laboratory and manufacturing tools.

6 Mechanical specifications

6.1 MAYA-W1 footprint dimensions

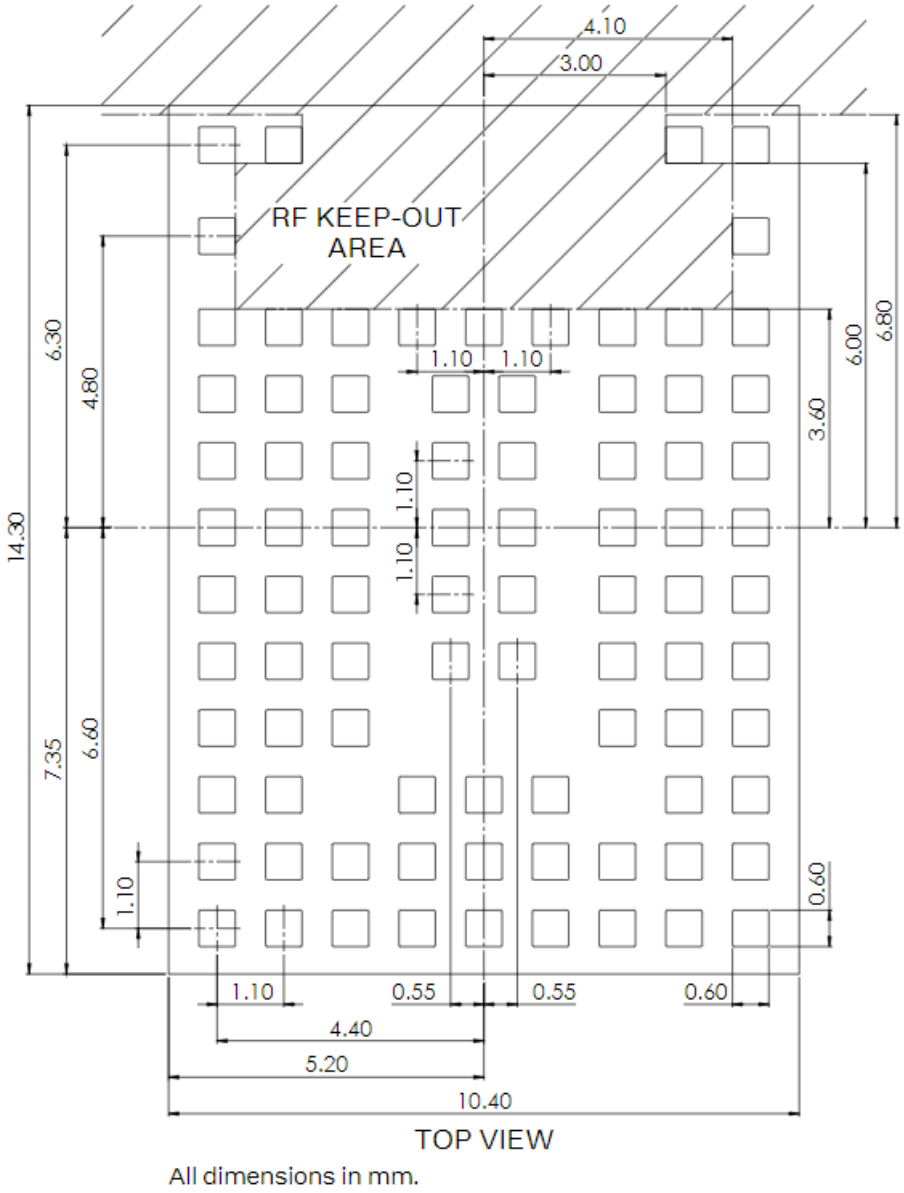


Figure 14: MAYA-W1 footprint dimensions

Parameter	Typical	Tolerance
Seating Plane Coplanarity [mm]	<0.1	
Pin Width [mm]	0.60	+0.015/-0.015
Pin Length [mm]	0.60	+0.015/-0.015

Table 30: Dimensions parameters

6.2 MAYA-W1 Mechanical specification

6.2.1 MAYA-W166

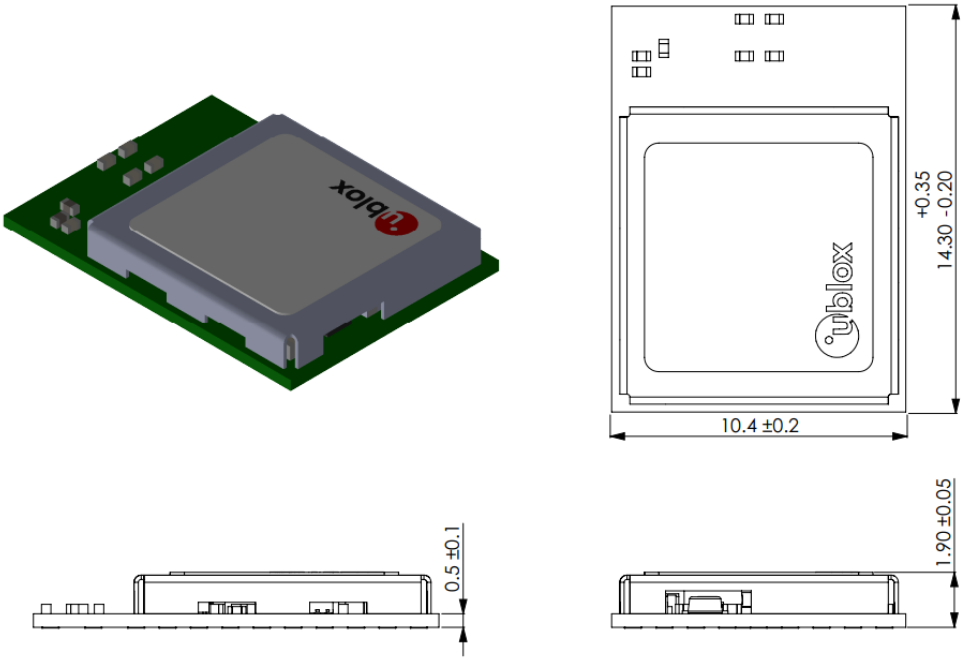


Figure 15: MAYA-W166 mechanical specification

6.2.2 MAYA-W161

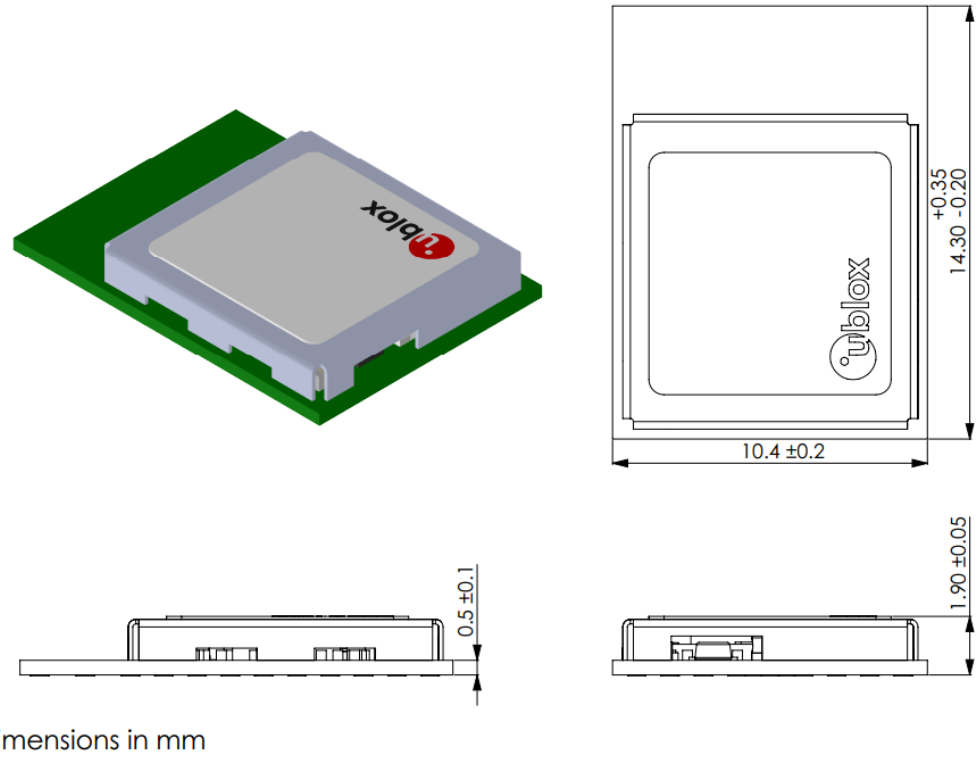


Figure 16: MAYA-W161 mechanical specification

6.2.3 MAYA-W160

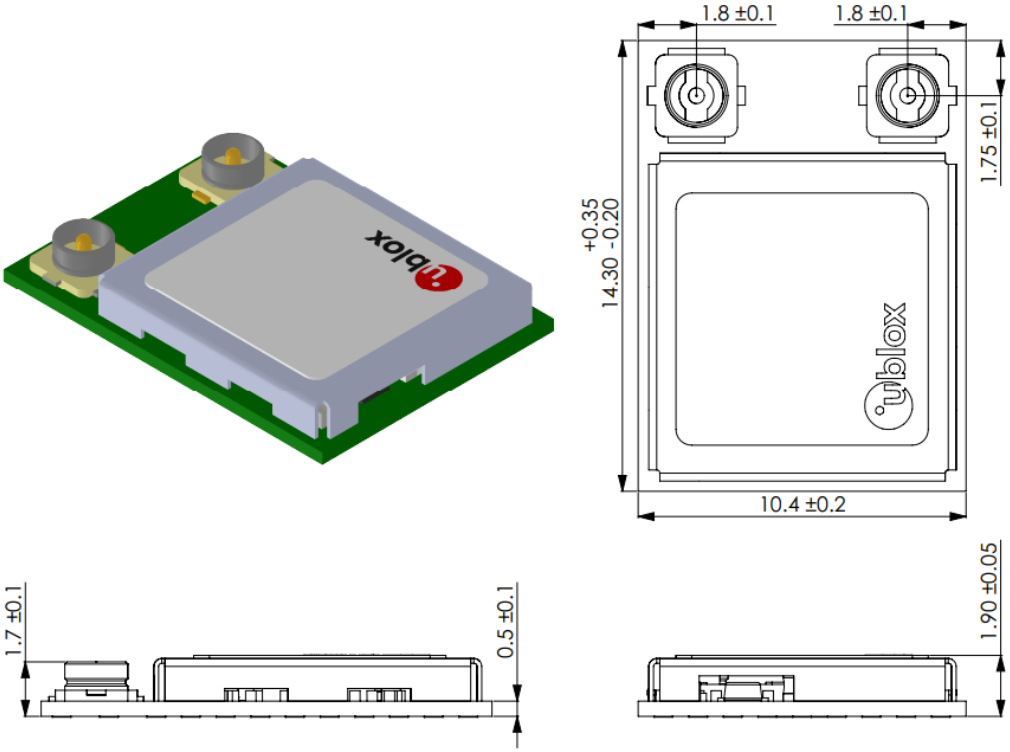


Figure 17: MAYA-W160 mechanical specification

6.3 Module weight

Module	Typ	Unit
MAYA-W160	<1	g
MAYA-W161	<1	g
MAYA-W166	<1	g

Table 31: Module weight

7 Qualification and approvals

7.1 Country approvals

Table 32 describes the status of MAYA-W1 module certification in each country/region.

Country/region	MAYA-W160	MAYA-W161	MAYA-W166
Europe	Approved	Approved	Approved
Great Britain	Approved	Approved	Approved
USA	Approved	Approved	Approved
Canada	Approved	Approved	Approved
Japan	Approved	Approved	Approved
South Korea	Approved	Approved	Approved
Brazil	Approved	Not approved	Not approved

Table 32: Country approval status

Additional country certifications can be progressed upon request. Contact your local support team for further information.

For detailed information about the regulatory requirements that must be met when using MAYA-W1 modules in an end product, see the system integration manual [2].

7.2 Bluetooth qualification

End products must be qualified and listed with the Bluetooth Special Interest Group (SIG).

Product declarations are submitted through the Bluetooth Launch Studio website.

MAYA-W1 series modules are qualified as a Controller Subsystem against Bluetooth Core 5.2 specification and are registered with the SIG Qualified Design IDs (QDID) shown in Table 33.

To list your product that integrates MAYA-W1 with no additional testing required, combine the QDID of the pre-qualified Controller Subsystem, as shown in Table 33, with the QDID of a Bluetooth stack implemented in the Host Subsystem.

Model	Product type	QD ID	Listing date
MAYA-W160, MAYA-W161, MAYA-W166	Controller subsystem	192202	2022-07-22

Table 33: MAYA-W1 series Bluetooth qualified design IDs

8 Product handling

8.1 Packaging

MAYA-W1 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the Product packaging guide [1].

8.1.1 Reels

MAYA-W1 series modules are deliverable in quantities of 500 pieces on a reel. MAYA-W1 series modules are shipped on reel Type A3 as described in the Product packaging guide [1].

8.1.2 Tapes

Figure shows the position and orientation of MAYA-W1 series modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 19.

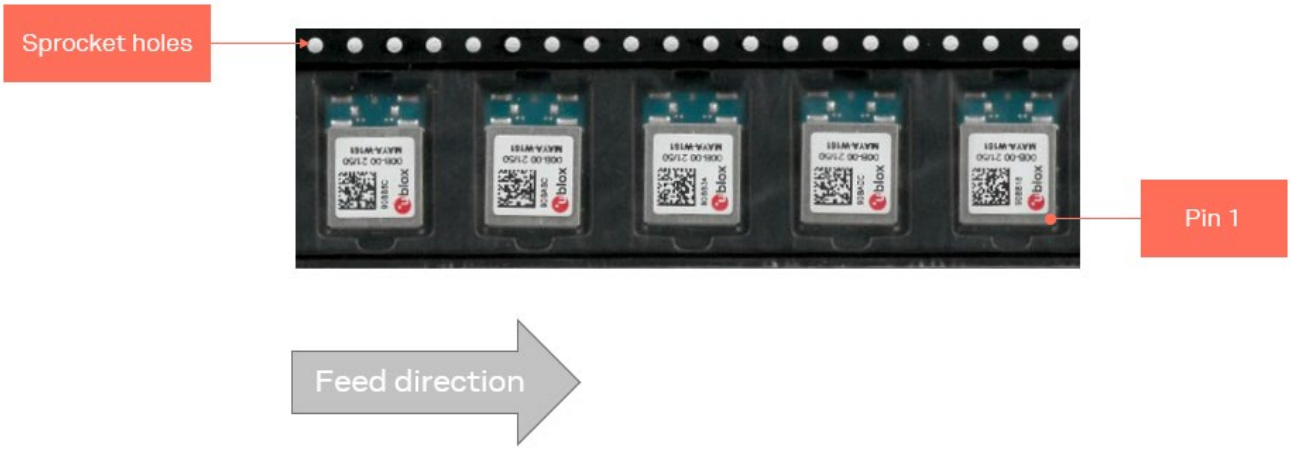


Figure 18: Orientation of MAYA-W1 modules on tape

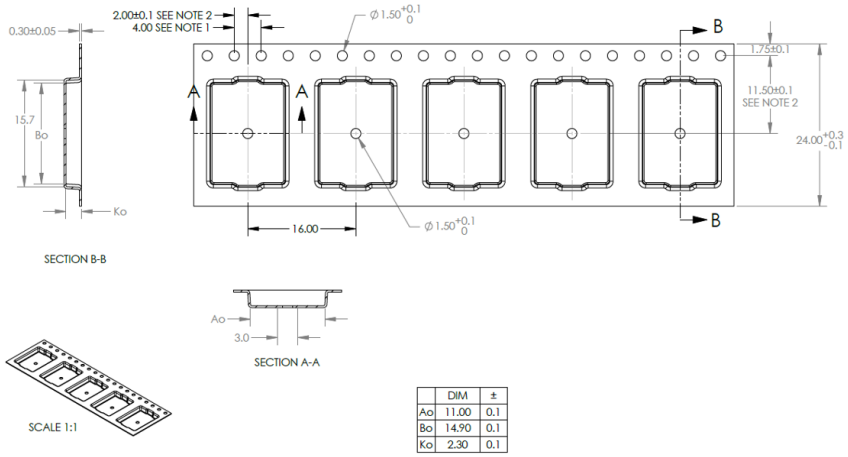


Figure 19: MAYA-W1 tape dimensions

8.2 Moisture sensitivity levels

⚠ MAYA-W1 series modules are rated as MSL Level 4 devices in accordance with the IPC/JEDEC J STD-020 standard. For detailed information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 72 hours in factory conditions of maximum 30 °C/60%RH or must be stored at less than 10%RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033B standard.

For more information regarding MSL (Moisture Sensitivity Level), labeling, and storage, see also the Product packaging guide [1].

8.3 Reflow soldering

Reflow profiles must be selected in accordance with u-blox recommendations:

- MAYA-W160 is suitable for one time reflow.
- MAYA-W161 and MAYA-W166 are suitable for two time reflow.

⚠ Reflow soldering profiles must be selected in accordance with u-blox soldering recommendations described in the system integration manual [2]. Failure to observe these recommendations can result in severe damage to the product.

8.4 ESD handling precautions

⚠ MAYA-W1 series modules are electrostatic sensitive devices (ESD) that demand adherence to special ESD precautions. Failure to observe these recommendations can result in severe damage to the product.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates MAYA-W1. We recommend that the module is not handled in a non-ESD protected environment. The **RF_ANT** pins are especially sensitive to ESD and special care must be taken when connecting antennas. ESD safe soldering equipment is recommended.

9 Labeling and ordering information

9.1 Product labeling

The labels applied to MAYA-W1 series modules include important product information. Figure 18 shows the given label information, where each of the given references are described in Table 34.

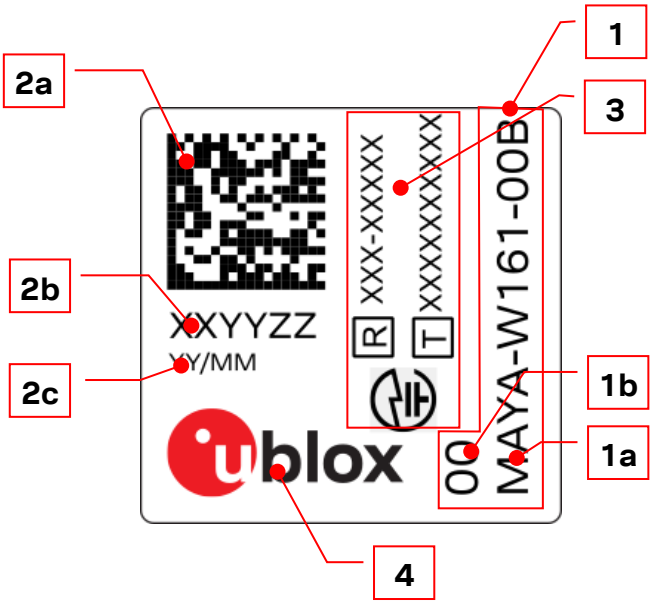


Figure 18: Label information shown on the MAYA-W1 series modules

Reference	Description
1	Text box containing product name and version
1a	Text MODEL: and Product name (ID)
1b	Product version
2a	Data Matrix with unique serial number of 19 alphanumeric symbols: • The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. • The following 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF. See also MAC addresses. • The last 4 symbols represent the hardware and firmware version encoded HHFF.
2b	The six last hex symbols of the MAC address (AABBCC**DDEEFF**)
2c	Date of production in the format YY/WW (year/week)
3	Japan certification IDs
4	u-blox logo, where the red dot indicates the position of pin no 1

Table 34: MAYA-W1 series label references

9.2 Explanation of codes

Table 35 describes the three product identifiers: namely, the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Product name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products.	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade.	PPPP -TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers that describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 35: Product code formats

9.3 Identification codes

Code	Meaning	Example
PPPP	Form factor	MAYA
TG	Platform (Technology and Generation) T – Dominant technology, For example, W: Wi-Fi, B: Bluetooth® G - Generation	W1: Wireless Generation 1
VV	Variant based on the same platform; range [00...99]	60, 61, or 66
TT	Major Product Version	00: first version
Q	Quality grade A: Automotive B: Professional C: Standard	B: Professional grade
XX	Minor product version (not relevant for certification)	Default value: 00

Table 36: Part identification code

9.4 Ordering information

Ordering code	Product
MAYA-W160-00B	Professional grade module with two separate U.FL connectors for Wi-Fi and Bluetooth
MAYA-W161-00B	Professional grade module with two separate antenna pins for Wi-Fi and Bluetooth
MAYA-W161-00C	Standard grade module with two separate antenna pins for Wi-Fi and Bluetooth
MAYA-W166-00B	Professional grade module with embedded PCB antenna for Wi-Fi and Bluetooth
MAYA-W166-01B	Professional grade module with single antenna pin for Wi-Fi and Bluetooth

Table 37: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to digital converter
BPF	Band pass filter
CAN	Controller area network
CTS	Clear to send
DC	Direct current
DSR	Data set ready
DTR	Data terminal ready
EIRP	Effective isotropic radiated power
GND	Ground
GPIO	General purpose input/output
H	High
I	Input (means that this is an input port of the module)
IEEE	Institute of Electrical and Electronics Engineers
I^2C	Inter-integrated circuit
L	Low
LPO	Low power oscillator
MIMO	Multi-input multi-output
MSD	Moisture sensitive device
N/A	Not applicable
O	Output (means that this is an output port of the module)
PCN/IN	Product change notification / Information note
PD	Pull-down
PU	Pull-up
RMII	Reduced media independent interface
RTS	Request to send
RXD	Receive data
SDIO	Secure digital input output
SPI	Serial peripheral interface
TXD	Transmit data
UART	Universal asynchronous Receiver/Transmitter
USB	Universal serial bus

Table 38: Explanation of the abbreviations and terms used

Related documents

[1] Product packaging guide, UBX-14001652
[2] MAYA-W1 system integration manual, UBX-21010495
MAYA-W1 product summary, UBX-20047825

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	31-May-2021	bcur	Initial release
R02	21-Jan-2022	lber, bcur, epla, mzes	Added power down column in the Pin assignment. Updated the Block diagrams. Corrected internal MAYA-W166 antenna type from PIFA to Niche in Product description and Internal antenna sections. Added Antenna Radiation Patterns. Added power-down data to Pin assignment. Added Software support section. Replaced tentative power consumption values with Radio specification. Added specifications for Wi-Fi power consumption, Bluetooth power consumption, and Digital pad ratings. Updated Power up sequence timing. Updated drawings in Mechanical specifications. Removed ambiguous description of operating condition ranges in Electrical specifications. Updated information describing Moisture sensitivity levels, Reflow soldering, and ESD handling precautions. Updated Bluetooth specification to 5.2.
R03	08-Apr-2022	epla	Corrected power consumption for WLAN and Bluetooth modes in Power consumption section. Added consumption data for power save modes in Table 21 and Table 22. Added rows with peak current consumptions in Table 21. Added MAYA-W166-01B variant with single antenna pin.
R04	08-Jul-2022	epla	Updated product status to Initial Production for MAYA-W161 and MAYA-W166-00B variants in Document information. Removed the previously duplicated list of Approved antennas now maintained in the system integration manual. Updated cover images and contact information.
R05	24-Aug-2022	mzes, frca, epla	Revised Product handling information. Added Packaging information. Updated status of W166-01 variant to Initial Production in Document information. Changed output power for Bluetooth classic from 10 to 8 dBm in Radio specification. Corrected peak current consumption value for 1.8 V in Wi-Fi power consumption table data. Updated Related documents. Corrected MSL 4 mount time after opening the dry pack in Moisture sensitivity levels. Removed unsupported SDIO host i/f option for Bluetooth in Table 3.
R06	11-Nov-2022	epla, frca	Updated tolerances for the module length in Mechanical specifications and corrected reel tape type in Packaging.
R07	02-May-2023	epla, frca	Extended document scope to include MAYA-W161-00C variant: Included in Document information and all other relevant sections. Updated product status to Initial Production for MAYA-W160. Added Antenna diversity feature in External RF antenna interface and other relevant sections. Added PDn pin description in Table 16. Rationalized content in Qualification and approvals content with the compliance content now included in the SIM [2]. Included color code and pin name information in the Pin assignment.
R08	13-Dec-2023	epla	Updated product status in Document information. Removed footnote about antenna diversity being preliminary feature. Updated max. 3V3 voltage in Absolute maximum ratings and Operating conditions. Added dimension parameters in MAYA-W1 Mechanical specification. Updated maximum UART baud rate. Updated Bluetooth qualification.
R09	11-Jun-2025	frca, epla	Updated Table 33 by adding Brazil certification for MAYA-W160 and dimension parameters in MAYA-W1 Mechanical specification

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