LEXI HW migration guide

Hardware guidelines to migrate between LEXI modules

Application note

Abstract

This document provides hardware design guidelines to migrate between the u-blox cellular modules based on the ultra-small LEXI form factor.

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Document information

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This document applies to the following products:

Product name
LEXI-R422
LEXI-R520
LEXI-R10001D
LEXI-R10401D
LEXI-R10801D

Contents

1 Overview

The u-blox ultra-small LEXI form factor (16 x 16 mm, 133-pin LGA) includes the following modules, with compatible pin assignments as described in Figure 1, so that the modules can be alternatively mounted on a single application PCB using exactly the same copper, solder resist and paste mask:

- LEXI-R422 modules, supporting LTE Cat M1 / NB2 and 2G cellular radio access technology.
- LEXI-R520 modules, supporting LTE Cat M1 / NB2 cellular radio access technology, and the u-blox SpotNow A-GPS receiver technology.
- LEXI-R10 series modules, supporting LTE Cat 1bis cellular radio access technology, and the Wi-Fi scan receiver technology.

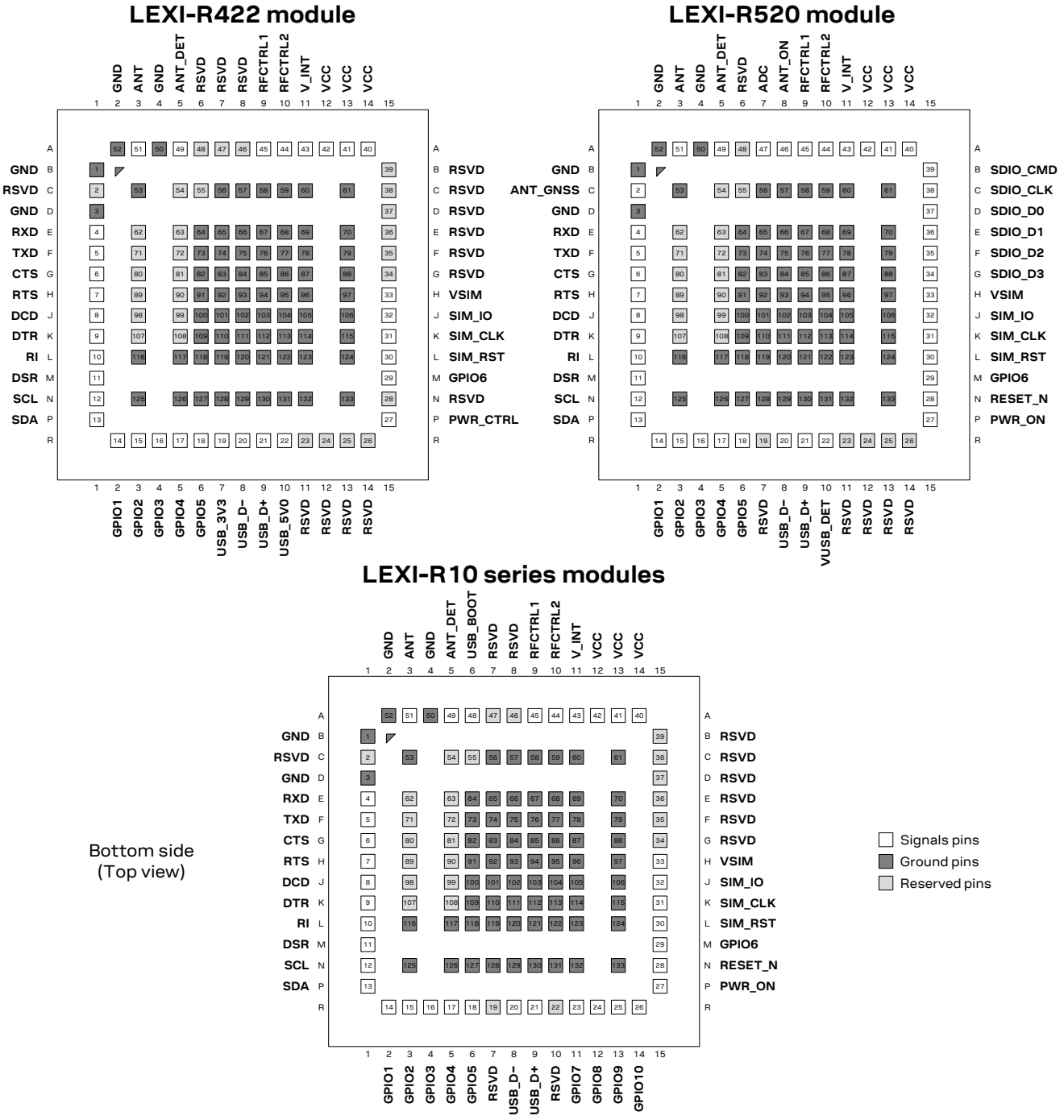

Figure 1: LEXI-R422, LEXI-R520 and LEXI-R10 series modules layout and pinout

2 Pin-out comparison between LEXI modules

Table 1 shows a detailed pin-out comparison between the LEXI-R422, LEXI-R520 and LEXI-R10 series modules, with related description of each pin, including remark for migration.

No.	ID	LEXI-R422	LEXI-R520	LEXI-R10	Description / Remark for migration
1	B1	GND	GND	GND	Ground
2	C1	RSVD	ANT_GNSS	RSVD	RF input for SpotNow A-GPS receiver on LEXI-R520. Reserved for future use on LEXI-R422 and LEXI-R10 series.
3	D1	GND	GND	GND	Ground
4	E1	RXD	RXD	RXD	1.8V UART data output
5	F1	TXD	TXD	TXD	1.8V UART data input
6	G1	CTS	CTS	CTS	1.8V UART flow control output
7	H1	RTS	RTS	RTS	1.8V UART flow control input
8	J1	DCD	DCD	DCD	1.8V UART DCD output, configurable as AUX UART data output
9	K1	DTR	DTR	DTR	1.8V UART DTR input, configurable as AUX UART data input
10	L1	RI	RI	RI	1.8V UART RI output, configurable as AUX UART flow ctrl output
11	M1	DSR	DSR	DSR	1.8V UART DSR output, configurable as AUX UART flow ctrl input
12	N1	SCL	SCL	SCL	1.8V I2C bus clock output
13	P1	SDA	SDA	SDA	1.8V I2C bus data input/output
14	R2	GPIO1	GPIO1	GPIO1	Configurable 1.8V GPIO
15	R3	GPIO2	GPIO2	GPIO2	Configurable 1.8V GPIO on LEXI-R422 and LEXI-R520. Configurable always-on 1.8V GPIO on LEXI-R10 series.
16	R4	GPIO3	GPIO3	GPIO3	Configurable 1.8V GPIO on LEXI-R422 and LEXI-R520. Configurable always-on 1.8V GPIO on LEXI-R10 series.
17	R5	GPIO4	GPIO4	GPIO4	Configurable 1.8V GPIO on LEXI-R422 and LEXI-R520. Configurable always-on 1.8V GPIO on LEXI-R10 series.
18	R6	GPIO5	GPIO5	GPIO5	Configurable 1.8V GPIO
19	R7	USB_3V3	RSVD	RSVD	3.3 V input to supply the USB interface on LEXI-R422. Reserved for future use, internally not connected, on LEXI-R520 / LEXI-R10.
20	R8	USB_D-	USB_D-	USB_D-	USB data line D-
21	R9	USB_D+	USB_D+	USB_D+	USB data line D+
22	R10	USB_5V0	VUSB_DET	RSVD	5 V input to enable the USB interface on LEXI-R422 / LEXI-R520. Reserved for future use, internally not connected, on LEXI-R10 series.
23	R11	RSVD	RSVD	GPIO7	Configurable 1.8V GPIO on LEXI-R10 series. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R520.
24	R12	RSVD	RSVD	GPIO8	Configurable 1.8V GPIO on LEXI-R10 series. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R520.
25	R13	RSVD	RSVD	GPIO9	Configurable 1.8V GPIO on LEXI-R10 series. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R520.
26	R14	RSVD	RSVD	GPIO10	Configurable 1.8V GPIO on LEXI-R10 series. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R520.
27	P15	PWR_CTRL	PWR_ON	PWR_ON	Power-on / off and reset input on LEXI-R422. Power-on / off input on LEXI-R520 and LEXI-R10 series.
28	N15	RSVD	RESET_N	RESET_N	Reset input on LEXI-R520 and LEXI-R10 series. Reserved for future use, internally not connected, on LEXI-R422.
29	M15	GPIO6	GPIO6	GPIO6	Configurable 1.8V GPIO on LEXI-R422 and LEXI-R520. Configurable always-on 1.8V GPIO on LEXI-R10 series.
30	L15	SIM_RST	SIM_RST	SIM_RST	SIM reset output for external 1.8V SIM on LEXI-R422. SIM reset output for external 1.8V / 3V SIM on LEXI-R520 / LEXI-R10.

No.	ID	LEXI-R422	LEXI-R520	LEXI-R10	Description / Remark for migration
31	K15	SIM_CLK	SIM_CLK	SIM_CLK	SIM clock output for external 1.8V SIM on LEXI-R422. SIM clock output for external 1.8V / 3V SIM on LEXI-R520 / LEXI-R10.
32	J15	SIM_IO	SIM_IO	SIM_IO	SIM data input/output for external 1.8V SIM on LEXI-R422. SIM data input/output for external 1.8V / 3V SIM on LEXI-R520 / LEXI-R10.
33	H15	VSIM	VSIM	VSIM	SIM supply output for external 1.8V SIM on LEXI-R422. SIM supply output for external 1.8V / 3V SIM on LEXI-R520 / LEXI-R10.
34	G15	RSVD	SDIO_D3	RSVD	SDIO / SPI_CS for diagnostic on LEXI-R520. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R10.
35	F15	RSVD	SDIO_D2	RSVD	SDIO / SPI_CLK for diagnostic on LEXI-R520. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R10.
36	E15	RSVD	SDIO_D1	RSVD	SDIO / SPI_MISO for diagnostic on LEXI-R520. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R10.
37	D15	RSVD	SDIO_D0	RSVD	SDIO / SPI_MOSI for diagnostic on LEXI-R520. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R10.
38	C15	RSVD	SDIO_CLK	RSVD	SDIO for diagnostic on LEXI-R520. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R10.
39	B15	RSVD	SDIO_CMD	RSVD	SDIO for diagnostic on LEXI-R520. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R10.
40	A14	VCC	VCC	VCC	Module supply input on LEXI-R520 / LEXI-R10. Module supply input connected to internal PMU on LEXI-R422.
41	A13	VCC	VCC	VCC	Module supply input on LEXI-R520 / LEXI-R10. Module supply input connected to internal RF PA on LEXI-R422.
42	A12	VCC	VCC	VCC	Module supply input on LEXI-R520 / LEXI-R10. Module supply input connected to internal RF PA on LEXI-R422.
43	A11	V_INT	V_INT	V_INT	1.8 V generic digital interface supply output.
44	A10	RFCTRL2	RFCTRL2	RFCTRL2	Antenna dynamic tuner interface output.
45	A9	RFCTRL1	RFCTRL1	RFCTRL1	Antenna dynamic tuner interface output.
46	A8	RSVD	ANT_ON	RSVD	External GPS Antenna / LNA supply control output on LEXI-R520. Reserved for future use on LEXI-R422 and LEXI-R10 series.
47	A7	RSVD	ADC	RSVD	ADC input on LEXI-R520. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R10.
48	A6	RSVD	RSVD	USB_BOOT	Input to force FW update over USB mode on LEXI-R10 series. Reserved for future use, internally not connected, on LEXI-R422 / LEXI-R520.
49	A5	ANT_DET	ANT_DET	ANT_DET	Antenna detection input.
50	A4	GND	GND	GND	Ground
51	A3	ANT	ANT	ANT	RF input/output for cellular RF signals Rx/Tx on any module. Acting also as RF input for Wi-Fi RF signals reception on LEXI-R10.
52	A2	GND	GND	GND	Ground

Table 1: LEXI-R422, LEXI-R520 and LEXI-R10 series modules pin-out comparison

As also illustrated in Figure 1, all the other pins from number 53 to number 133 that are not listed in Table 1 are pins reserved for future use or ground pins on all the LEXI-R422, LEXI-R520 and LEXI-R10 series modules. All the pins reserved for future use (RSVD) are intended to be unconnected, except:

- **RSVD** pin number **99** (**J5**) which is recommended to be externally accessible by connecting it to a dedicated Test-Point for diagnostic.

3 Design guidelines

3.1 Schematic design example

Figure 2 shows an example of a simple schematic diagram where a u-blox LEXI-R422, LEXI-R520 or LEXI-R10 series module is integrated in the same application board, using the UART interfaces for AT and data communication with the external MCU processor of the application, and using all the key supported interfaces and functions commonly used in applications integrating the LEXI form factor.

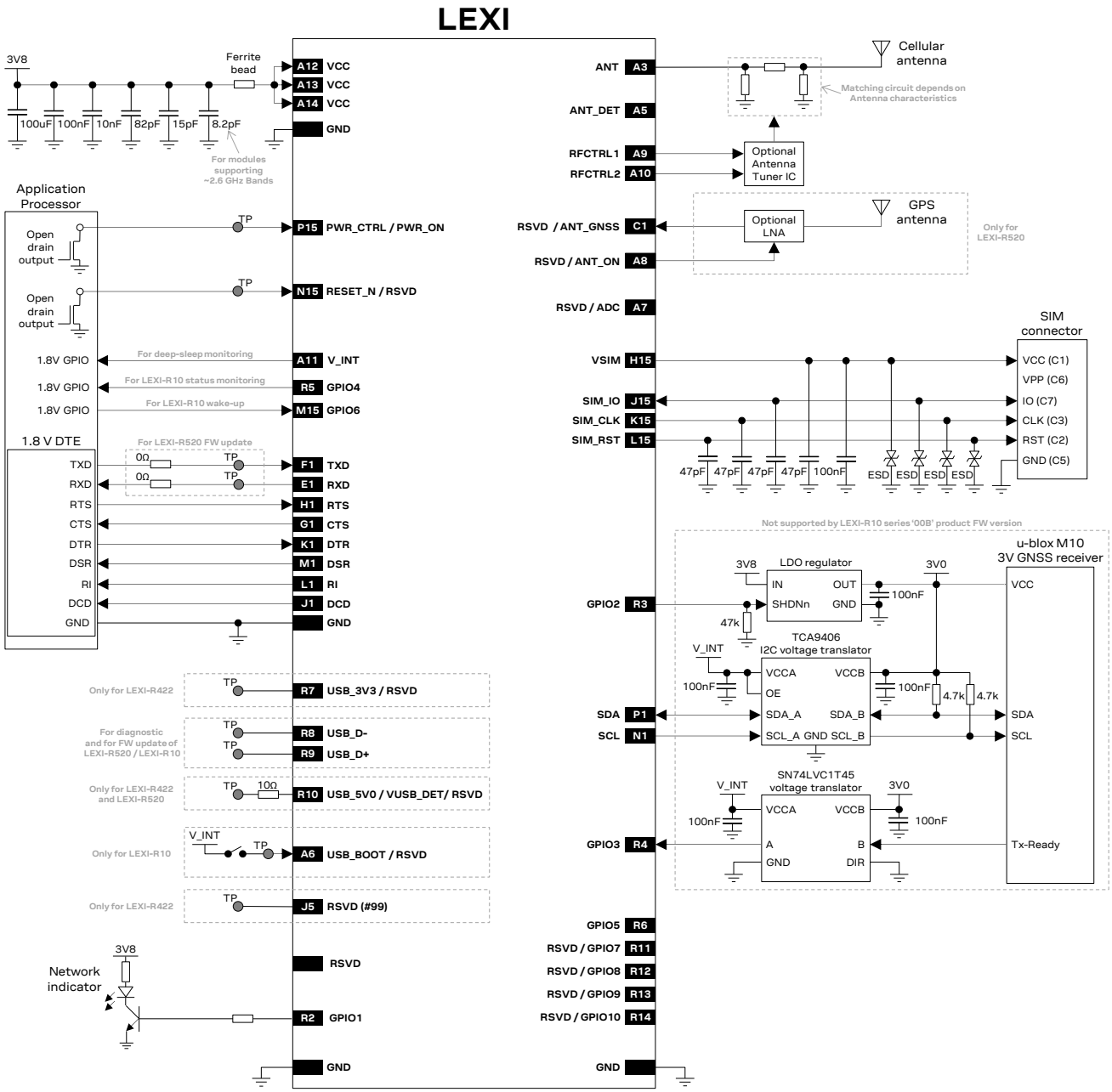

Figure 2: Example of schematic diagram to integrate a LEXI-R422, LEXI-R520 or LEXI-R10 series module

The notes and remarks included in the schematic diagram describe the purposes of the implemented circuits, the parts that may be optional, and the specific design guidelines according to the interfaces and functions supported specifically by each of the LEXI-R422, the LEXI-R520 and/or the LEXI-R10 series modules.

3.2 VCC module supply input

In the simple schematic diagram shown in Figure 2, the **VCC** supply of the LEXI modules is provided by a suitable supply source, at 3.8 V nominal voltage, not illustrated in the diagram.

All the LEXI cellular modules are designed for low power consumption, in particular in deep-sleep / PSM / eDRX operating mode, but while selecting the supply source for LEXI cellular modules, it is important considering with adequate safe design margin the maximum current consumption of each LEXI cellular module (see related data sheet [1], [5], [9]), as it reflects the RATs supported:

- LEXI-R520 are the less demanding modules in terms of current required to transmit at maximum Tx power (~23 dBm) in LTE Cat M1 / NB2 half-duplex cellular radio access technology.
- LEXI-R10 series modules may require slightly more continuous current to transmit at maximum Tx power (~23 dBm) in LTE Cat 1bis full-duplex cellular radio access technology.
- LEXI-R422 modules require much significant peak / pulse current while transmitting at maximum Tx power (~33 dBm) in 2G TDMA cellular radio access technology.

The simple schematic diagram shown in Figure 2 includes proper bypass capacitors and EMI filter parts that we recommend placing close to the **VCC** input pins of the modules, considering that the **VCC** supply line may be a source of noise, and considering that the ultra-small LEXI cellular modules are assumed to be integrated in small devices, with internal antenna and other parts placed quite near the **VCC** supply line:

- 100 µF low ESR capacitor, to avoid undershoot and overshoot at the start and at the end of RF transmission, which might increase the RF radiated spurious emissions, mainly recommended for LEXI-R422 modules supporting 2G TDMA RAT, suitable for any LEXI module.
- 100 nF 0402 ceramic capacitor, to filter digital logic noise from clocks and data sources, suitable and recommended for any LEXI module.
- 10 nF 0402 ceramic capacitor, to filter digital logic noise from clocks and data sources, suitable and recommended for any LEXI module.
- 82 pF 0402 ceramic capacitor with Self-Resonant Frequency in the low frequency cellular bands, suitable and recommended for any LEXI module.
- 15 pF 0402 ceramic capacitor with Self-Resonant Frequency in the mid frequency cellular bands, suitable and recommended for any LEXI module.
- 8.2 pF 0402 ceramic capacitor with Self-Resonant Frequency in the high frequency cellular bands or in the Wi-Fi band, suitable and recommended for LEXI-R10 series modules.
- Ferrite bead specifically designed for EMI suppression in GHz band (as Murata BLM18EG221SN1), suitable and recommended for any LEXI module.

We recommend routing the **VCC** supply line as far as possible from the RF antenna and any possible noise-sensitive part / circuit, and we recommend narrowing the **VCC** line width down to no wider than the pad of the capacitors, to adequately filter EMI, as illustrated in Figure 3.

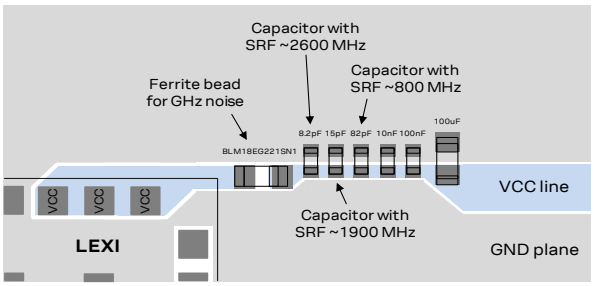

Figure 3: VCC line layout example to reduce EMI

For additional specific design guidelines about module supply design, see the **VCC** interface sections in the related system integration manual [2], [6], [10].

Applying a valid **VCC** power supply triggers different behavior of the modules:

- LEXI-R520 modules automatically switch-on by applying a valid **VCC** supply.
- LEXI-R422 and LEXI-R10 series modules continue to be switched off even after a valid **VCC** supply has been applied: the **PWR_CTRL** input line of LEXI-R422 modules or the **PWR_ON** input line of LEXI-R10 series modules must be properly toggled, with valid **VCC** supply present, to start the switch-on sequence of these modules.

3.3 V_INT 1.8 V supply output

LEXI cellular modules provide a 1.8 V supply output at the **V_INT** pin, which is internally generated when the cellular module is switched on, outside the deep sleep mode.

The same voltage domain is used internally to supply the generic digital interfaces of the modules (as the UART interfaces, I2C interface, GPIOs), and therefore we recommend using the **V_INT** supply output to supply the module side of external voltage translators connected to these interfaces of the modules.

We recommend monitoring the status of the **V_INT** output line by an input pin of the external host processor as illustrated in Figure 2, to define when the cellular module is switched on and outside the deep sleep mode. We also recommend providing a test point to access the line for diagnostic.

LEXI-R10 series modules, differently from LEXI-R422 and LEXI-R520 modules, include some special always-on GPIOs, which are the **GPIO2**, **GPIO3**, **GPIO4** and **GPIO6**, that are supplied by an always-on internal 1.8 V supply available also when the module is in ultra-low power deep-sleep mode, differently from the **V_INT** supply.

3.4 Cellular RF interface

Figure 2 shows the **ANT** cellular antenna circuit implemented with the optional antenna dynamic tuning according to the design guidelines provided in the antenna interface sections of the related system integration manual [2], [6], [10].

While selecting the antenna for LEXI cellular modules, consider the frequency range supported by each LEXI module, as illustrated in Figure 4.

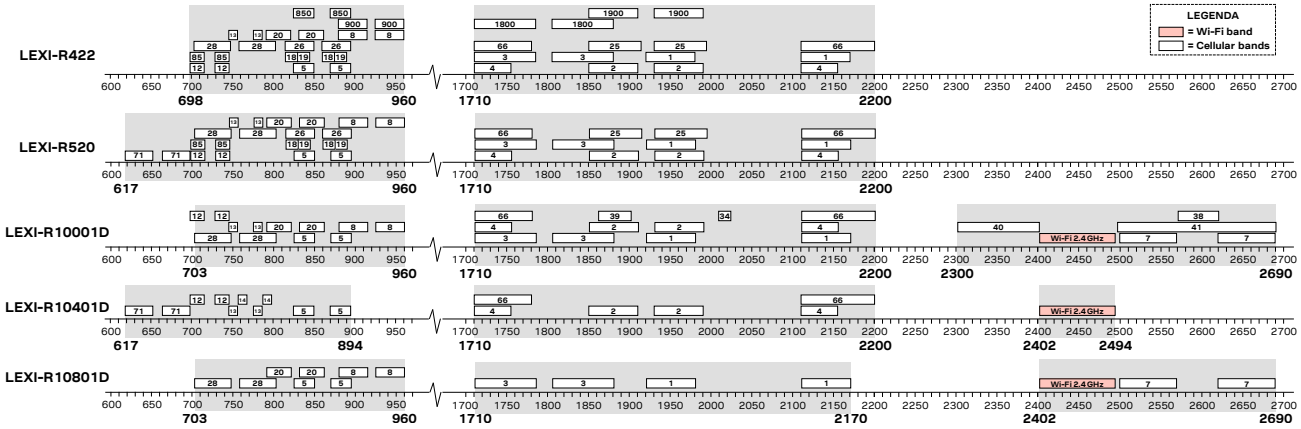

Figure 4: Summary of operating frequency bands supported by LEXI modules

Designers must consider the antenna from all perspectives at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the end-device integrating cellular modules with all the applicable required certification schemes depends on the antenna's radiating performance.

While implementing the cellular RF antenna design for LEXI modules, consider providing the best possible return loss in the frequency range supported by the modules, and place the antenna far from **VCC** supply line and related parts, as well as far from any possible source of interference and/or noise.

LEXI modules support the optional antenna dynamic tuning function, which may be useful to improve RF performances (antenna efficiency / return loss), in particular using embedded antenna integrated in a small end-device.

The RF coexistence with other radio systems operating simultaneously with the cellular RF system may be challenging when the modules are integrated in small devices, due to the limited capability in providing proper RF isolation in small end-devices. In the perspective of integrating an external GNSS receiver, consider the following regarding RF coexistence:

- LEXI-R10 series LTE Cat 1bis modules integrate a band-pass SAW filter along each LTE FDD RF path, improving the RF isolation with an external GNSS receiver by design.
- LEXI-R422 LTE-M / NB-IoT / 2G modules and LEXI-R520 LTE-M / NB-IoT modules do not integrate a band-pass SAW filter along cellular RF paths, meaning that an external GNSS stop-band SAW filter along the cellular RF line may be suitable to improve the RF isolation with an external GNSS receiver.

For additional design guidelines and examples, see the related integration manual [2], [6], [10].

The optional antenna detection circuit using the **ANT_DET** input is not implemented in Figure 2, as commonly not required for applications integrating LEXI modules.

LEXI-R10 series modules, differently from LEXI-R422 and LEXI-R520 modules, support the reception of Wi-Fi 2.4 GHz RF signals over the same **ANT** RF port available in time sharing with transmission and reception of LTE RF signals. The Wi-Fi subsystem inside LEXI-R10 series modules consists in a receiver radio circuitry only, providing the optional Wi-Fi scan function, with the aim of retrieving the information about Wi-Fi network in area, to determine device location. This optional and additional Wi-Fi scan function requires the support of the 2.4 GHz RF reception by the antenna in use.

3.5 GNSS RF interface

LEXI-R520 modules integrate the u-blox SpotNow A-GPS receiver connected to the **ANT_GNSS** RF input of the module. Figure 2 shows an application circuit example with an external GPS antenna connected to the **ANT_GNSS** RF input with an optional external LNA with supply controlled by the **ANT_ON** output of the module to optimize the power consumption.

There is no external SAW filter along the RF path as commonly not required, considering the u-blox SpotNow A-GPS receiver does not operate simultaneously with the LTE transmitter of the LEXI-R520 module, making the RF coexistence topic not applicable for the LEXI-R520 SpotNow use-case.

Similar to the cellular RF antenna design, the GNSS RF antenna design needs to be implemented providing the best possible return loss in the GPS frequency range supported by the modules and placing the GNSS RF parts as far as possible from any possible source of interference or noise.

LEXI-R422 and LEXI-R10 series modules do not include an **ANT_GNSS** RF input pin as they do not integrate any GNSS receiver.

3.6 System control interfaces

The **PWR_ON** / **PWR_CTRL** input line is designed to be driven by an open drain driver as illustrated in Figure 2. The assertion or toggling of the **PWR_ON** / **PWR_CTRL** input line can:

- Trigger the switch-on of LEXI modules when they are in power-off mode (switched off, but with a valid voltage present at the **VCC** module supply input).
- Trigger the wake-up of LEXI modules when they are in ultra-low power deep-sleep mode.
- Trigger the graceful switch-off of LEXI modules, in equivalent way of AT+CPWROFF command.

- Trigger the abrupt emergency reset / reboot of LEXI-R422 modules only.
- Trigger the abrupt emergency hardware shutdown of LEXI-R520 modules only.

The **RESET_N** input line is designed to be driven by open drain driver as illustrated in Figure 2 too. The assertion or toggling of the **RESET_N** input line causes different actions:

- the **RESET_N** line triggers an unconditional reboot of the module when toggled, without internal PMU shutdown when set low, in case of LEXI-R520 modules,
- the **RESET_N** line triggers an unconditional reboot of the module when toggled, with internal PMU shutdown when set low, in case of LEXI-R10 series modules.

LEXI-R422 modules do not provide a **RESET_N** pin, as the abrupt emergency reset / reboot function is available over the **PWR_CTRL** input line of this module.

The timings for proper control of the **PWR_ON** / **PWR_CTRL** and **RESET_N** lines may differ between the LEXI-R422, LEXI-R520 and LEXI-R10 series modules, and they are reported in the related data sheet of the modules [1], [5], [9].

3.7 SIM interface

LEXI modules are designed to work with the SIM interface circuit implemented in Figure 2, connecting the module to an external SIM card connector according to the design guidelines provided in related system integration manual [2], [6], [10]. Bypass capacitors with proper self-resonant frequency are recommended to be placed close to the SIM connector, as well as ESD protections, but these are not required using a SIM chip instead of a SIM card with related connector.

Selecting the SIM card / chip for the application, mind that

- LEXI-R422 modules support external 1.8 V type SIM card / chip only.
- LEXI-R520 and LEXI-R10 series modules support external 1.8 V and 3 V type SIM card / chip.

The optional SIM detection function is not implemented in Figure 2, as commonly not required for applications integrating LEXI modules.

3.8 UART interfaces

The application processor is connected to the LEXI modules over main UART interface in the simple schematic diagram illustrated in Figure 2.

The design is implemented with the UART interface configured at the same voltage level on both sides (application processor and LEXI module), without using voltage translators, as recommended to minimize any possible leakage and benefit from the extremely low current consumption of the u-blox LEXI modules, particularly in deep-sleep / power saving mode.

Thus, the UART voltage level of the application processor is recommended to be properly set at the **V_INT** level of the module (1.8 V nominal), for all the LEXI modules.

The **RXD** data output and **TXD** data input lines, supported by all the LEXI modules for AT and data communication, are directly connected with the application processors. These lines have external Test-Points made available as recommended for FW update access using u-blox EasyFlash tool, which can be executed only over these lines on the LEXI-R520 module.

The hardware flow control lines (**CTS** module output, and **RTS** module input) are directly connected with the application processors as recommended to make the communication robust and reliable, required if the multiplexer functionality is used in the application.

All the other UART lines are directly connected to the application processors, also considering that the **DTR**, **DSR**, **DCD** and **RI** pins can be alternatively configured, in mutually exclusive way, as second auxiliary UART interface on all the LEXI modules.

Mind that the **DTR** input must be set low to have URCs and/or the greeting text sent by the LEXI-R422 and LEXI-R520 modules.

The main primary UART interface provides the following functions on LEXI modules:

- LEXI-R422 modules:
  - AT commands and Data communication
  - Multiplexer protocol functionality
  - FW update by FOAT
- LEXI-R520 modules:
  - AT commands and Data communication
  - Multiplexer protocol functionality
  - FW update by FOAT
  - FW update by dedicated u-blox EasyFlash tool
- LEXI-R10 series modules:
  - AT commands and Data communication
  - Multiplexer protocol functionality
  - FW update by FOAT
  - FW update by dedicated u-blox EasyFlash tool

The auxiliary second UART interface provides the following functions on LEXI modules:

- LEXI-R422 modules:
  - AT commands and Data communication
  - GNSS data tunneling
  - FW update by FOAT
- LEXI-R520 modules:
  - AT commands and Data communication
  - GNSS data tunneling
  - FW update by FOAT
  - Diagnostic trace logging
- LEXI-R10 series modules:
  - AT commands and Data communication
  - FW update by FOAT
  - Diagnostic trace logging

Mind that, if low-power modes are enabled by AT commands, the whole UART interfaces, including the data lines, the hardware flow control lines and the **RI** pin, goes low when the module enters the ultra-low power deep-sleep mode, because related **V_INT** supply domain is powered down. This may happen very frequently, even in between every short DRX cycle, with the LEXI-R10 series modules. Hence, if low-power modes are enabled, we recommend:

- monitoring the UART break condition at the **RXD** data output line of the module or monitoring the **V_INT** output of the module, to determine when the ultra-low power deep sleep mode is entered
- configuring one always-on GPIO of LEXI-R10 series modules, such as **GPIO2** or **GPIO4**, with the module status indication function, to monitor if the module is switched off or in any other mode (deep sleep, active, or connected)
- configuring one always-on GPIO of LEXI-R10 series modules, such as **GPIO2** or **GPIO4**, with the Ring Indicator function, instead of using the **RI** pin, to avoid seeing spurious Ring Indicator events each time the module (frequently) enters the deep-sleep mode.

Mind that, before the switch-on / wake-up of the generic digital interface supply (**V_INT**), which is the supply rail of the UART interfaces aside other pins, no voltage driven by an external application should be applied to any generic digital interface of the LEXI-R422 and LEXI-R520 modules.

For additional specific design guidelines, see the UART sections in the related system integration manual [2], [6], [10].

3.9 USB interface

The USB interface is left unconnected in the simple schematic diagram example shown in Figure 2, providing Test-Points for diagnostic and/or FW update access as recommended.

The USB interface consists of the following USB lines on LEXI modules:

- LEXI-R422 modules provide the following USB lines:
  - **USB_5V0** input to enable the USB interface by applying an external voltage (5.0 V typical).
  - **USB_3V3** input to supply the USB interface by applying an external 3.3 V typical voltage.
  - **USB_D+** / **USB_D-** lines, carrying the USB data and signaling.
- LEXI-R520 modules provide the following USB lines:
  - **VUSB_DET** input to enable the USB interface by applying an external voltage (5.0 V typical).
  - **USB_D+** / **USB_D-** lines, carrying the USB data and signaling.
- LEXI-R10 series modules provide the following USB lines:
  - **USB_D+** / **USB_D-** lines, carrying the USB data and signaling.
  - **USB_BOOT** input pin to enable the FW update over the USB interface.

The USB interface provides the following functions on LEXI modules:

- LEXI-R422 modules:
  - FW update by dedicated u-blox EasyFlash tool.
  - Diagnostic trace logging.
- LEXI-R520 modules:
  - Diagnostic trace logging.
- LEXI-R10 series modules:
  - AT commands communication
  - Data communication
  - FW update by FOAT
  - FW update by dedicated u-blox EasyFlash tool
  - Diagnostic trace logging
  - Ethernet over USB

For additional specific design guidelines, see the USB sections in the related system integration manual [2], [6], [10].

3.10 I2C interface

The I2C interface is connected to an external u-blox M10 GNSS receiver in the simple schematic diagram shown in Figure 2. Voltage translators are included as the external u-blox M10 GNSS receiver operates at 3 V voltage level in this example.

The “00B” product version of LEXI-R10 series modules do not support the I2C interface, but the modules are HW-ready, and the support of the I2C interface is planned for future FW versions.

For additional specific design guidelines, see the I2C sections in the related system integration manual [2], [6], [10].

3.11 GPIO pins

Figure 2 also illustrate a typica use-case of the GPIOs pins of LEXI modules:

- the **GPIO1** controls an LED, to provide the network status indication.
- the **GPIO2** controls the supply of the external u-blox M10 GNSS receiver, implementing the GNSS supply enable function.
- the **GPIO3** is connected to the external u-blox M10 GNSS receiver, implementing the GNSS data ready function, waking-up the LEXI module in case the GNSS receiver has data to be sent.
- the **GPIO4**, which is an always-on GPIO of LEXI-R10 series modules, is connected to the application processor, implementing the module status indication function, indicating the operating status of the module (off vs. deep-sleep or other).
- the **GPIO5** is left unconnected, but it may be used for other purposes.
- the **GPIO6**, which is an always-on GPIO of LEXI-R10 series modules, is connected to the application processor, implementing the module wake-up and low power mode control function, allowing the external application processor to control the low power mode of the module, waking up the module from the deep-sleep, or other.

Note that all the GPIO pins of LEXI-R422 and LEXI-R50 modules are in the **V_INT** supply domain as the other generic digital interfaces (UART, I2C, etc.), while the GPIO pins of LEXI-R10 series modules are in two different supply domains:

- the **GPIO1**, **GPIO5**, **GPIO7**, **GPIO8**, **GPIO9** and **GPIO10** pins of LEXI-R10 series modules are in the **V_INT** supply domain as the other generic digital interfaces (UART interfaces, I2C interface, and antenna dynamic tuner interface), so that their function is not available when the module is in the ultra-low power deep-sleep mode, with the generic digital interface supply (**V_INT**) switched off,
- the **GPIO2**, **GPIO3**, **GPIO4** and **GPIO6** pins of LEXI-R10 series modules are in the “always-on” supply domain, so that their function is available also when the module is in the ultra-low power deep-sleep mode, with the generic digital interface supply (**V_INT**) switched off.

Other functions can be enabled on the GPIOs of the LEXI modules, as described in the related data sheet [1], [5], [9] and related AT commands manual [3], [7], [11].

3.12 Reserved pins

LEXI modules include pins reserved for future (**RSVD**) that are all intended to be unconnected, except:

- **RSVD** pin number **99** (**J5**) of LEXI-R422 modules, that is recommended to be externally accessible by connecting it to a dedicated Test-Point for diagnostic.

3.13 Test-Points

Table 2 lists the interfaces dedicated for FW update and/or diagnostic purposes on LEXI modules.

Module	FW update	Cellular diagnostic
LEXI-R422	USB, PWR_CTRL	USB, PWR_CTRL, V_INT, RSVD #99
LEXI-R520	UART, PWR_ON, V_INT	USB, RESET_N, V_INT or AUX UART, RESET_N, V_INT
LEXI-R10 series	USB, USB_BOOT, PWR_ON or UART, PWR_ON, V_INT	USB, RESET_N, V_INT or AUX UART, RESET_N, V_INT

Table 2: Interfaces for FW update and/or diagnostic purposes on LEXI modules

The schematic diagram illustrated in Figure 2 includes accessible test-points directly connected to the following pins, which are strongly recommended for FW update and diagnostic purposes:

- **V_INT**
- **PWR_ON/PWR_CTRL**
- **RESET_N**
- **TXD**
- **RXD**
- **VUSB_DET/USB_5V0**
- **USB_3V3**
- **USB_D+**
- **USB_D−**
- **USB_BOOT**
- **RSVD #99**

3.14 Other

All the GND pins are intended to be externally connected to ground, while other interfaces are not implemented or not used in the simple example of design as shown in Figure 2.

☞ For additional specific design guidelines, see the related system integration manual [2], [6], [10] of the u-blox LEXI modules.

Appendix

A Glossary

Abbreviation	Definition
2G	Second Generation cellular technology (GSM, GPRS, E-GPRS)
ADC	Analog to Digital Converter
A-GPS	Assisted Global Positioning System
Cat	Category
CTS	Clear To Send
DCD	Data Carrier Detect
DSR	Data Set Ready
DTR	Data Terminal Ready
eDRX	Extended Discontinuous Reception
ESD	Electro-Static Discharge
GND	Ground
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTE	Long-Term Evolution
MCU	Micro-Controller Unit
PA	Power Amplifier
PMU	Power Management Unit
PSM	Power Saving Mode
RAT	Radio Access Technology
RI	Ring Indicator
RTS	Request To Send
SCL	Serial Clock
SDA	Serial Data
SDIO	Secure Digital Input Output interface
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
TDMA	Time-Division Multiple-Access
TP	Test-Point
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Related documentation

[1] u-blox LEXI-R422 data sheet, UBX-22020834
[2] u-blox LEXI-R422 system integration manual, UBX-23007449
[3] u-blox LEXI-R422 / LEXI-R4 series AT commands Manual, UBX-17003787
[4] u-blox LEXI-R422 / LEXI-R42 series application development guide, UBX-20050829
[5] u-blox LEXI-R520 data sheet, UBX-22020070
[6] u-blox LEXI-R520 system integration manual, UBX-23008006
[7] u-blox LEXI-R520 / LEXI-R5 series AT commands manual, UBX-19047455
[8] u-blox LEXI-R520 / LEXI-R5 series application development guide, UBX-20033314
[9] u-blox LEXI-R10 series data sheet, UBX-23007594
[10] u-blox LEXI-R10 series system integration manual, UBX-23008149
[11] u-blox LEXI-R10 series AT commands manual, UBXDOC-686885345-1786
[12] u-blox LEXI-R10 series application development guide, UBXDOC-686885345-1983

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Revision history

Revision	Date	Name	Comments
R01	29-Mar-2024	sses	Initial release
R02	05-Jun-2024	sses	Clarified UART interfaces capabilities. Clarified Ring Indicator function availability. Minor other clarifications and corrections.
R03	06-Jun-2024	sses	Corrected DCD and DTR pin assignment in Table 1.
R04	02-Aug-2024	sses	Extended document applicability to LEXI-R10001D. Clarified LEXI-R10 voltage supply domain of the pins, UART interfaces capabilities and recommendations with ultra-low power deep-sleep modes enabled.

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