

# LEA-F9T-10B

**High accuracy timing module**  
**Professional grade**

Data sheet



## Abstract

This data sheet describes the LEA-F9T timing module with multi-band GNSS receiver and nanosecond-level timing accuracy. LEA-F9T meets the most stringent 5G timing requirements, is ideal for global deployment due to GPS, BeiDou, Galileo, and GLONASS reception, and is unaffected by ionospheric errors. The module provides differential timing mode for highly accurate local timing and built-in security for highest robustness against malicious attacks.

## Document information

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This document applies to the following products:

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LEA-F9T	LEA-F9T-10B-00	TIM 2.22	-	Mass production

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# 1 Functional description

## 1.1 Overview

LEA-F9T is a multi-band GNSS module offering 5 ns (1-sigma) timing accuracy with unparalleled low power consumption.

LEA-F9T incorporates the u-blox F9 multi-band platform in a small surface-mount device with a form factor of 22 x 17 mm.

## 1.2 Performance

Parameter	Specification	
Receiver type	Multi-band GNSS receiver for timing applications	
Accuracy of time pulse signal <sup>1 2</sup>	Absolute timing mode	5 ns
	Differential timing mode <sup>3</sup>	2.5 ns
Frequency of time pulse signal	0.25 Hz to 25 MHz (configurable)	
Time pulse jitter	±4 ns	
Time-mark resolution	8 ns	
Operational limits <sup>4</sup>	Dynamics	≤ 4 g
	Altitude	80,000 m
	Velocity	500 m/s
Velocity accuracy <sup>2 5</sup>	0.05 m/s	
Dynamic heading accuracy <sup>2 5</sup>	0.3 deg	

**Table 1: LEA-F9T specifications**

GNSS		GPS+GLO+GAL+BDS	GPS+BDS+GAL	GPS+GAL	GPS+GLO	GPS+BDS	GPS
Acquisition <sup>6</sup>	Cold start	24 s	25 s	29 s	26 s	28 s	29 s
	Hot start	2 s	2 s	2 s	2 s	2 s	2 s
	Aided start <sup>7</sup>	2 s	2 s	2 s	2 s	2 s	2 s
Max navigation update rate <sup>8</sup>		6 Hz	7 Hz	15 Hz	15 Hz	12 Hz	20 Hz

**Table 2: LEA-F9T performance in different GNSS modes**

<sup>1</sup> 1-sigma, fixed position mode, depends on temperature, atmospheric conditions, GNSS antenna, multipath conditions, satellite visibility and geometry

<sup>2</sup> Assumes typical performance of the navigation satellite systems.

<sup>3</sup> Depends on baseline length, demonstrated with 20 km baseline

<sup>4</sup> Assuming Airborne 4 g platform

<sup>5</sup> 50% at 30 m/s for dynamic operation

<sup>6</sup> Commanded starts. All satellites at -130 dBm. Measured at room temperature. Dual band operation.

<sup>7</sup> Dependent on the speed and latency of the aiding data connection, commanded starts

<sup>8</sup> 95% In PVT navigation mode, assumes secondary navigation output disabled (default)

GNSS		GPS+GLO+GAL+BDS	GPS+BDS+GAL	GPS+GAL	GPS+GLO	GPS+BDS	GPS
Horizontal position accuracy (CEP) <sup>2</sup>	Standalone <sup>9</sup>	1.5 m	1.5 m	1.5 m	1.5 m	1.5 m	1.5 m

**Table 3: LEA-F9T position accuracy in different GNSS modes**


To achieve the best absolute timing accuracy, measure the propagation delay of the entire signal path from the antenna to the receiver's time pulse output, and then compensate for this delay using the CFG-TP configuration items.

GNSS		GPS+GLO+GAL+BDS
Sensitivity <sup>10</sup>	Tracking and nav.	-167 dBm
	Reacquisition	-160 dBm
	Cold start	-148 dBm
	Hot start	-157 dBm

**Table 4: LEA-F9T sensitivity**

## 1.3 Supported GNSS constellations

The LEA-F9T GNSS module is a concurrent GNSS receiver that can receive and track multiple GNSS systems. Thanks to the multi-band RF front-end architecture, all major GNSS constellations (GPS, Galileo, GLONASS and BeiDou) as well as NavIC, SBAS, and QZSS satellites can be received concurrently. LEA-F9T can be configured to function as a L1, L2 or L1, L5 dual-band receiver. If low power consumption is a key factor, then the receiver can be configured for a subset of GNSS constellations.

LEA-F9T can receive the NavIC L5 satellite signals that share the same frequency with GPS L5 signals and can be configured to work on its own or in parallel with the other GNSS constellations.

The QZSS system shares the same frequency bands with GPS and can only be processed in conjunction with GPS.

To benefit from multi-band signal reception, dedicated hardware preparation must be made during the design-in phase. See the Integration manual [1] for u-blox design recommendations.

LEA-F9T supports the GNSS and their signals as shown in Table 5.<sup>11</sup>

GPS / QZSS	GLONASS	Galileo	BeiDou	NavIC
L1C/A (1575.420 MHz)	L1OF (1602 MHz + k*562.5 kHz, k = -7,...,6)	E1-B/C (1575.420 MHz)	B1I (1561.098 MHz) B1C (1575.420 MHz)	-
L2C (1227.600 MHz)	-	E5b (1207.140 MHz)	B2I (1207.140 MHz)	-
L5 (1176.450 MHz)	-	E5a (1176.450 MHz)	B2a (1176.450 MHz)	SPS-L5 (1176.450 MHz)

**Table 5: Supported GNSS signals on LEA-F9T**

LEA-F9T can use the u-blox AssistNow™ Online service which provides GNSS assistance information.

<sup>9</sup> Depends on atmospheric conditions, GNSS antenna, multipath conditions, satellite visibility, and geometry


<sup>10</sup> Demonstrated with a good external LNA. Measured at room temperature.

<sup>11</sup> Only L1, L2 or L1, L5 bands are supported concurrently

## 1.4 Supported GNSS augmentation systems


### 1.4.1 Quasi-Zenith Satellite System (QZSS)

The Quasi-Zenith Satellite System (QZSS) is a regional navigation satellite system that provides positioning services for the Pacific region covering Japan and Australia. LEA-F9T is able to receive and track QZSS signals concurrently with GPS signals, resulting in better availability especially under challenging signal conditions, e.g. in urban canyons.

 QZSS can be enabled only if the GPS operation is also configured.

### 1.4.2 Satellite-based augmentation system (SBAS)

LEA-F9T supports SBAS (including WAAS in the US, EGNOS in Europe, L1Sb (QZSS SBAS) in Japan and GAGAN in India) to deliver improved location accuracy within the regions covered. However, the additional inter-standard time calibration step used during SBAS reception results in degraded time accuracy overall.

 SBAS reception is disabled by default in LEA-F9T.

### 1.4.3 Differential timing mode

To improve timing accuracy locally, LEA-F9T can be used in differential timing mode, in which correction data is sent to neighboring LEA-F9T timing receivers via a communication network.

In differential timing mode LEA-F9T can operate either as a reference station generating the following RTCM 3.3 messages, or as a corrected station using the following RTCM 3.3 messages:

Message type	Description
RTCM 1005	Stationary RTK reference station ARP
RTCM 1077	GPS MSM7
RTCM 1087	GLONASS MSM7
RTCM 1097	Galileo MSM7
RTCM 1127	BeiDou MSM7
RTCM 1230	GLONASS code-phase biases
RTCM 4072.1	Additional reference station information (u-blox proprietary RTCM Message)

**Table 6: Supported RTCM 3.3 messages**

## 1.5 Broadcast navigation data and satellite signal measurements

LEA-F9T can output all the GNSS broadcast data upon reception from tracked satellites. This includes all the supported GNSS signals as well as the QZSS and SBAS augmentation services. The UBX-RXM-SFRBX message provides this information. For the UBX-RXM-SFRBX message specification, see the Interface description [2]. The receiver can provide satellite signal information in a form compatible with the Radio Resource LCS Protocol (RRLP) [4].

### 1.5.1 Carrier-phase measurements

The LEA-F9T modules provide raw carrier-phase data for all supported signals, along with pseudorange, Doppler and measurement quality information. The data contained in the UBX-RXM-RAWX message follows the conventions of a multi-GNSS RINEX 3 observation file. For the UBX-RXM-RAWX message specification, see Interface description [2].



Raw measurement data is available once the receiver has established data bit synchronization and time-of-week.

## 1.6 Supported protocols

LEA-F9T supports the following protocols:

Protocol	Type
UBX	Input/output, binary, u-blox proprietary
NMEA 4.11 (default), 4.10, 4.0, 2.3, and 2.1	Input/output, ASCII
RTCM 3.3	Input/output, binary

**Table 7: Supported protocols**

For specification of the protocols, see the Interface description [\[2\]](#).

## 2 System description

### 2.1 Block diagram

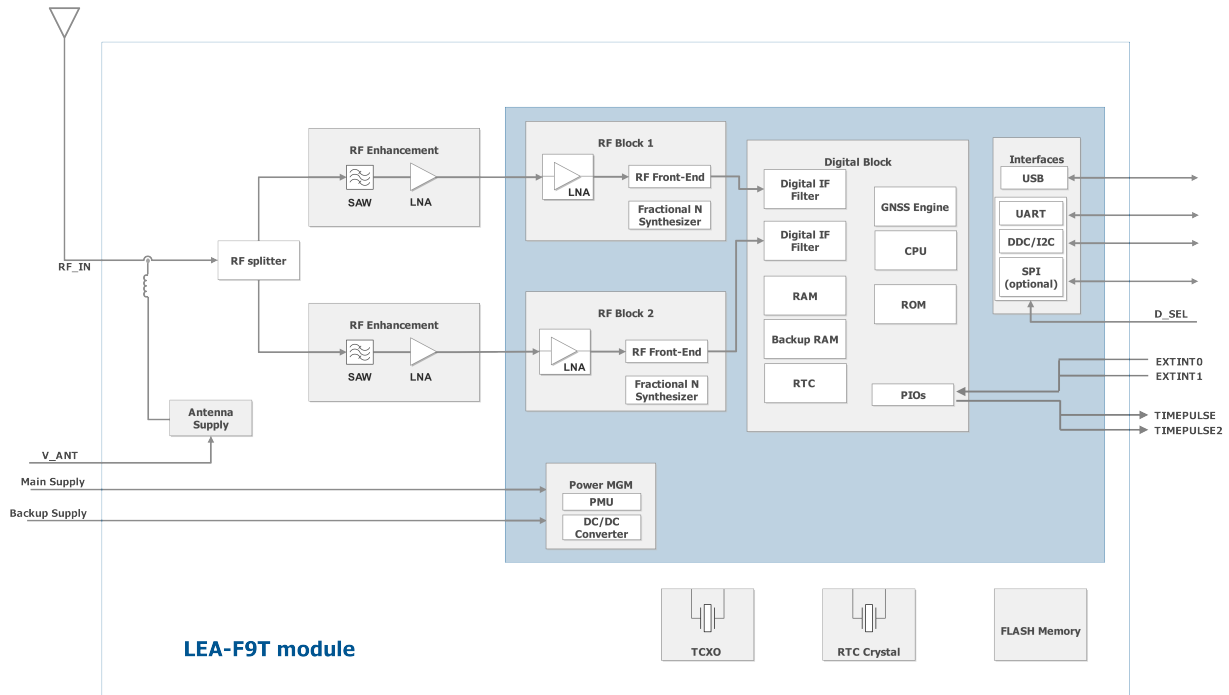


Figure 1: LEA-F9T block diagram



An active antenna is recommended for use with the LEA-F9T. For more information, see the Integration manual [1].



## 3 Pin definition

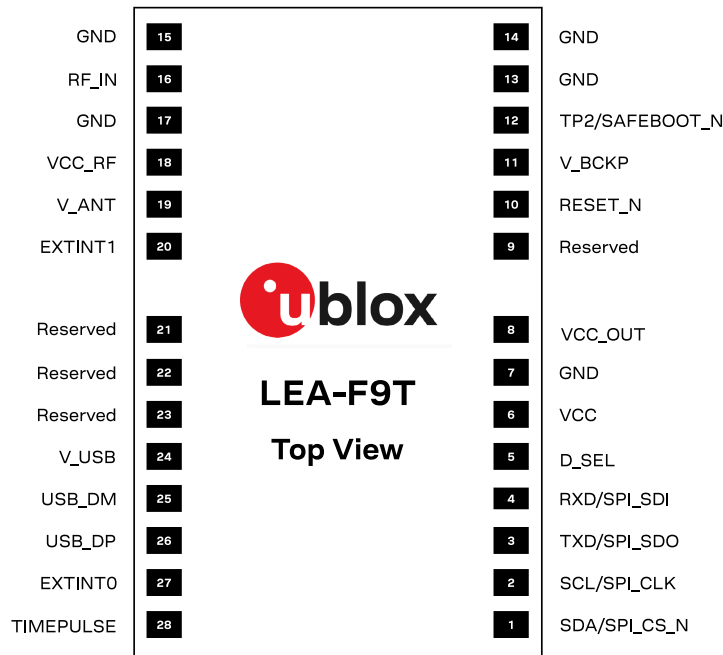
### 3.1 Pin assignment

The pin assignment of the LEA-F9T module is shown in [Figure 2](#). The defined configuration of the PIOs is listed in [Table 8](#).

For detailed information on pin functions and characteristics, see the LEA-F9T Integration manual [\[1\]](#).



The LEA-F9T is an LCC package with the I/O, power connections on the outside edge and central ground pads.



**Figure 2: LEA-F9T pin assignment**



Pin no.	Name	I/O	Description
1	SDA / SPI_CS_N	I/O	I2C data if D_SEL = 1 (or open) / SPI_CS_N if D_SEL = 0
2	SCL / SPI_CLK	I/O	I2C clock if D_SEL = 1 (or open). SPI Clock if D_SEL = 0
3	TXD / SPI_SDO	O	Host UART1 output if D_SEL = 1 (or open). SPI_SDO if D_SEL = 0
4	RXD / SPI_SDI	I	Host UART1 input if D_SEL = 1 (or open). SPI_SDI if D_SEL = 0
5	D_SEL	I	Interface select for pins 1-4
6	VCC	I	Voltage supply
7	GND	-	Ground
8	VCC_OUT	O	Output voltage. Leave open if not used.
9	Reserved	-	Reserved
10	RESET_N	I	RESET_N
11	V_BCKP	I	Backup supply voltage
12	SAFEBOOT_N/TP2	I/O	Time pulse 2 / SAFEBOOT_N (for future service, updates and reconfiguration)
13	GND	-	Ground
14	GND	-	Ground

Pin no.	Name	I/O	Description
15	GND	-	Ground
16	RF_IN	I	RF input
17	GND	-	Ground
18	VCC_RF	O	Voltage for external LNA
19	V_ANT	I	Active antenna voltage supply
20	EXTINT1	I	External interrupt pin 1
21	Reserved	-	Reserved
22	Reserved	-	Reserved
23	Reserved	-	Reserved
24	V_USB	I	USB supply
25	USB_DM	I/O	USB data
26	USB_DP	I/O	USB data
27	EXTINT0	I	External interrupt pin 0
28	TIMEPULSE 1	O	Time pulse 1

**Table 8: LEA-F9T pin assignment**

## 4 Electrical specifications


### 4.1 Absolute maximum ratings

-  CAUTION. Risk of device damage. Exceeding the absolute maximum ratings may affect the lifetime and reliability of the device or permanently damage it. Do not exceed the absolute maximum ratings.
-  This product is not protected against overvoltage or reversed voltages. Use appropriate protection to avoid device damage from voltage spikes exceeding the specified boundaries.

Parameter	Symbol	Condition	Min	Max	Units
Power supply voltage	VCC		-0.5	3.6	V
Voltage ramp on VCC <sup>12</sup>			20	8000	µs/V
Backup battery voltage	V_BCKP		-0.5	3.6	V
Voltage ramp on V_BCKP <sup>12</sup>			20		µs/V
Input pin voltage	Vin	VCC ≤ 3.1 V	-0.5	VCC + 0.5	V
		VCC > 3.1 V	-0.5	3.6	V
VCC_RF output current	ICC_RF			300	mA
Supply voltage USB	V_USB		-0.5	3.6	V
USB signals	USB_DM, USB_DP		-0.5	V_USB + 0.5	V
Input power at RF_IN	Prfin	source impedance = 50 Ω, continuous wave		10	dBm
Storage temperature	Tstg		-40	+105	°C

**Table 9: Absolute maximum ratings**

### 4.2 Operating conditions

-  Extreme operating temperatures can significantly impact the specified values. If an application operates near the min or max temperature limits, ensure the specified values are not exceeded.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Power supply voltage	VCC	2.7	3.0	3.6	V	
Supply voltage for USB interface	V_USB	3.0		3.6	V	
V_USB current	I_USB		2.0		mA	
Backup battery voltage	V_BCKP	1.65		3.6	V	
Backup battery current <sup>13, 14</sup>	I_BCKP		45		µA	V_BCKP = 3 V, VCC = 0 V
SW backup current <sup>14</sup>	I_SWBCKP		10		mA	
Input pin voltage range	Vin	0		VCC	V	
Digital IO pin low level input voltage	Vil			0.4	V	
Digital IO pin high level input voltage	Vih	0.8 * VCC			V	
Digital IO pin low level output voltage	Vol			0.4	V	Iol = 2 mA
TIMEPULSE						Iol = 4 mA

<sup>12</sup> Exceeding the ramp speed may permanently damage the device

<sup>13</sup> To measure the I\_BCKP, the receiver should first be switched on, i.e. VCC and V\_BCKP is available. Then set VCC to 0 V while the V\_BCKP remains available. Afterward, measure the current consumption at the V\_BCKP.

<sup>14</sup> The value has been characterized at 25 °C ambient temperature.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Digital IO pin high level output voltage TIMEPULSE	V <sub>oh</sub>	VCC – 0.4			V	I <sub>oh</sub> = 2 mA I <sub>oh</sub> = 4 mA
DC current through any digital I/O pin (except supplies)	I <sub>pin</sub>			5	mA	
Pull-up resistance for SCL, SDA	R <sub>pu</sub>	7	15	30	kΩ	
Pull-up resistance for D_SEL, RXD, TXD, SAFEBOOT_N, EXTINT	R <sub>pu</sub>	30	75	130	kΩ	
Pull-up resistance for RESET_N	R <sub>pu</sub>	7	10	13	kΩ	
VCC_RF voltage	VCC_RF		VCC – 0.1		V	
VCC_RF output current	ICC_RF			50	mA	
Receiver chain noise figure <sup>15</sup>	NF <sub>tot</sub>		4		dB	
External gain (at RF_IN) <sup>16</sup>	Ext_gain	6		30	dB	
Operating temperature	T <sub>opr</sub>	–40	+25	+105	°C	

**Table 10: Operating conditions**

## 4.3 Indicative power requirements

Table 11 provides examples of typical current requirements when using a cold start command. The given values are total system supply current for a possible application including RF and baseband sections.

All values in Table 11 have been measured at 25 °C ambient temperature.



The actual power requirements vary depending on the FW version used, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	GPS+GLO +GAL+BDS	GPS	Unit
I <sub>PEAK</sub>	Peak current	Acquisition	140	130	mA
I <sub>VCC</sub> <sup>17</sup>	VCC current	Acquisition	100	85	mA
I <sub>VCC</sub> <sup>17</sup>	VCC current	Tracking	95	78	mA

**Table 11: Currents to calculate the indicative power requirements**

<sup>15</sup> Only valid for GPS

<sup>16</sup> Overall gain from antenna feed

<sup>17</sup> Simulated GNSS signal

## 5 Communications interfaces

LEA-F9T has several communications interfaces, including UART, SPI, I2C and USB.

All the inputs have internal pull-up resistors in normal operation and can be left open if not used. All the PIOs are supplied by VCC, therefore all the voltage levels of the PIO pins are related to VCC supply voltage.

### 5.1 UART

LEA-F9T has one UART interface which supports configurable baud rates. See the integration manual [1].

Hardware flow control is not supported.

The UART is enabled if D\_SEL pin of the module is left open or "high".

Symbol	Parameter	Min	Max	Unit
$R_u$	Baud rate	9600	921600	bit/s
$\Delta_{Tx}$	Tx baud rate accuracy	-1%	+1%	-
$\Delta_{Rx}$	Rx baud rate tolerance	-2.5%	+2.5%	-

Table 12: LEA-F9T UART specifications

### 5.2 SPI

The SPI interface is disabled by default. The SPI interface shares pins with UART and I2C and can be selected by setting D\_SEL = 0. The SPI interface can be operated in peripheral mode only. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.

The SPI timing parameters for peripheral operation are defined in Figure 3. Default SPI configuration is CPOL = 0 and CPHA = 0.

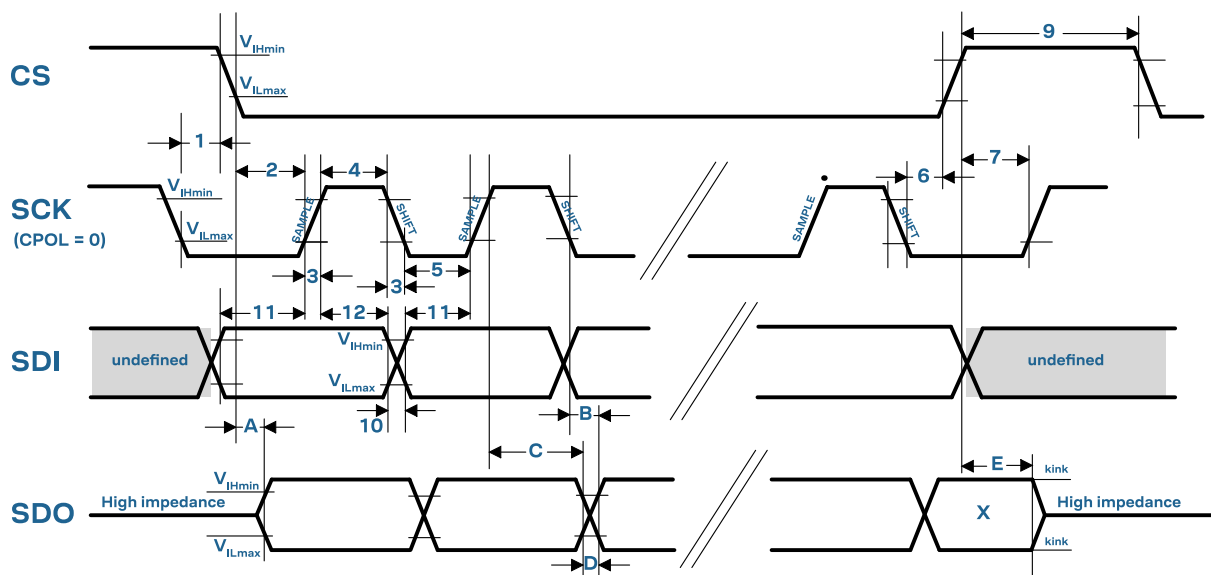


Figure 3: LEA-F9T SPI specification mode 1: CPHA=0 SCK = 5.33 MHz

Symbol	Parameter	Min	Max	Unit
1	CS deassertion hold time	23	-	ns

Symbol	Parameter	Min	Max	Unit
2	Chip select time (CS to SCK)	20	-	ns
3	SCK rise/fall time	-	7	ns
4	SCK high time	24	-	ns
5	SCK low time	24	-	ns
6	Chip deselect time (SCK falling to CS)	30	-	ns
7	Chip deselect time (CS to SCK)	30	-	ns
9	CS high time	32	-	ns
10	SDI transition time	-	7	ns
11	SDI setup time	16	-	ns
12	SDI hold time	24	-	ns

**Table 13: SPI peripheral input timing parameters 1 - 12**

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	12	40	ns
B	SDO data valid time (SCK), weak driver mode	15	40	ns
C	SDO data hold time	100	140	ns
D	SDO rise/fall time, weak driver mode	0	5	ns
E	SDO data disable lag time	15	35	ns

**Table 14: SPI peripheral timing parameters A - E, 2 pF load capacitance**

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	16	55	ns
B	SDO data valid time (SCK), weak driver mode	20	55	ns
C	SDO data hold time	100	150	ns
D	SDO rise/fall time, weak driver mode	3	20	ns
E	SDO data disable lag time	15	35	ns

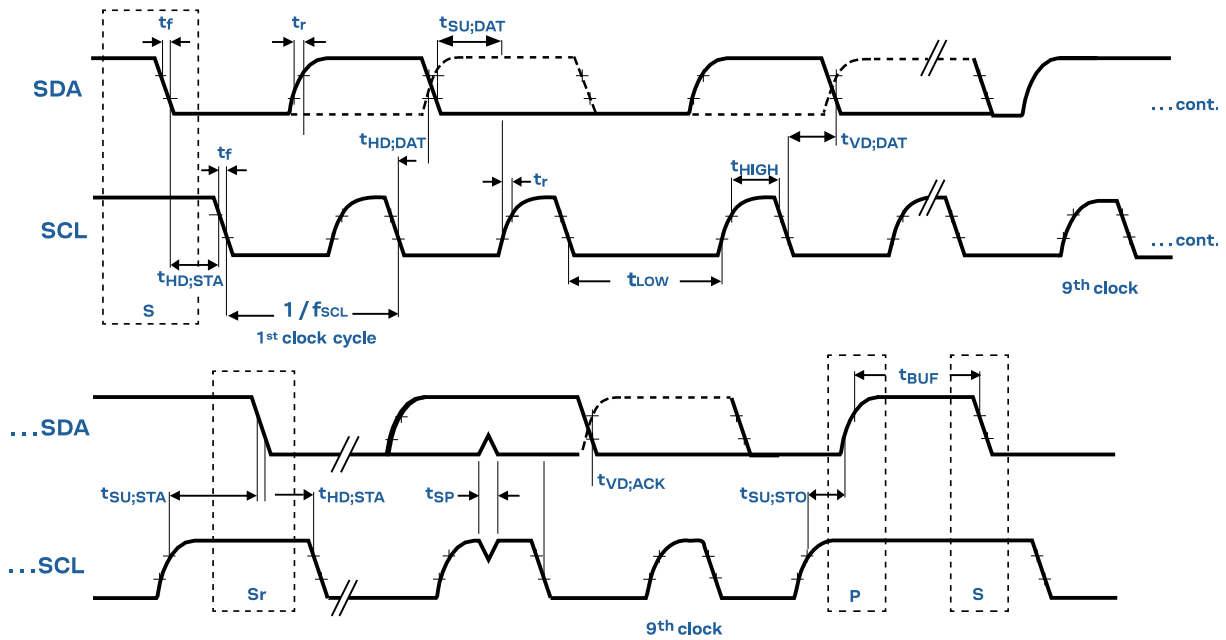
**Table 15: SPI peripheral timing parameters A - E, 20 pF load capacitance**

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	26	85	ns
B	SDO data valid time (SCK), weak driver mode	30	85	ns
C	SDO data hold time	110	160	ns
D	SDO rise/fall time, weak driver mode	13	45	ns
E	SDO data disable lag time	15	35	ns

**Table 16: SPI peripheral timing parameters A - E, 60 pF load capacitance**

## 5.3 I2C

An I2C interface is available for communication with an external host CPU in I2C Fast-mode. Backwards compatibility with Standard-mode I2C bus operation is not supported. The interface can be operated only in peripheral mode with a maximum bit rate of 400 kbit/s. The interface can make use of clock stretching by holding the SCL line LOW to pause a transaction. In this case, the bit transfer rate is reduced. The maximum clock stretching time is 20 ms.



$$V_{IL} = 0.3 V_{DD}$$

$$V_{IH} = 0.7 V_{DD}$$

Figure 4: LEA-F9T I2C peripheral specification

Symbol	Parameter	I2C Fast-mode		Unit
		Min	Max	
$f_{SCL}$	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	0.6	-	$\mu s$
$t_{LOW}$	Low period of the SCL clock	1.3	-	$\mu s$
$t_{HIGH}$	High period of the SCL clock	0.6	-	$\mu s$
$t_{SU;STA}$	Setup time for a repeated START condition	0.6	-	$\mu s$
$t_{HD;DAT}$	Data hold time	0 <sup>18</sup>	- <sup>19</sup>	$\mu s$
$t_{SU;DAT}$	Data setup time	100 <sup>20</sup>	-	ns
$t_r$	Rise time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
$t_f$	Fall time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6	-	$\mu s$
$t_{BUF}$	Bus-free time between a STOP and START condition	1.3	-	$\mu s$
$t_{VD;DAT}$	Data valid time	-	0.9 <sup>19</sup>	$\mu s$
$t_{VD;ACK}$	Data valid acknowledge time	-	0.9 <sup>19</sup>	$\mu s$
$V_{nL}$	Noise margin at the low level	0.1 VCC	-	V

<sup>18</sup> External device must provide a hold time of at least one transition time (max 300 ns) for the SDA signal (with respect to the min  $V_{ih}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

<sup>19</sup> The maximum  $t_{HD;DAT}$  must be less than the maximum  $t_{VD;DAT}$  or  $t_{VD;ACK}$  with a maximum of 0.9  $\mu s$  by a transition time. This maximum must only be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

<sup>20</sup> When the I2C peripheral is stretching the clock, the  $t_{SU;DAT}$  of the first bit of the next byte is 62.5 ns.

Symbol	Parameter	I2C Fast-mode		Unit
		Min	Max	
V <sub>nH</sub>	Noise margin at the high level	0.2 VCC	-	V

**Table 17: LEA-F9T I2C peripheral timings and specifications**


The I2C interface is only available with the UART default mode. If the SPI interface is selected by using D\_SEL = 0, the I2C interface is not available.

## 5.4 USB

The USB 2.0 FS (full speed, 12 Mbit/s) interface can be used for host communication. Due to the hardware implementation, it may not be possible to certify the USB interface. The V\_USB pin supplies the USB interface.

## 5.5 Default interface settings

Interface	Settings
UART1 output	115200 baud, 8 bits, no parity bit, 1 stop bit. NMEA protocol with <b>GGA</b> , <b>GLL</b> , <b>GSA</b> , <b>GSV</b> , <b>RMC</b> , <b>VTG</b> , <b>TXT</b> , <b>ZDA</b> messages are output by default. UBX and RTCM 3.3 protocols are enabled by default but no output messages are enabled by default.
UART1 input	115200 baud, 8 bits, no parity bit, 1 stop bit. UBX, NMEA and RTCM 3.3 input protocols are enabled by default.
USB	Default messages activated as in UART1. Input/output protocols available as in UART1.
I2C	Available for communication in the Fast-mode with an external host CPU in peripheral mode only. Default messages activated as in UART1. Input/output protocols available as in UART1. Maximum bit rate 400 kb/s.
SPI	Allow communication to a host CPU, operated in peripheral mode only. Default messages activated as in UART1. Input/output protocols available as in UART1. SPI is not available unless D_SEL pin is set to low (see section D_SEL interface in Integration manual [1]).

**Table 18: Default interface settings**


Refer to the applicable Interface description [2] for information about further settings.



By default, LEA-F9T outputs NMEA messages that include satellite data for all GNSS bands being received. This results in a high NMEA output load for each navigation period. Make sure the UART baud rate used is sufficient for the selected navigation rate and the number of GNSS signals being received.



## 6 Mechanical specifications

4:1

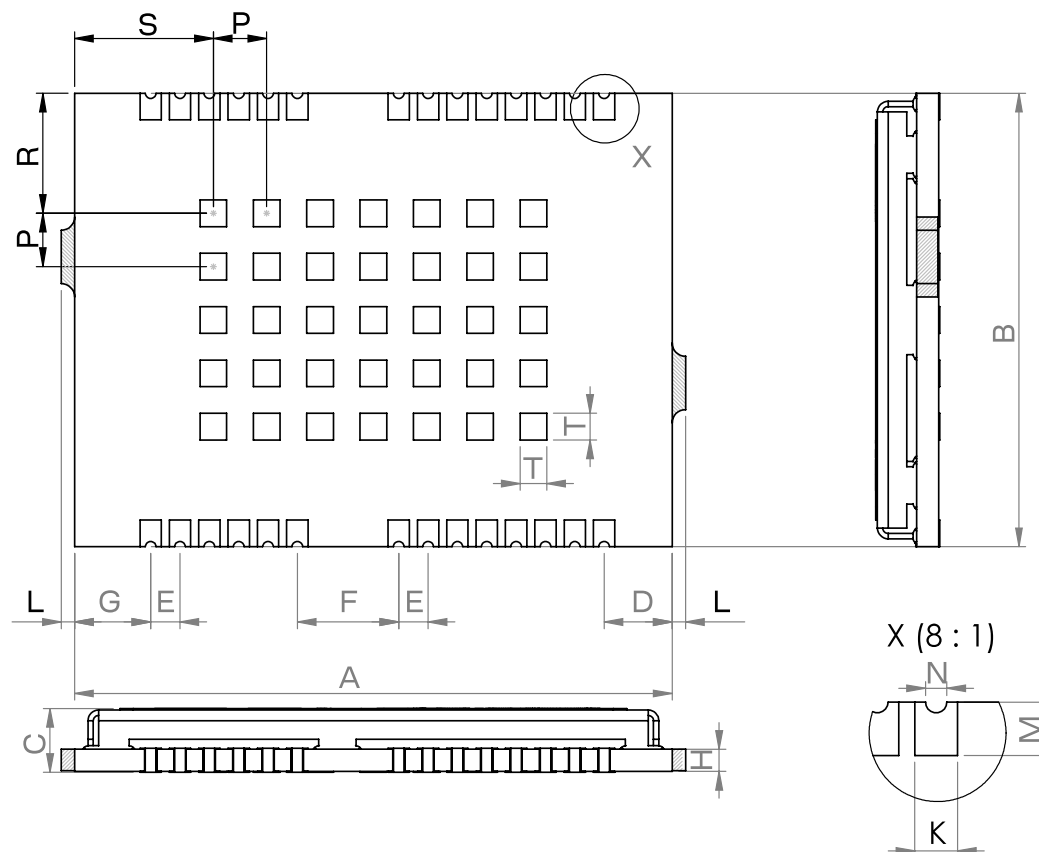


Figure 5: LEA-F9T mechanical drawing

Symbol	Min (mm)	Typical (mm)	Max (mm)
A	22.3	22.4	22.5
B	16.9	17.0	17.1
C	2.1	2.4	2.7
D	2.45	2.55	2.65
E	1.0	1.1	1.2
F	3.7	3.8	3.9
G	2.75	2.85	2.95
H		0.82	
K	0.7	0.8	0.9
M	0.9	1.0	1.1
N	0.4	0.5	0.6
P	1.95	2.0	2.05

Symbol	Min (mm)	Typical (mm)	Max (mm)
R	4.3	4.5	4.7
S	5.0	5.2	5.2
T	0.8	1.0	1.2
L			0.3
Weight		1.9 g	

**Table 19: LEA-F9T mechanical dimensions**



The mechanical picture of the de-paneling residual tabs (L) is an approximate representation. The shape and position may vary.



Take the size of the de-paneling residual tabs into account when designing the component keep-out area.

## 7 Qualifications and approvals

<b>Quality and reliability</b>	
Product qualification	Qualified according to u-blox qualification policy, based on a subset of AEC-Q104
Chip qualification	Modules are based on AEC-Q100 qualified GNSS chips
Manufacturing	Manufactured at ISO/TS 16949 certified sites
<b>Environmental</b>	
RoHS compliance	Yes
Moisture sensitivity level (MSL) <sup>21 22</sup>	3
<b>Type approvals</b>	
European RED certification (CE)	Declaration of Conformity (DoC) is available on the <a href="#">u-blox website</a> .
UK conformity assessment (UKCA)	Yes

**Table 20: Qualifications and approvals**

<sup>21</sup> For the MSL standard, see IPC/JEDEC J-STD-020 and J-STD-033, available on [www.jedec.org](http://www.jedec.org)

<sup>22</sup> For more information regarding moisture sensitivity levels, labelling, storage and drying, see the Product packaging reference guide [3]

## 8 Product marking and ordering information

This section provides information about product marking and ordering.

### 8.1 Product marking

The product marking provides information on LEA-F9T and its revision, as in [Figure 6](#). For a description of the product marking, see [Table 21](#).

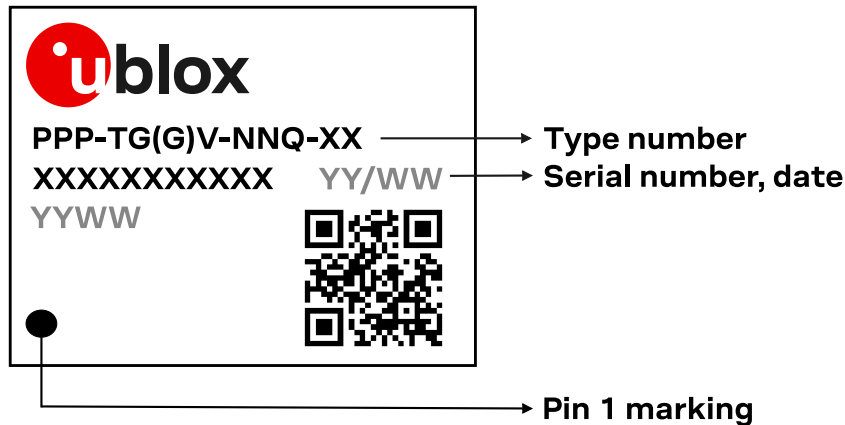


Figure 6: Example of LEA-F9T product marking

Code	Meaning	Example
PPP	Form factor	LEA
TG(G)	Platform	F9 = u-blox F9
V	Variant	T = Timing
NN	Major product version	00, 01, ..., 99
Q	Product grade	A = Automotive, B = Professional, C= Standard
XX	Revision	Hardware and firmware revisions
YY/WW or YYWW	Production date	Year/week, e.g. 24/04 or 2404
XXXXXXXXXXXX	Serial number	Alphanumeric characters, e.g. BN600001181
Other information	QR code	For internal/technical use

Table 21: Description of product marking

### 8.2 Product identifiers

The LEA-F9T label features three product identifiers: product name, ordering code, and type number. The product name identifies all u-blox products. It is used in documentation such as this Data sheet and is independent of packaging and product grade. The ordering code indicates the major product version and product grade, and the type number additionally specifies the hardware and firmware revisions.

[Table 22](#) describes the three different product identifiers used in the LEA-F9T label

Identifier	Format	Example
Product name	PPP-TG(G)V	LEA-F9T
Ordering code	PPP-TG(G)V-NNQ	LEA-F9T-10B
Type number	PPP-TG(G)V-NNQ-XX	LEA-F9T-10B-00

Table 22: Product identifiers

## 8.3 Ordering codes

Ordering code	Product	Remark
LEA-F9T-10B	u-blox LEA-F9T	

**Table 23: Product ordering codes**

u-blox provides information on product changes affecting the form factor, size or function of the product. For the Product change notifications (PCNs), see our website at <https://www.u-blox.com/en/product-resources>.

## Related documents

- [1] LEA-F9T Integration manual, [UBX-20032109](#)
- [2] TIM 2.22 Interface description [UBX-23004791](#)
- [3] Product packaging reference guide, [UBX-14001652](#)
- [4] Radio Resource LCS Protocol (RRLP), (3GPP TS 44.031 version 11.0.0 Release 11)



For regular updates to u-blox documentation and to receive product change notifications please register on our homepage <https://www.u-blox.com>.

## Revision history

Revision	Date	Status / comments
R01	12-Aug-2020	Objective specification
R02	27-Jan-2022	Advance information Typos plus FW ver. to TIM2.20, sec. 1.1: Nav. update change and footnote info., sec. 1.3: GPS, BeiDou, Galileo NavIC signals added, sec. 1.6: supported NMEA protocols added, sec. 3.1: package ground pad note added, sec. 4.1: Vcc/Vbckp ramp limits added, sec. 4.2: SW backup current change;NF change;Ext. gain change plus added footnote;Max operating temp. change, sec. 4.3: Vcc supply currents change, sec. 5.3: I2C max. clock stretching time added, sec. 5.5 ZDA message added to NMEA default o/p list.
R03	22-Feb-2022	Advance information sec. 4.2 minimum antenna gain reduced to 6dB
R04	14-Dec-2022	Advance information Firmware version to TIM2.21, concurrent B1I with B1C prohibition removed
R05	19-Jun-2023	Firmware version to TIM2.22 Updated product status to initial production Maximum navigation update rate changed Updated I2C and SPI timing specifications in section Communications interfaces Updated VCC_RF output current in table Absolute maximum ratings Updated backup current in table Operating conditions Added timepulse details in table Operating conditions
R06	19-Dec-2024	Updated product status to mass production Updated sections: <ul style="list-style-type: none"> <li>Added USB voltages and Pull-up resistance details in table Operating conditions</li> <li>Mechanical specifications with information on de-paneling residual tabs</li> <li>Qualifications and approvals</li> <li>Information on moisture sensitivity level has been moved from the Integration manual to chapter Qualifications and approvals</li> <li>Product labeling</li> </ul>

## Contact

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