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JODY-W3 series

Host-based modules with Wi-Fi 6 and Bluetooth 5.3

System integration manual

Abstract

This document describes the system integration of JODY-W3 series modules. These host-based modules support concurrent dual-band Wi-Fi 802.11n/ac/ax and Bluetooth® 5.3 and are designed for both simultaneous and independent operations. JODY-W3 modules include an integrated MAC/baseband processor and RF front-end components of automotive grade.

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This document applies to the following products:

Product name
JODY-W354-A
JODY-W374-A
JODY-W374
JODY-W377-A
JODY-W377

☞ For information about the related hardware, software, and status of listed product types, see the JODY-W3 series data sheet [1].

Contents

1 System description

1.1 Overview

JODY-W3 series modules provide complete short range transceiver solutions that can be easily integrated into automotive and industrial applications. The modules are intended for the most advanced in-car infotainment and connectivity systems and deliver the highest data rates in Wi-Fi using advanced Wi-Fi 6 802.11ax technology. JODY-W3 series modules operate in concurrent dual-bands, Wi-Fi 2.4 and 5 GHz, dual-MAC, and 2x2 MIMO. They also support Bluetooth 5.3 features, like extended advertising, long range, and 2 Mbit/s (PHY) data rate.

JODY-W3 series modules are provided in a surface-mount device (SMD) component packages based on the NXP AW690/88Q9098/88W9098 chipsets. The modules require a host processor running on a Linux or Android operating system and connect to the host processor through either PCIe or SDIO for Wi-Fi, high-speed UART for Bluetooth, and PCM/I2S for Bluetooth audio.

1.2 Module architecture

JODY-W3 series modules support Wi-Fi 6 802.11a/b/g/n/ac/ax and Bluetooth 5.3 operations:

- JODY-W354 and JODY-W374 provide two antenna ports, one for dual band Wi-Fi (2.4 GHz and 5 GHz) and one for 5 GHz Wi-Fi and Bluetooth.
- JODY-W377 provides three antenna ports, two for dual band Wi-Fi (2.4 GHz and 5 GHz) and one dedicated for Bluetooth.

Table 1 shows the available antenna and host interface configurations for JODY-W3 series modules.

<table>
<tr><th rowspan="2">Variant / Ordering code</th><th rowspan="2">LTE filter</th><th colspan="3">Antenna configuration</th><th colspan="2">Host interfaces</th></tr>
<tr><th>ANT0</th><th>ANT1</th><th>ANT2</th><th>Wi-Fi</th><th>Bluetooth</th></tr>
<tr><td>JODY-W354-00A</td><td>-</td><td rowspan="5">5 GHz Wi-Fi and Bluetooth</td><td rowspan="5">2.4 GHz and 5 GHz Wi-Fi</td><td rowspan="5">-</td><td rowspan="2">PCIe</td><td rowspan="2">UART</td></tr>
<tr><td>JODY-W354-20A</td><td>•</td></tr>
<tr><td>JODY-W374-00A</td><td>-</td><td rowspan="5">PCIe or SDIO</td><td rowspan="5">UART</td></tr>
<tr><td>JODY-W374-20A</td><td>•</td></tr>
<tr><td>JODY-W374-00B</td><td>-</td></tr>
<tr><td>JODY-W377-00A</td><td>-</td><td rowspan="2">2.4 GHz and 5 GHz Wi-Fi</td><td rowspan="2">2.4 GHz and 5 GHz Wi-Fi</td><td rowspan="2">Bluetooth</td></tr>
<tr><td>JODY-W377-00B</td><td>-</td></tr>
</table>

Table 1: Supported configurations of the JODY-W3 module series

☞ Some JODY-W3 series modules use a dedicated LTE coexistence band-pass filter in the 2.4 GHz Wi-Fi path. Module variants equipped with an LTE coexistence filter, as shown in Table 1, are recommended for designs with co-located LTE devices operating in bands 7, 38, 40, or 41.

1.2.1 Block diagrams

Figure 1 shows the block diagram for the JODY-W354 and JODY-W374 module variants.

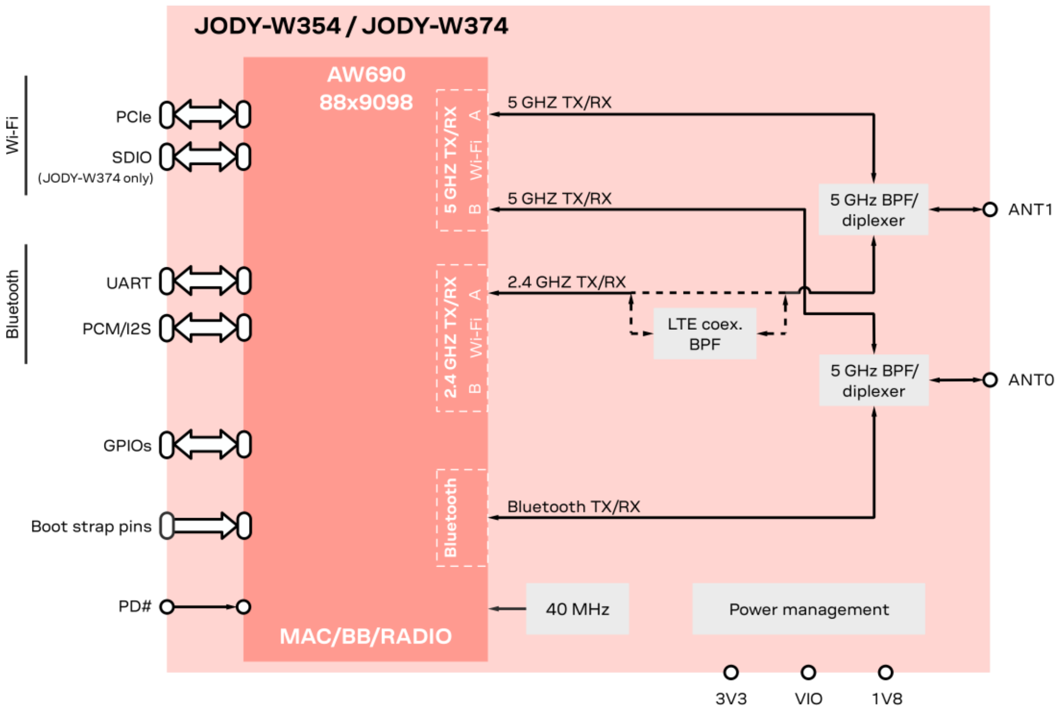

Figure 1: JODY-W354 and JODY-W374 block diagram

Figure 2 shows the block diagram for the JODY-W377 module variant.

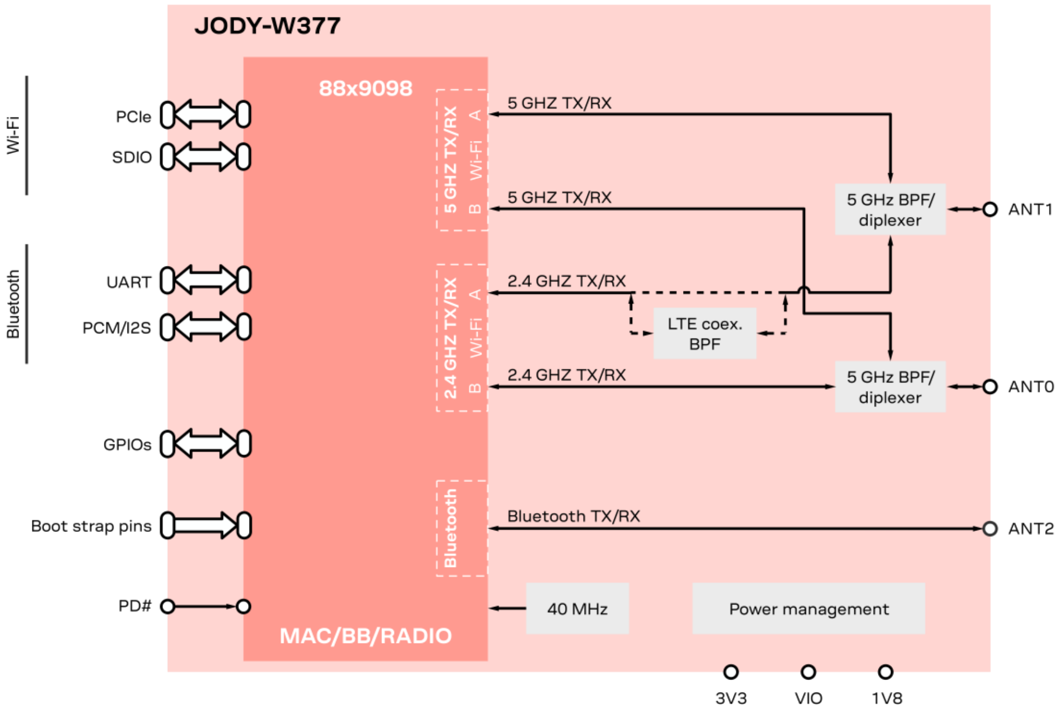

Figure 2: JODY-377 block diagram

1.3 Pin definition

1.3.1 Pin attributes

- **Function:** Pin function
- **Pin name:** Name of the package pin or terminal
- **Pin number:** Package pin numbers associated with each signal
- **Power:** Voltage domain that powers the pin
- **Type:** Signal type description:
    - I = Input
    - O = Output
    - I/O = Input and Output
    - D = Open drain
    - DS = Differential
    - PWR = Power
    - GND = Ground
    - PU = Internal Pull-Up
    - PD = Internal Pull-Down
    - H = High-impedance pin
    - RF = Radio interface
- **Description:** Pin description and notes, including alternate pin functions
- **Active:** Pin state in Active mode
- **Power down:** Pin state in Power Down mode

1.3.2 Pin assignment

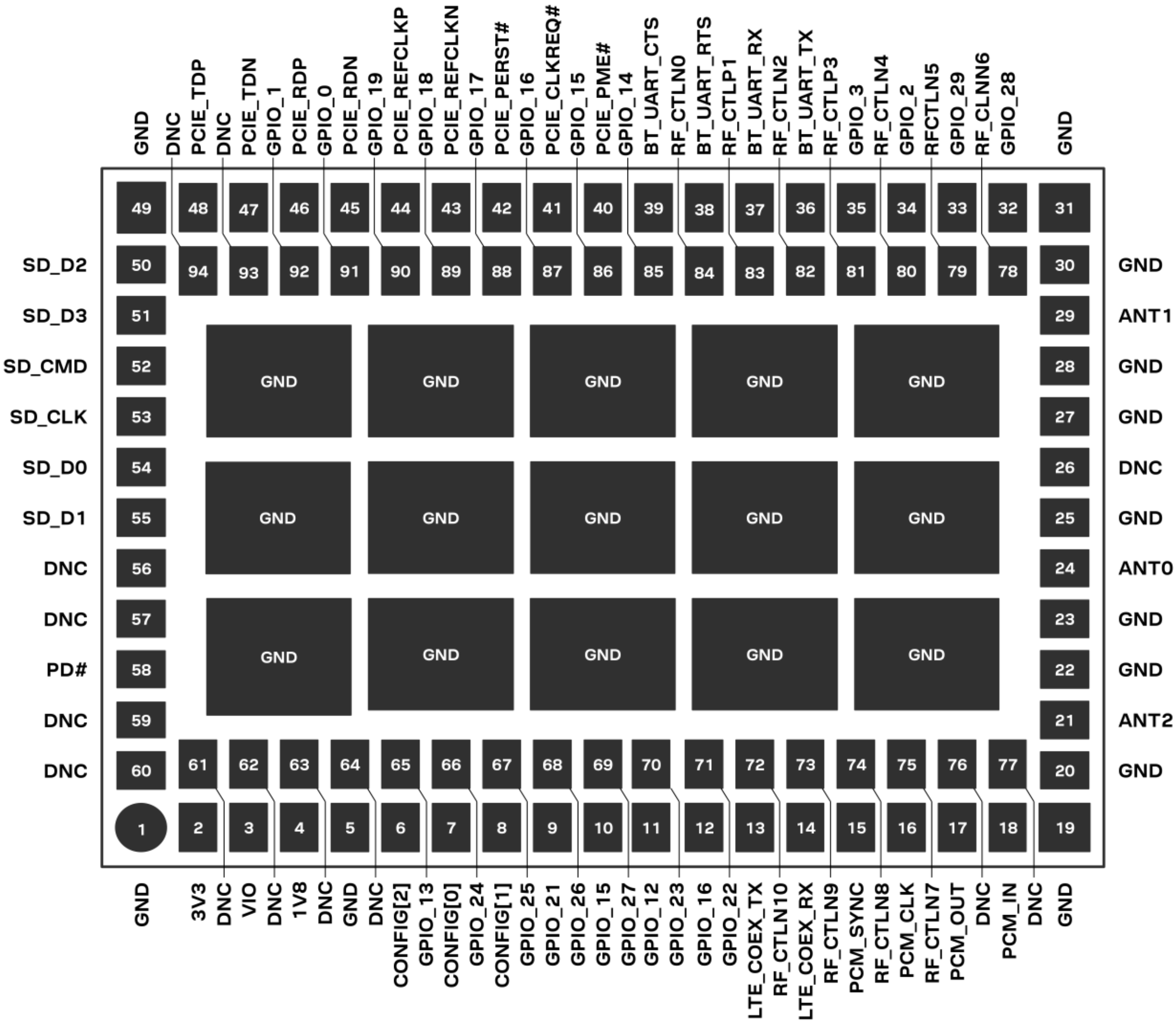

Figure 3: JODY-W3 series module pin assignments (top view)

1.3.3 Pin list

Function	Pin name	Pin no.	Power	Type	Description	Active	Power down
Power and ground	3V3	2		PWR	3.3 V power supply	PWR	-
	VIO	3		PWR	1.8 V or 3.3 V VIO supply	PWR	-
	1V8	4		PWR	1.8 V power supply	PWR	-
	GND	1, 5, 19, 20, 22, 23, 25, 27, 28, 30, 31, 49	GND	GND	Ground	GND	-
	Exposed pins	-	GND	GND	Connect to Ground	GND	-
SDIO host interface[1]	SD_CLK	53	1V8	I	SDIO clock input	I	Tristate
	SD_CMD	52	1V8	I/O	SDIO command line	I/O	Tristate
	SD_D0	54	1V8	I/O	SDIO data line bit [0]	I/O	Tristate

[1] SDIO pins not used on JODY-W354

Function	Pin name	Pin no.	Power	Type	Description	Active	Power down
	SD_D1	55	1V8	I/O	SDIO data line bit [1]	I/O	Tristate
	SD_D2	50	1V8	I/O	SDIO data line bit [2]	I/O	Tristate
	SD_D3	51	1V8	I/O	SDIO data line bit [3]	I/O	Tristate
Bluetooth host interface	BT_UART_TX	36	VIO	O	BT UART output signal. Connect to Host RX	O	Drive low
	BT_UART_RX	37	VIO	I	BT UART input signal. Connect to Host TX	I	Tristate
	BT_UART_RTS	38	VIO	O	BT UART request-to-send output signal. Connect to Host CTS	O	Drive high
	BT_UART_CTS	39	VIO	I	BT UART clear-to-send input signal. Connect to Host RTS	I	Tristate
Digital audio interface	PCM_SYNC	15	VIO	I/O	PCM frame sync. Input if slave, Output if master Alternate function: I2S Word Select	I/O	Tristate
	PCM_CLK	16	VIO	I/O	PCM clock Input if slave, Output if master Alternate function: I2S bit clock Configuration pin CON[10] See also Configuration pins.	I/O	Tristate
	PCM_IN	18	VIO	I	PCM data input Alternate function: I2S data in Configuration pin CON[8] See also Configuration pins.	I	Tristate
	PCM_OUT	17	VIO	O	PCM data output Alternate function: I2S data out Configuration pin CON[9] See also Configuration pins.	O	Tristate
GPIO interface	GPIO_21	9	VIO	I/O	GPIO[21]	I/O	Tristate
	WL_HOST_WAKE	10	VIO	I/O	Wi-Fi wake-up from Module / GPIO[15] Configuration pin CON[5] See also Configuration pins.	I/O	Tristate
	GPIO_12	11	VIO	I/O	GPIO[12] / UART_DSRn / W_DISABLE2n	I/O	Tristate
	BT_HOST_WAKE	12	VIO	I/O	BT wake-up from Module / GPIO[16] Configuration pin CON[6] See also Configuration pins.	I/O	Tristate
	GPIO_31	13	VIO	O	JTAG_TDO (output) / GPIO[31] LTE coexistence UART TX[2]	O	Tristate
	GPIO_30	14	VIO	I	JTAG_TDI (input) / GPIO[30] LTE coexistence UART RX[2]	I	Tristate
	GPIO_28	32	VIO	I/O	JTAG_TCK (input) / GPIO[28]	I/O	Tristate
	GPIO_29	33	VIO	I/O	JTAG_TMS (input) / GPIO[29]	I/O	Tristate
	GPIO_2	34	VIO	I/O	GPIO[2] / PTA external radio state signal (input)	I/O	Tristate
	GPIO_3	35	VIO	I/O	GPIO[3]	I/O	Tristate
	GPIO_14	85	VIO	I/O, PD	GPIO[14] Configuration pin CON[4] See also Configuration pins.	I/O	Tristate
	WL_HOST_WAKE	86	VIO	I/O	Wi-Fi wake-up from Module / GPIO[15] Configuration pin CON[5] See also Configuration pins.	I/O	Tristate

[2] LTE coexistence UART not supported in current firmware releases

Function	Pin name	Pin no.	Power	Type	Description	Active	Power down
					Same function as pin 10.		
	GPIO_13	65	VIO	I/O	GPIO[13] / UART_DTRn	I/O	Drive high
	GPIO_24	66	VIO	I/O	GPIO[24]	I/O	Tristate
	GPIO_25	67	VIO	I/O	GPIO[25]	I/O	Drive high
	GPIO_26	68	VIO	I/O	GPIO[26]	I/O	Tristate
	GPIO_27	69	VIO	I/O	GPIO[27]	I/O	Tristate
	GPIO_23	70	VIO	I/O	GPIO[23]	I/O	Drive low
	GPIO_22	71	VIO	I/O	GPIO[22]	I/O	Drive high
	BT_HOST_WAKE	87	VIO	I/O	Bluetooth wake-up from module / GPIO[16] Configuration pin CON[6] See also Configuration pins. Same function as pin 12.	I/O	Tristate
	GPIO_17	88	VIO	I/O	GPIO[17] / PTA external radio grant signal (output) Configuration pin CON[7] See also Configuration pins.	I/O	Tristate
	GPIO_18	89	VIO	I/O	GPIO[18] / Independent software reset for Wi-Fi subsystem (input) / PTA request from the external radio (input)	I/O	Tristate
	GPIO_19	90	VIO	I/O	GPIO[19] / Independent software reset for Bluetooth subsystem (input) / PTA external radio priority signal (input)	I/O	Tristate
	GPIO_0	91	VIO	I/O	GPIO[0]	I/O	Drive low
	GPIO_1	92	VIO	I/O	GPIO[1] / Independent software reset for Bluetooth subsystem (input) / PTA external radio priority signal (input)	I/O	Tristate
PCIe host interface	PCIE_PME#	40	VIO	I/O	PCIe wake signal (input/output, active low) Note: Pull-up required on host side	I/O	-
	PCIE_CLKREQ#	41	VIO	I/O	PCIe clock request (input/output, active low) Note: Pull-up required on host side	I	-
	PCIE_PERST#	42	VIO	I/O	PCIe host indication to reset the device (input, active low) Note: Muxed with GPIO[20]	I/O	Drive high
	PCIE_REFCLKN	43	1V8	I	PCIe negative differential clock input	I	-
	PCIE_REFCLKP	44	1V8	I	PCIe positive differential clock input	I	-
	PCIE_RDN	45	1V8	I	PCIe negative differential data input Note: place a 220nF coupling capacitor close to host CPU output.	I	-
	PCIE_RDP	46	1V8	I	PCIe positive differential data input Note: place a 220nF coupling capacitor close to host CPU output.	I	-
	PCIE_TDN	47	1V8	O	PCIe negative differential data output	O	-
	PCIE_TDP	48	1V8	O	PCIe positive differential data output	O	-
Host interface	CONFIG[0]	7	1V8	I	Host interface configuration pin See also Configuration pins.	I	Tristate

Function	Pin name	Pin no.	Power	Type	Description	Active	Power down
config-uration	CONFIG[1]	8	1V8	I	Host interface configuration pin See also Configuration pins.	I	Tristate
	CONFIG[2]	6	1V8	I	Host interface configuration pin See also Configuration pins.	I	Tristate
RF control[3]	RF_CNTL10_N	72	VIO	O	RF Control output low	O	Drive low
	RF_CNTL9_N	73	VIO	O	RF Control output high	O	Drive high
	RF_CNTL8_N	74	VIO	O	RF Control output low	O	Drive low
	RF_CNTL7_N	75	VIO	O	RF Control output high	O	Drive high
	RF_CNLT6_N	78	VIO	O	RF Control output low	O	Drive low
	RF_CNTL5_N	79	VIO	O	RF Control output high	O	Drive high
	RF_CNTL4_N	80	VIO	O	RF Control output low	O	Drive low
	RF_CNTL3_P	81	VIO	O	RF Control output high	O	Drive high
	RF_CNTL2_N	82	VIO	O	RF Control output low	O	Drive low
	RF_CNTL1_P	83	VIO	O	RF Control output high	O	Drive high
	RF_CNTL0_N	84	VIO	O	RF Control output low	O	Drive low
Clock / Power-down	PD#	58	1V8	I, PU	Full Power-down of the chipset (input, active low) (51 kΩ to 1V8) 0 = full power-down mode 1 = normal operation	I	Drive high through PU
Radio	ANT0	24		RF	Antenna signal 0 See also Antenna interfaces	RF	-
	ANT1	29		RF	Antenna signal 1 See also Antenna interfaces	RF	-
	ANT2	21		RF	Antenna signal 2 (JODY-W377) Not used (JODY-W354, JODY-W374) See also Antenna interfaces	RF	-
Other	DNC	26, 56, 57, 59, 60, 61, 62, 63, 64, 76, 77, 93, 94	-	-	Do not connect	-	-

Table 2: JODY-W3 series module pinout

1.4 Supply interfaces

1.4.1 Main supply inputs

JODY-W3 series modules are powered through the **3V3/VIO/1V8** pins. An integrated Buck converter supplied from the **1V8** generates the core voltage to the embedded systems ASIC. The **3V3** power rail is mainly used to supply the internal power amplifiers.

The current consumed through the **VIO** and **1V8,** and **3V3** pins by JODY-W3 series modules can vary by several orders of magnitude depending on the operation mode and state. Current consumption can change from the high current consumption during Wi-Fi transmission at maximum RF power level in connected-mode, to the low current consumption during low power idle-mode with the power saving configuration enabled.

For a detailed description on the supply voltage requirements, see the JODY-W3 series data sheet [1].

[3] Not implemented

Rail	Allowable ripple (peak to peak)[4] over DC supply	Current consumption, peak
3V3	30 $mV_{pk\text{-}pk}$	800 mA[5]
1V8	30 $mV_{pk\text{-}pk}$	1300 mA[5]
VIO	30 $mV_{pk\text{-}pk}$	5 mA[6]

Table 3: Summary of voltage supply requirements

1.4.2 Regulated DC power supply

JODY-W3 series modules must be powered by a regulated DC power supply, such as an LDO or SMPS. The appropriate type for your design depends on the main power source of the application.

SMPS is the ideal choice when the source of the main supply has a significantly higher voltage than that of the JODY-W3 series module. SMPS then provides the best power efficiency for your application and minimizes the current drawn from the main supply source. LDO is a better choice if the main supply voltage is close to the JODY-W3 series module supply voltages. Linear regulators are not recommended to step-down high voltages as these devices dissipate a considerable amount of energy.

⚠ When choosing SMPS, ensure that the AC ripple voltage at switching frequency does not violate the requirements specified in Table 3.

Regardless of the chosen DC power regulator, it is crucial that it can supply the high-peak current consumed by the module. When designing the module supply, a contingency of at least 20% over the stated peak current is recommended.

1.5 System function interfaces

1.5.1 Power-up sequence

PD# is ideally held low during start up and released when the power is stable, or later when the module must be turned on. **PD#** is powered by the **1V8** voltage domain and is connected by a 51 kΩ pull-up resistor to **1V8. PD#** follows the **1V8** supply if it is not actively driven by the host.

The power-up sequence of JODY-W3 with **VIO** set to 3.3 V is shown in Figure 4. In this configuration, enable **VIO** first, followed by other supplies shortly thereafter.

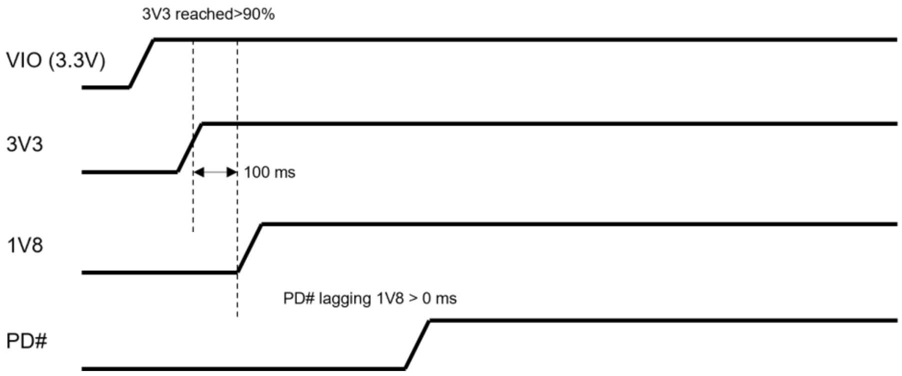

Figure 4: Power-up sequence of JODY-W3 module with VIO = 3.3 V

[4] Ripple measured on the power connectors of u-blox EVK.
[5] Peak current during concurrent dual band 2x2 operation.
[6] The current consumption for VIO depends on how GPIO's and other digital pins are used and could significantly exceed the number stated here for specific customizations.

The power up sequence for JODY-W3 with **VIO** set to 1.8 V is shown in Figure 5. In this configuration, the start-up sequence must start with **3V3** followed by **VIO** and **1V8**.

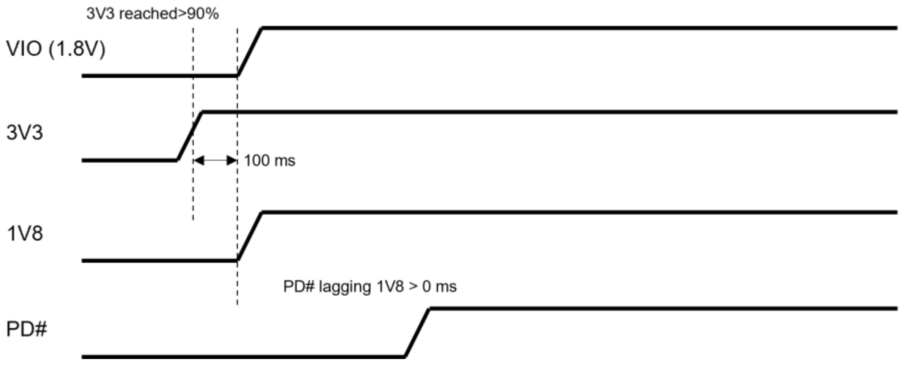

Figure 5. Power-up sequence of JODY-W3 module with VIO=1.8 V

☞ Power down mode can only be entered through **PD#** assertion by the host. **PD#** must be asserted for a minimum of 100 ms.

1.5.2 Reset

Although external reset is not a prerequisite for correct operation, it can be asserted by the host controller through **PD#** in the event of any abnormal module behavior. The **PD#** pin may be connected to a reset signal from the host.

JODY-W3 series modules are reset to a default operating state by any of the following events:

- Power on: Module is powered on and internal voltages are good
- **PD#** assert: The device is reset when the **PD#** input pin is <0.2 V and transitions from low to high

☞ A firmware download to the module is required after each reset. For information describing how to download the firmware, see also Software.

1.5.3 Power-off sequence

JODY-W3 modules enter Power Down mode when **PD#** is asserted. After assertion when **PD#** has reached below 0.2 V, the power on **3V3/VIO/1V8** supplies can be removed and the module enters the Power Off mode. **3V3/VIO/1V8** can be switched low simultaneously or with **1V8** leading **3V3**. The timing of **VIO** does not care.

1.5.4 Wake-up signals

JODY-W3 series modules provides module-to-host wake-up signals, used to exit the host from any sleep mode over Wi-Fi or Bluetooth. Wake-up signals are powered by the **VIO** voltage domain.

Name	I/O	Description
WL_HOST_WAKE	I/O	Wi-Fi Module-to-host wake-up signal (output) / GPIO[15] Used as configuration pin, see also Configuration pins.
BT_HOST_WAKE	I/O	Bluetooth Module-to-host wake-up signal (output) / GPIO[16] Used as configuration pin, see also Configuration pins.

Table 4: Wake-up signal definitions

1.5.5 Configuration pins

JODY-W3 series modules support configuration pins to set specific parameters following a reset. The definition and function of these configuration pins changes immediately (approx. 1 ms) to their initial function after reset, as described in the pin definitions, Table 2.

The interface combinations associated with each boot option are as follows:

- **PCIE-UART mode:** Commands and data for the Wi-Fi traffic are transferred through the PCIe bus to the module. The Bluetooth traffic uses the high-speed UART interface.
- **SDIO-UART mode:** Commands and data for the Wi-Fi traffic is transferred through the SDIO bus to the module. The Bluetooth traffic uses the high-speed UART interface.

During boot-up, configuration pins CON[4:10] must be set according to the settings described in Table 5. No external circuitry is required to set the configuration and these pins can consequently be left unconnected (NC). If these pins are connected, make sure that signals CON[5:10] are not pulled low and that CON[4] is not pulled high by any external circuitry during boot-up. After boot, CON[4..10] revert to their main function.

Configuration bits	Pin name	Pin number	Configuration settings	Internal PU/PD
CON[10]	PCM_CLK	16	1	Weak PU
CON[9]	PCM_OUT	17	1	Weak PU
CON[8]	PCM_IN	18	1	Weak PU
CON[7]	GPIO_17	88	1	Weak PU
CON[6]	BT_HOST_WAKE	12, 87	1	Weak PU
CON[5]	WL_HOST_WAKE	10, 86	1	Weak PU
CON[4]	GPIO_14	85	0	A 51 kΩ resistor to GND is attached on the module. No external resistor required. Do not pull high during boot-up.

Table 5: Configuration pins

Configuration pins CON[2:0] are used to set the firmware boot options that subsequently select the interfaces used for the Wi-Fi and Bluetooth traffic. With reference to Table 6, CON[2:0] must be strapped to GND through a 51 kΩ pull-down resistor to set a configuration bit to "0". To set a configuration bit to "1" the pin should not be connected.

Configuration bits	Pin name	Pin number	Strap values	Wi-Fi	Bluetooth
CON[2:0]	CONFIG[2:0]	CONFIG[2]: 6 CONFIG[1]: 8 CONFIG[0]: 7	000[7]	SDIO	UART
			011	PCIe	UART
			others	reserved	reserved

Table 6: Firmware boot options

[7] SDIO interface is not supported on JODY-W354

1.5.6 Power states

JODY-W3 series modules have several operation states. The power states and general guidelines for Wi-Fi and Bluetooth operations are defined in Table 7.

General status	Power state	Description
Power-down	Not Powered	**3V3**, **VIO,** and **1V8** supplies not present or below the operating range: module is switched off.
	Power Down	Asserting **PD#** while **3V3**, **VIO**, and **1V8** supplies are present powers down the module. This represents the lowest power condition with active voltage rails. All internal clocks are shutdown, and the register and memory states are not maintained. On exiting power down mode, the module is automatically reset, and the firmware must be downloaded again to re-enter any of the normal operation modes.
Normal operation	Active	Enables TX/RX data connection with the system running at the specified power consumption.
	Deep sleep	Used in power save modes.

Table 7: Description for Wi-Fi power states

1.6 Data communication interfaces

JODY-W3 series modules support PCI express v2.0, SDIO 3.0 and high-speed UART host interfaces. This means that all Wi-Fi traffic is communicated through either PCIe or SDIO by setting the appropriate boot option. The high-speed UART interface between the host and the JODY-W3 series module is used for the Bluetooth traffic. For information about the available host interface configuration options, see also Configuration pins.

1.6.1 SDIO 3.0 interface

JODY-W3 series modules include an SDIO device interface that is compatible with the industry-standard SDIO 3.0 specification (UHS-I, up to 104 Mbyte/s). The host controller uses the SDIO bus protocol to access the Wi-Fi functions. The interface supports 4-bit and 1-bit SDIO transfer modes at the full clock range up to 208 MHz. The modules also support legacy modes like Default Speed (DS) and High-Speed (HS) modes.

☞ The SDIO signal voltage is fixed to 1.8 V for Default Speed and High-Speed modes.

JODY-W3 modules act as devices on the SDIO bus. Table 8 summarizes the supported bus speed modes.

Bus speed mode	Max. bus apeed [MB/s]	Max. clock frequency [MHz]	Signal voltage [V]
SDR104	104	208	1.8
SDR50	50	100	1.8
DDR50	50	50	1.8
SDR25	25	50	1.8
SDR12	12.5	25	1.8
HS: High-Speed	25	50	1.8
DS: Default Speed	12.5	25	1.8

Table 8: SDIO bus speeds

Pull-up resistors are required for all SDIO data and command lines. These pull-up resistors can be provided either externally on the host PCB or internally in the host application processor. Depending on the routing of the SDIO lines on the host, it might be necessary to connect in-series termination resistors to these lines. See also Data communication interfaces.

Name	I/O	Description	Remarks
SD_CLK	I	SDIO Clock input	
SD_CMD	I/O	SDIO Command line	External PU required
SD_D0	I/O	SDIO Data line bit [0]	External PU required
SD_D1	I/O	SDIO Data line bit [1]	External PU required
SD_D2	I/O	SDIO Data line bit [2]	External PU required
SD_D3	I/O	SDIO Data line bit [3]	External PU required

Table 9: SDIO signal definitions

SDIO interface pins are powered by the **1V8** voltage domain.

1.6.2 PCIe interface

A PCIe v2.0 interface (Gen 2, single lane) is supported in the Wi-Fi section of the chipset. The interface supports link speeds of 2.5 and 5 Gbps.

When implementing the PCIe interface, consider the following:

- **PCIE_PERST#** must be set low during power up and released once the reference clock is stable.
- **PCIE_PERST#** has an internal pull-down resistor. If you choose to include a pull-up resistor, a value of 2 kΩ is recommended.

Table 10 shows the description of the chipset pins. The interface data pins are powered from the **1V8** voltage supply, and the interface GPIOs are powered from **VIO**.

Name	I/O	Description	Power supply
PCIE_PERST#	I	PCIe host indication to reset the device. Active low. Multiplexed with GPIO[20].	VIO
PCIE_CLKREQ#	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required. Active low. An external pull-up resistor on host side is required.	VIO
PCIE_PME#	OD	PCI wake signal. Active low. An external pull-up resistor on host side is required.	VIO
PCIE_RDN	I	PCIe receiver differential pair. 220 nF AC coupling capacitors should be placed close to the host TDN/TDP outputs.	1V8
PCIE_RDP	I		
PCIE_TDN	O	PCIe transmitter differential pair. 220 nF AC coupling capacitors are included on the module.	1V8
PCIE_TDP	O		
PCIE_REFCLKN	I	PCIe 100 MHz differential clock inputs. HCSL voltage levels.	1V8
PCIE_REFCLKP	I		

Table 10: PCIe signal descriptions

1.6.3 High-speed UART interface

JODY-W3 series modules support a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface in compliance with the industry standard 16550 specification. The main features of the UART interface include:

- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit and receive operations
- Two flow control pins (**RTS**/**CTS**)
- Interrupt triggers for low-power, high-throughput operation
- Supports standard baud rates and high throughput up to 4 Mbps.

The UART interface operation includes:

- Bluetooth firmware upload to the module
- Bluetooth data

Name	I/O	Description	Remarks
BT_UART_TX	O	UART TX signal	Connect to Host RX
BT_UART_RX	I	UART RX signal	Connect to Host TX
BT_UART_RTS	O	UART RTS signal	Connect to Host CTS
BT_UART_CTS	I	UART CTS signal	Connect to Host RTS

Table 11: UART signal description

High-Speed UART signals are powered by the **VIO** voltage domain.

1.6.4 PCM/I2S - Audio interface

JODY-W3 series modules support a bi-directional 4-wire PCM digital audio interface for digital audio communication with external digital audio devices like an audio codec.

The PCM interface supports:

- Master and slave mode
- PCM bit width size of 8 bit or 16 bit
- Up to four slots with configurable bit width and start positions
- Short frame and long frame synchronization

☞ PCM pins are shared with the I2S interface and can be configured to I2S mode using HCI commands.

Name	I/O	Description	Remarks
PCM_CLK	I/O	PCM clock Alternate function: I2S clock	Master output. Slave input. Used as configuration pin. See also Configuration pins.
PCM_SYNC	I/O	PCM frame sync Alternate function: I2S word select	Master output. Slave input.
PCM_IN	I	PCM data in Alternate function: I2S data in	Used as configuration pin. See also Configuration pins.
PCM_OUT	O	PCM data out Alternate function: I2S data out	Used as configuration pin. See also Configuration pins.

Table 12: PCM digital audio signal descriptions

PCM/I2S signals are powered by the **VIO** voltage domain.

1.7 Coexistence interfaces

1.7.1 PTA

Pin name	Pin number	Function	Pin type	Description
GPIO_2	34	EXT_STATE	I	External radio state input signal External radio traffic direction (Tx/Rx): • 1: TX • 0: RX
GPIO_17	88	EXT_GNT	O	External radio grant output signal
GPIO_1	92	EXT_FREQ	I	External radio frequency input signal Frequency overlap between external radio and Wi-Fi: • 1: overlap • 0: non-overlap This signal is useful when the external radio is a frequency hopping device.
GPIO_19	90	EXT_PRI	I	External radio priority input signal Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2 bit priority (sample twice). Can also have TX/RX info following the priority info if EXT_STATE is not used.
GPIO_18	89	EXT_REQ	I	Request from the external radio

Table 13: PTA coexistence interface

1.7.2 WCI-2

Pin name	Pin number	Function	Pin type	Description
GPIO_31	13	WCI2_SOUT	0	WCI-2 output signal
GPIO_30	14	WCI2_SIN	I	WCI-2 input signal

Table 14: WCI-2 coexistence interface

1.8 Antenna interfaces

1.8.1 Wi-Fi and Bluetooth antennas

JODY-W3 module series support different antenna configurations.

- JODY-W354 and JODY-W374 have two antenna pins: **ANT0** for Wi-Fi 5 GHz and Bluetooth, and **ANT1** for dual-band Wi-Fi connectivity.
- JODY-W377 has three antenna pins: **ANT0 and ANT1** for dual-band Wi-Fi, and **ANT2** for Bluetooth.

Follow these recommendations when developing an antenna interface for JODY-W3 modules:

- To minimize the effort on the certification process, consider integrating the u-blox antenna reference design in the end product.
- The JODY-W3 **ANT** pins have a nominal characteristic impedance of 50 Ω and must be connected to the external antennas through a 50 Ω transmission line. This is necessary to ensure good RF transmission and reception performance.
- Good isolation must be provided between the various antennas in the system. It is important to maximize the isolation between antennas operating in the same or adjacent bands. See also the Antenna Integration application note [11].

For instructions on how to design circuits that comply with these requirements, see also Antenna interfaces.

1.8.2 Approved antenna designs

JODY-W3 modules come with a pre-certified antenna design that can be used to save cost and time during the certification process. To leverage this benefit, customers are required to implement an antenna layout that is fully compliant with the u-blox reference design outlined in the JODY-W3 antenna reference design application note [22]. Reference design source files are available from u-blox on request.

For Bluetooth and Wi-Fi operation, JODY-W3 modules have been tested and approved for use with the antennas featured in the list of Approved antennas.

u-blox modules may also be integrated with other antennas. In which case, OEM installers must certify their own designs with the respective regulatory agencies.

1.9 Other remarks

1.9.1 Unused pins

JODY-W3 series modules have unconnected (NC) pins that are reserved for future use. These pins must be left unconnected on the application board.

1.9.2 GPIO usage

GPIOs are used to connect the JODY-W3 series module to various external devices. Table 15 shows the typical assignments for some of the GPIO pins. Other GPIO signals shown in Table 2 have not yet been assigned by the chip manufacturer. The exact function of these signals is normally dependent on the firmware releases.

GPIO	Module pin	Function
GPIO[15]	WL_HOST_WAKE	Wi-Fi to host wake-up signal. Used as configuration pin. See also Configuration pins
GPIO[16]	BT_HOST_WAKE	Bluetooth to host wake-up signal. Used as configuration pin. See also Configuration pins
GPIO[18]	GPIO_18	Wi-Fi independent reset
GPIO[19]	GPIO_19	Bluetooth independent reset
GPIO[0]	GPIO_0	Indicates the sleep mode of the module. Put to test point for debug purpose.

Table 15: Assigned GPIO functions

☞ Some GPIOs are used as configuration pins during boot-up. See also Configuration pins.

2 Design-in

Follow the design guidelines stated in this chapter to optimize the integration of JODY-W3 series modules in the final application board.

2.1 Overview

Although every application circuit must be properly designed, there are several points that require special attention during application design. A list of these points, in order of importance, follows:

- Module antenna connection: **ANT0, ANT1** and **ANT2** pins.
  Antenna circuits affect the RF compliance of all applications that include the certification schemes supported by JODY-W3 modules. To maintain compliance and subsequent certification of the application design, it is important to observe the antenna schematic and layout design for Antenna interfaces.
- Module supply: **3V3**, **1V8, VIO**, and **GND** pins.
  Supply circuits can affect the RF performance. It is important to observe the schematic and layout design for Supply interfaces.
- High-speed interfaces: **PCIe**, **SDIO** pins.
  High-speed interfaces are a potential source of radiated noise that can affect the regulatory compliance standards for radiated emissions. It is important to follow the PCI express, SDIO 3.0 and General high-speed layout guidelines.
- System functions: **PD#** and pins shown as **Configuration pins**.
  Careful utilization of these pins in the application design is required to guarantee that the voltage level is correctly defined during module boot. It is important to follow the pin recommendations in the General high-speed layout guidelines.
- Other pins: High-speed **UART**, **PCM**, **specific signals** and **NC** pins.
  Careful utilization of these pins is required to guarantee proper functionality. It is important to follow the schematic and design layout recommendations in General high-speed layout guidelines.

2.2 Antenna interfaces

JODY-W3 modules provide the following RF interface options for connecting the external antennas:

JODY-W354/JODY-W374 ports:

- **ANT0** for Wi-Fi 5 GHz and Bluetooth connectivity.
- **ANT1** for 2.4 and 5 GHz Wi-Fi connectivity.

JODY-W377 ports:

- **ANT0** for 2.4 and 5 GHz Wi-Fi connectivity.
- **ANT1** for 2.4 and 5 GHz Wi-Fi connectivity.
- **ANT2** for Bluetooth connectivity.

ANT ports have a nominal characteristic impedance of 50 Ω. For correct impedance matching these ports must be connected to the respective antenna through a 50 Ω transmission line. Poor termination of **ANT** pins can result in degraded performance of the module.

To optimize the isolation between the antennas and ensure good performance of the application, follow the requirements described in Table 16 and Table 17.

⚠ According to FCC regulations, the transmission line from the module antenna pin to the physical antenna (or antenna connector on the host PCB) is considered as part of the approved antenna design. Therefore, module integrators must use exactly the antenna reference design used in the module FCC type approval or certify their own design.

2.2.1 Antenna design

At the start the application design phase, when the mechanical design and the physical dimensions of the board are still under analysis/decision, the antenna integration shall be considered. This since the compliance and subsequent certification of the RF design depends heavily on the radiating performance of the antennas.

To ensure that the RF certification of JODY-W3 modules is extended through to the application design, it is important to carefully follow the guidelines outlined below.

- External antennas, including, linear monopole classes:
  - Place the module and antenna in any convenient area on the board. External antennas do not impose any restriction on where the module is placed on the PCB.
  - Select antennas with an optimal radiating performance in the operating bands. The radiation performance depends mainly on the antennas.
  - Choose RF cables that offer minimum insertion loss. Unnecessary insertion loss is introduced by low quality or long cables. Large insertion losses reduce radiation performance.
  - Use a high-quality 50 Ω coaxial connector for proper PCB-to-RF-cable transition.

- Integrated antennas, such as patch-like antennas:
  - Internal integrated antennas impose some physical restrictions on the PCB design:
    - Integrated antennas excite RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane related to the antenna element must be considered.
    - Find a numerical example to estimate the physical restrictions on a PCB, where: Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.5 cm in free space or 1.5 cm on a FR4 substrate PCB.

- Choose antennas with optimal radiating performance in the operating bands. Radiation performance depends on the complete product and antenna system design, including the mechanical design and usage of the product. Table 16 summarizes the requirements for the antenna RF interface.

- Make the RF isolation between the system antennas as high as possible, and the correlation between the 3D radiation patterns of the two antennas as low as possible. In general, RF separation of at least a quarter wavelength between the two antennas is required to achieve a minimum isolation and low pattern correlation. If possible, increase the separation to maximize the performance and fulfill the requirements in Table 17.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of Antenna pins.
Frequency Range	2400 – 2500 MHz 5150 – 5850 MHz	For 802.11b/g/n/ax and Bluetooth. For 802.11a/n/ac/ax.

Item	Requirements	Remarks
Return Loss	S11 < -10 dB (VSWR < 2:1) recommended S11 < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S11, as the VSWR, refers to the amount of reflected power, measuring how well the primary antenna RF connection matches the 50 Ω characteristic impedance of antenna pins. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of antenna pins over the operating frequency range, to maximize the amount of power transferred to the antenna.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power fed to the antenna input: the efficiency is a measure of how well an antenna receives or transmits.
Maximum Gain		The maximum antenna gain must not exceed the value specified in type approval documentation to comply with regulatory agencies radiation exposure limits.

Table 16: Summary of antenna interface requirements

Table 17 specifies additional requirements for implementing a dual antenna design.

Item	Requirements	Remarks
Isolation (in-band)	S21 > 30 dB recommended	The antenna-to-antenna isolation is the S21 parameter between the two antennas in the band of operation. Lower isolation might be acceptable depending on use-case scenario and performance requirements.
Isolation (out-of-band)	S21 > 35 dB recommended S21 > 30 dB acceptable	Out-of-band isolation is evaluated in the band of the aggressor. This ensures that the transmitting signal from the other radio is sufficiently attenuated by the receiving antenna. It also avoids any saturation and intermodulation effect on the receiver port.
Envelope Correlation Coefficient (ECC)	ECC < 0.1 recommended ECC < 0.5 acceptable	The ECC parameter correlates the far field parameters between antennas in the same system. A low ECC parameter is fundamental in improving the performance of MIMO-based systems.

Table 17: Summary of Wi-Fi/Bluetooth coexistence requirements

⚠ When operating dual antennas in the same 2.4 GHz band, sufficient isolation is critical for attaining an optimal throughput performance in Wi-Fi/Bluetooth coexistence mode.

Select antennas that provide:

- Optimal return loss (or VSWR) over all the operating frequencies.
- Optimal efficiency figure over all the operating frequencies.
- An appropriate gain that does not exceed the regulatory limits specified in some regulatory country authorities like the FCC in the United States.

It is recommended to add pads for a PI-filter for impedance tuning optimization on the antenna trace if later needed.

A useful approach for the antenna micro-strip design is to place an U.FL connector close to the embedded PCB or chip antenna. The U.FL connector only needs to be mounted on units used for verification.

2.2.1.1 RF connector design

If an external antenna is required, the designer should consider using a proper RF connector. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Table 18 suggests some RF connector plugs that can be used by the designers to connect RF coaxial cables based on the declaration of the respective manufacturers. The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitable mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	

Table 18: U.FL compatible plug connector

Typically, the RF plug is available as a cable assembly. Different types of cable assembly are available; the user should select the cable assembly best suited to the application. The key characteristics are:

- RF plug type: Select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Typically from 0.8 mm to 1.37 mm. Select thicker cables to minimize insertion loss
- Cable length: Standard length is typically 100 mm or 200 mm; custom lengths may be available on request. Select shorter cables to minimize insertion loss.
- RF connector on the other side of the cable: for example another U.FL (for board-to-board connection) or SMA (for panel mounting)

Consider that SMT connectors are typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect U.FL connector to a more robust connector such as SMA fixed on panel.

☞ A de-facto standard for SMA connectors implies the usage of reverse polarity connectors (RP-SMA) on end-user accessible Wi-Fi and Bluetooth interfaces to increase the difficulty to replace the antenna with higher gain versions and exceed regulatory limits.

The following recommendations apply for proper layout of the connector:

- Strictly follow the connector manufacturer’s recommended layout. Some examples are provided below:
  - SMA Pin-Through-Hole connectors require GND keep-out (that is, clearance, a void area) on all the layers around the central pin up to annular pins of the four GND posts.
  - U.FL surface mounted connectors require no conductive traces (that is, clearance, a void area) in the area below the connector between the GND land pins.
- In case of that the connector’s RF pin size is wider than the microstrip, the GND layer beneath the RF connector shall be removed to minimize the stray capacitance and thus keeping the RF line to 50 Ω. For example, the active pin of the UF.L connector must have a GND keep-out (also called “void area”) on at least the first inner layer. This to reduce parasitic capacitance to ground. A layout example of the U.FL connector is shown in Figure 6. See also the JODY-W3 antenna reference design application note [22].

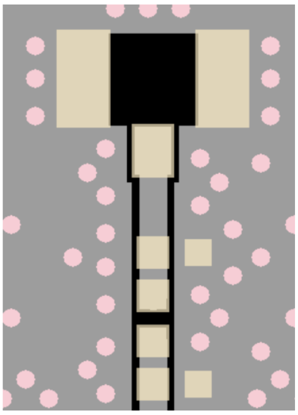

Figure 6: U.FL connector layout example with pi-matching components placed on top of microstrip

2.2.1.2 Integrated antenna design

If integrated antennas are used, the transmission line is terminated by the antennas themselves. Follow the guidelines given below:

- The antenna design process should start together with the mechanical design of the product. PCB mock-ups are useful in estimating overall efficiency and radiation path of the intended design during early development stages.
- Use antennas designed by an antenna manufacturer providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the related integrated antenna requirements. The ground plane of the application PCB may be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated, however overall antenna efficiency may benefit from larger ground planes. Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts such as metal objects or ferrite sheets as they may absorb part of the radiated power, shift the resonant frequency of the antenna or affect the antenna radiation pattern.
- It is highly recommended to strictly follow the specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning/matching to reach the target performance. It is recommended to plan measurement and validation activities with the antenna manufacturer before releasing the end-product to manufacturing.
- The receiver section may be affected by noise sources like hi-speed digital busses. Avoid placing the antenna close to busses as DDR or consider taking specific countermeasures like metal shields or ferrite sheets to reduce the interference.
- Take care of interaction between co-located RF systems like LTE sidebands on 2.4 GHz band. Transmitted power may interact or disturb the performance of JODY-W3 modules where specific LTE filter is not present.

2.2.1.3 RF Transmission line design

RF transmission lines, such as those that connect from **ANT** pins to their related antenna connectors, must be designed with a characteristic impedance of 50 Ω.

Figure 7 shows the design options and the most important parameters for designing a transmission line on a PCB:

- Microstrip. A track separated with dielectric material and coupled to a single ground plane.
- Coplanar microstrip. A track separated with dielectric material and coupled to both the ground plane and side conductor.

- Stripline. A track separated by dielectric material and sandwiched between two parallel ground planes.

The most common configuration for a printed circuit board (PCB) is the coplanar microstrip, as shown in Figure 7.

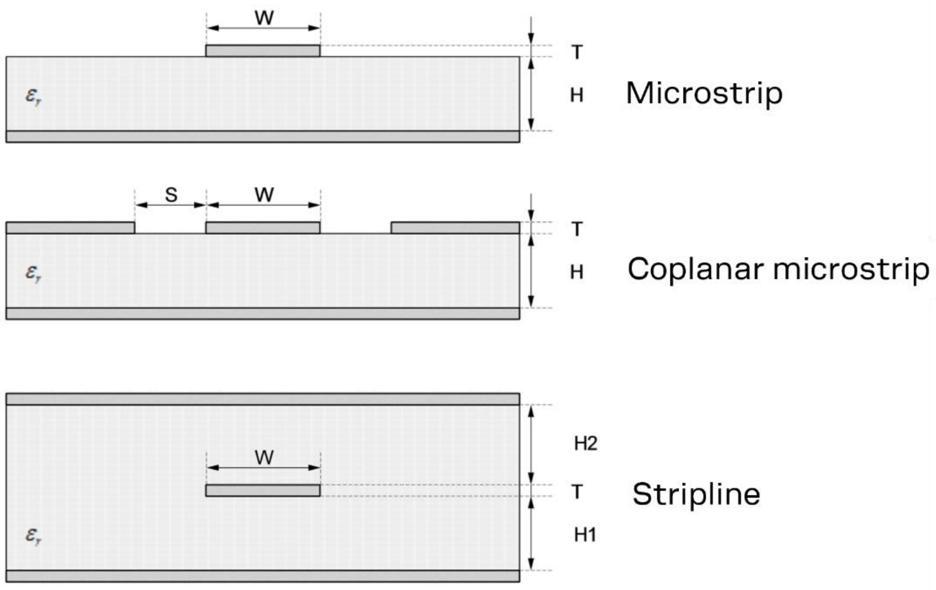

Figure 7: Transmission line trace design

Follow these recommendations to design a 50 Ω transmission line correctly:

- The designer must provide enough clearance from surrounding traces and ground in the same layer. Generally, the trace to ground clearance should be at least twice that of the trace width. The transmission line should also be "guarded" by the ground plane area on each side.
- In the first iteration, calculate the characteristic impedance using tools provided by the layout software. Ask the PCB manufacturer to provide the final values usually calculated using dedicated software and production stack-ups. It is sometimes possible to request an impedance test coupon on side of the panel to measure the real impedance of the traces.
- Although FR-4 dielectric material can result in high losses at high frequencies, it can still be an appropriate choice for RF designs. In which case, aim to:
  - Minimize RF trace lengths to reduce dielectric losses.
  - If traces longer than few centimeters are needed, use a coaxial connector and cable to reduce losses.
  - For good impedance control over the PCB manufacturing process, design the stack-up with wide 50 Ω traces with width of at least 200 µm.
  - Contact the PCB manufacturer for specific tolerance of controlled impedance traces. As FR-4 material exhibits poor thickness stability it gives less control of impedance over the trace width.
- For PCBs with components larger than 0402 and dielectric thickness below 200 µm, add a keep-out, that is, some clearance (void area) on the ground reference layer below any pin on the RF transmission lines. This helps to reduce the parasitic capacitance to ground.
- Route RF lines in 45 ° angle and avoid acute angles. The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible.
- Add GND stitching vias around transmission lines, as shown in Figure 8.
- Provide a sufficient number of vias on the adjacent metal layer. Include a solid metal connection between the adjacent metal layer on the PCB stack-up to the main ground layer.

- To avoid crosstalk between RF traces and Hi-impedance or analog signals, route RF transmission lines as far from noise sources (like switching supplies and digital lines) and any other sensitive circuit.
- Avoid stubs on the transmission lines. Any component on the transmission line should be placed with the connected pin located over the trace. Also avoid any unnecessary components on RF traces.

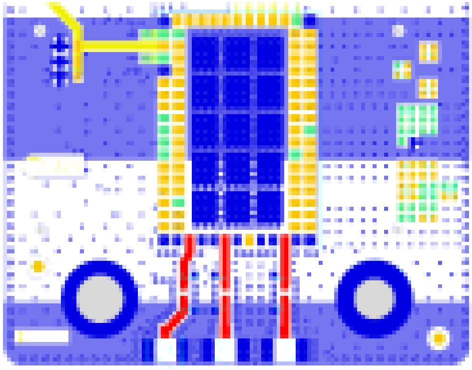

Figure 8: RF trace and ground design example

2.3 Supply interfaces

2.3.1 Module supply design

Though the GND pins are internally connected, it is recommended to connect all the available ground pins to solid ground on the application board as a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance. JODY-W3 modules must be sourced through **3V3, 1V8** and **VIO** pins with proper DC power supplies that comply with the voltage supply requirements summarized in Table 3.

Good connection of the JODY-W3 series module power supply pins with DC supply source is required for accurate RF performance and schematic guidelines are summarized below:

- All power supply pins must be connected to an appropriate DC source.
- Any series component with Equivalent Series Resistance (ESR) greater than a few mΩ should be avoided. Only exceptions to this rule are ferrite beads used for DC filtering, however those parts should be used carefully to avoid instability of the DC/DC supply powering the module and are in general not required.
- A minimum bulk capacitance of 10 µF on the **3V3** rail is required (optionally on **1V8** and **VIO**) close to the module to help filter current spikes from the RF section and avoid ground bounce. The preferred choice is a ceramic capacitor with X7R or X5R dielectric due to low ESR/ESL. Special care should be taken in the selection of X5R/X7R dielectrics due to capacitance derating vs DC bias voltage.
- Additional bypass capacitors in the range of 100 nF to 1 µF on all supply pins are required for high frequency filtering. The preferred choice is a ceramic capacitor with X7R or X5R dielectric due to low ESR/ESL. Smaller size bypass capacitors should be chosen for the manufacturing process to minimize ESL. This capacitor should be placed as close as possible to the module supply pin.

2.3.1.1 Guidelines for VCC supply circuit design using a switching regulator

It is recommended to use a Switched Mode Power Supply (SMPS) when the difference from the available supply rail to the **JODY-W3** supply rails allows significant power savings. For example, conversion of a 12 V or greater voltage supply to the nominal 3.3 V value for the **3V3** supply.

The characteristics of the SMPS connected to the **3V3** pin should meet the following prerequisites to comply with the module requirements summarized in Table 3.

- **Power capability:** The switching regulator together with any additional filter in front of the module must be capable of providing a voltage within the specified operating range. The regulator must also be capable of delivering the specified peak current.
- **Low output ripple**: The switching regulator peak-to-peak Voltage ripple must not exceed the specified limits. This requirement applies both to voltage ripple generated by SMPS operating frequency and to high frequency noise generated by power switching.
- **PWM/PFM mode operation**: It is preferable to select regulators with fixed Pulse Width Modulation (PWM) mode. Pulse Frequency Modulation (PFM) mode typically exhibits higher ripple and may affect RF performance. If power consumption is not a concern, PFM/PWM mode transitions should be avoided in favor of fixed PWM operation to reduce the peak-to-peak noise on voltage rails. Switching regulators with mixed PWM/PFM mode can be used provided that the PFM/PWM modes and transition between modes complies with the requirements.

2.3.1.2 Guidelines for supply circuit design using a Low Drop-Out (LDO) linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **3V3, 1V8** or **VIO** value is relatively low. The linear regulators provide acceptable efficiency when transforming a supply of less than 5 V to a voltage value within the normal operating range of the module. A linear regulator can be also considered to power the **VIO** section due to the low current requirements, especially if cascaded from a SMPS-generated low voltage rail.

The characteristics of the Low Drop-Out (LDO) linear regulator used to power the voltage rails must meet the following prerequisites to comply with the requirements summarized in Table 3.

- **Power capabilities**: The LDO linear regulator with its output circuit must be capable of providing a voltage value to the **3V3, 1V8** or **VIO** pins within the specified operating range and must be capable of withstanding and delivering the maximum specified peak current while in connected-mode.
- **Power dissipation**: The power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range. The worst-case junction temperature can be estimated as shown below:

  $$T_{j,est} = (V_{in} - V_{out}) * I_{avg} * \theta_{ja} + T_a$$

  Where: θ_{ja} is the junction-to-ambient thermal resistance of the LDO's package[8], I_{avg} is the current consumption of the given voltage rail in continuous TX/RX mode and T_a is the maximum operating temperature of the end product inside the housing.

2.4 Data communication interfaces

2.4.1 PCI Express

The PCI Express (Peripheral Component Interconnect Express) bus of JODY-W3 series modules support PCIe v2.0 connectivity at transfer rates up to 5 Gbaud. PCIe differential clock and data pairs are a controlled impedance bus, and the main parameters considered for the track impedance calculation are depicted in Figure 9.

[8] Thermal dissipation capability reported on datasheets is usually tested on a reference board with adequate copper area (ref. to JESD51 [10]). Junction temperature on a typical PCB may be higher than the estimated value due to the limited space to dissipate the heat. Thermal reliefs on pads also affect the capability of a device to dissipate the heat.

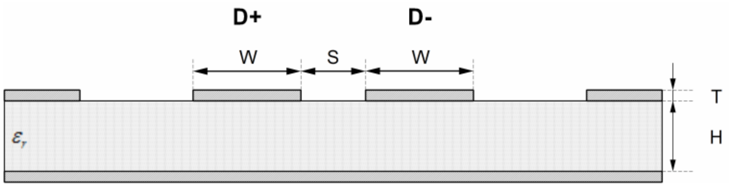

Figure 9: Differential pair, generic controlled impedance parameters

To guarantee bus signal integrity and avoid EMI issues, the PCIe data lines must follow the recommendations described in Table 19.

Signal Group	Parameter	Min.	Typ.	Max.	Unit
PCIe differential data	Single Ended impedance, Z_{SE}	60			Ω
	Differential impedance, Z_{diff}		100		Ω
	Common mode impedance, Z_{CM}		50		Ω
	Impedance control, Z_{SE}, Z_{diff}, Z_{CM}	$Z_0 - 20\%$	Z_0	$Z_0 + 20\%$	
	PCB signal attenuation margin			13,2	dB
	Bus skew length mismatch on same differential pair			0,1	mm
	Bus skew length mismatch between differential pairs	Not required			-
	Isolation to other pairs and PCB signals	5*W			

Table 19: PCI express bus requirements

2.4.2 SDIO 3.0

The SDIO 3.0 bus supported in JODY-W3 series modules can support a clock frequency up to 208 MHz. Consequently, the modules demand special care to guarantee signal integrity requirements and to minimize EMI issues. The signals should be routed with a single ended impedance of 50 Ω.

It is advisable to route all signals in the bus with the same length and have appropriate grounding in the surrounding layers. The total bus length should also be minimized. The layout of the SDIO bus should be implemented so that crosstalk with other parts of the circuit is minimized. This provides adequate isolation between the signals, clock, and surrounding busses/traces. Include an undisrupted return current path in close vicinity to the signal traces. Figure 10 shows the suggested application schematic for the SDIO bus in JODY-W3 modules, while Table 20 summarizes the electrical requirements of the bus.

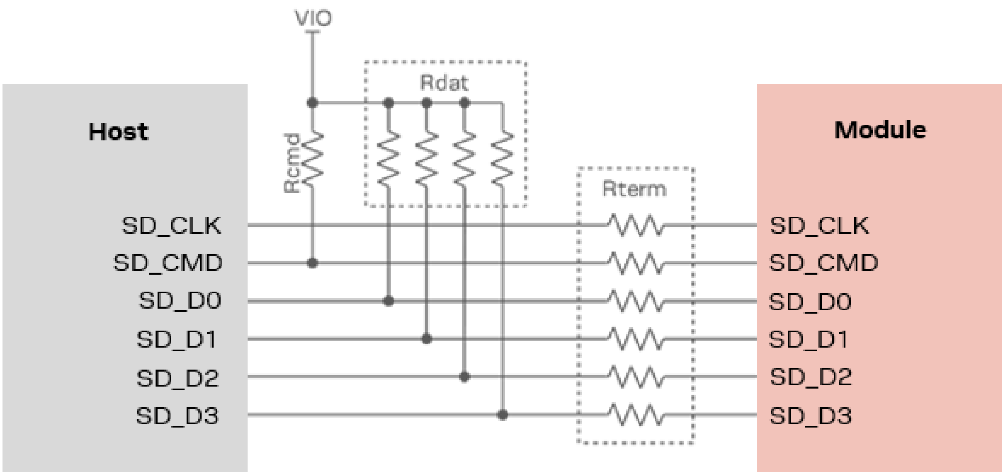

Figure 10: SDIO application schematic

☞ A small value capacitor in the range of few pF to GND could be considered for **SDIO_CLK** as an EMI debug option and signal termination. This capacitor should be placed as close as possible to the JODY-W3 clock input pin and can be assembled only for EMI purposes. The capacitor increases the total line capacitance but must not exceed the total capacitance necessary to avoid violating clock rise and degrading the timing specifications.

Signal Group	Parameter	Min.	Typ.	Max.	Unit
CLK, CMD, DAT[0:3]	Single ended impedance, Z_0		50		Ω
CLK, CMD, DAT[0:3]	Impedance control	$Z_0 - 10\%$	Z_0	$Z_0 + 10\%$	Ω
DAT[0:3]	Pull-Up range, Rdat	10	47	100	kΩ
CMD	Pull-Up range, Rcmd	10	10	50	kΩ
CLK, CMD, DAT[0:3]	Series termination (Host side), Rterm[9]	0	0		Ω
CLK, CMD, DAT[0:3]	Bus length[10]			100	mm
CMD, DAT[0:3]	Bus skew length mismatch to CLK	-3		+3	mm
CLK	Center to center CLK to other SDIO signals[11]	4*W			
CMD, DAT[0:3]	Center to center between signals[11]	3*W			

Table 20: SDIO bus requirements

☞ JODY-W3 series supports only 1.8 V SDIO signal voltage. A level shifter is needed to connect to a 3.3 V host controller.

2.4.3 High-speed UART interface

The high-speed UART interface for the JODY-W3 complies with the HCI UART Transport layer and uses the settings shown in Table 21.

UART Settings	
Baud rate default after reset	115 200 baud
Baud rate default after firmware load	3 000 000 baud
Data bits	8
Parity bit	No parity
Stop bit	1 stop bit
Flow Control	RTS/CTS

Table 21: HCI UART transport layer settings

Flow control with RTS/CTS is used to prevent temporary UART buffer overrun.

- When **CTS** is set to logic level 1 the host/host controller is allowed to send.
- When **CTS** is set to logic level 0 the host/host controller is not allowed to send.

☞ The use of hardware flow control with RTS/CTS is mandatory.

Common baud rates supported by the UART interface are listed in Table 22. The acceptable deviation from the UART receive target baud rate is ±3%.

Baud rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	
4800	76800	921600	2000000	
9600	115200	1000000	2100000	

[9] Series termination values larger than typical recommended only for addressing EMI issues.
[10] Routing should minimize the total bus length.
[11] Center to center spacing requirement can be ignored for up to 10 mm of routed length to accommodate BGA escape.

19200	230400	1382400	2764800

Table 22: Possible baud rates for the UART interface

After a hardware reset, the UART interface is configured for 115 200 baud without flow control. When the firmware is loaded, the baud rate is set to 3 000 000 baud and flow control is enabled. A host application can change the baud rate for the UART interface with the vendor specific HCI command `HCI_CMD_UART_BAUD` (OCF `0x0009`). For an example of how to change the baud rate, see also Bluetooth usage.

```
hcitool -i hci0 cmd 0x3F 0x0009 <4 byte little-endian value for baud rate>
```

☞ The HCI command complete event is generated at the old baud rate. Once the host receives the command complete at the old baud rate, it can switch to the new baud rate and should wait for 5 ms or more before sending any new command.

2.5 Other interfaces and notes

All digital pins have internal keeper resistors and can be left open if they are not used.

2.6 General high-speed layout guidelines

These general design guidelines are considered as best practices and are valid for any bus present in JODY-W3 modules; the designer should prioritize the layout of higher speed busses. Low-frequency signals are generally not layout critical.

⚠ One exception is represented by high-impedance traces (such as signals driven by weak pull resistors) that may be affected by crosstalk. For those traces, a supplementary isolation of 4*W from other busses is recommended.

2.6.1 General considerations for schematic design and PCB floor-planning

- Verify which signal bus requires termination and add series resistor terminations to the schematics.
- Carefully consider the placement of the module with respect to antenna position and host processor; RF trace length should be minimized first, followed by SDIO bus length.
- SDIO bus routing shall be planned to minimize layer-to-layer transition to a minimum.
- Verify with PCB manufacturer allowable stack-ups and controlled impedance dimensioning for antenna traces and busses.
- Verify that the power supply design and power sequence are compliant with JODY-W3 specifications described in System function interfaces.

2.6.2 Component placement

- Accessory parts like bypass capacitors shall be placed as close as possible to the module to improve filtering capability, prioritizing the placement of the smallest size capacitor close to module pins.
- Do not place components close to the antenna area. The designer should carefully follow the recommendations of the antenna manufacturer concerning the distance of the antenna in relation to other parts of the system. The designer should also maximize the distance of the antenna to High-frequency busses like DDRs and related components or consider an optional metal shield to reduce interferences that could be picked up by the antenna and subsequently reduce module sensitivity.

2.6.3 Layout and manufacturing

- Avoid stubs on high-speed signals. Test points or component pads should be placed over the PCB trace.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length; longer traces degrade signal performance. Ensure that maximum allowable length for high-speed busses is not exceeded.
- Ensure to track your impedance matched traces. Consult early with your PCB manufacturer for proper stack-up definition.
- RF, analog and digital sections should have dedicated and clearly separated areas on the board.
- No digital routing is allowed in the GND reference plane area of RF traces (**ANT** pins and Antenna).
- It is strongly recommended to avoid digital routing beneath all layers of RF traces.
- Ground cuts or separation are not allowed below the module.
- Minimize the length of the RF traces as first priority. Then, minimize bus length to reduce potential EMI issues from digital busses.
- All traces (Including low speed or DC traces) must couple with a reference plane (GND or power), Hi-speed busses should be referenced to the ground plane. In this case, if the designer needs to change the ground reference, an adequate number of GND vias must be added in the area of transition to provide a low impedance path between the two GND layers for the return current.
- Hi-Speed busses are not allowed to change reference plane. If a reference plane change is unavoidable, some capacitors should be added in the area to provide a low impedance return path through the different reference planes.
- Trace routing should keep a distance greater than 3*W from the ground plane routing edge.
- Power planes should keep a distance from the PCB edge sufficient to route a ground ring around the PCB, the ground ring must then be stitched to other layers through vias.

⚠ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application baseboard below JODY-W3 series modules. Avoid placing temperature sensitive devices close to the module and provide adequate grounding to transfer the generated heat to the PCB.

2.7 Module footprint and paste mask

Figure 11 shows the recommended footprint for JODY-W3 module, bottom view. All dimensions are specified in the JODY-W3 series data sheet [1].

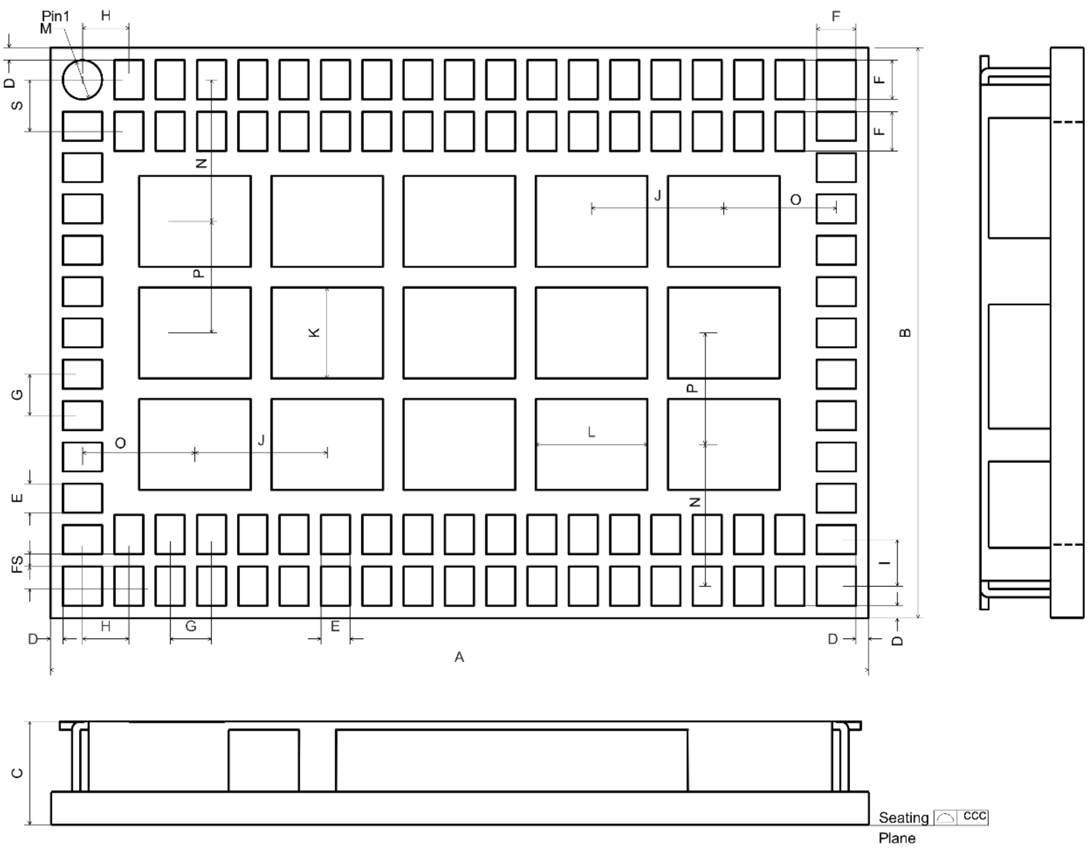

Figure 11: Recommended footprint for JODY-W3 module, bottom view

⚠ JODY-W3 have additional pins compared with JODY-W1 and JODY-W2, for future use. Connect these according to the Pin list.

Figure 11 shows the pin layout for the JODY-W3 series module. The proposed land pattern layout reflects the pin layout of the module. Both Solder Mask Defined (SMD) and Non Solder Mask Defined (NSMD) pins can be used, however the following considerations apply:

- Pins 1 to 94 should be NSMD
- Inner pads must have a good thermal bonding to PCB ground planes to help spreading the heat generated by the module.
- If NSMD design is chosen for inner pads, thermal reliefs should be considered and 4 or 9 vias per pad must be added for heat sink. Those vias may require copper capping.
- If SMD design is chosen for inner pads, the land pattern can be flooded on a ground plane beneath the module and vias added around the pads for heat sinking.

The suggested stencil layout for the JODY-W3 module is to follow the copper pad layout exactly as described in Figure 11 for the outer pads, while the central pads should implement a special solder paste pattern with the following characteristics:

- Solder paste area should be split in several smaller parts, typically four to nine depending on copper pad area.
- Total solder paste area should cover about 50% to 60% of copper thermal pad area.
- Total solder paste area must not exceed 65% of copper thermal pad area.

Missing to consider solder paste optimization can lead to poor soldering quality in production.

A suggested stencil opening implementation is shown in Figure 12.

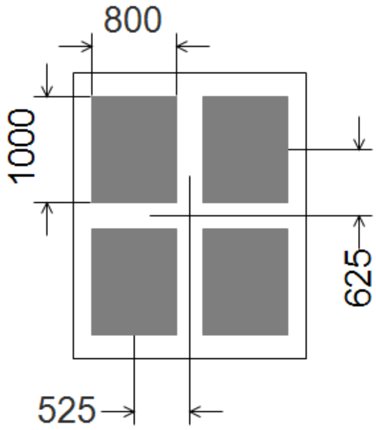

Figure 12: Stencil opening example for inner thermal pads (dimensions in µm)

⚠ The exact mask geometries, distances and stencil thicknesses must be adapted to the specific production process of the customer.

2.8 Thermal guidelines

JODY-W3 series modules are designed to operate from -40 °C to +85 °C at an ambient temperature inside the enclosure box. The board will generate heat during high loads that must be dissipated to sustain the lifetime of the components.

The improvement of thermal dissipation in the module decreases its internal temperature and consequently increases the long-term reliability of the device for applications operating at high ambient temperatures.

For best performance, recommended layouts should follow the following guidelines:

- Vias specification for ground filling: $300/600\ \mu m$, no thermal reliefs are allowed on vias.
- Ground vias density under the module: $50\ vias/cm^2$, thermal vias can be placed in gaps between the thermal pads of the module.
- Minimum layer count and copper thickness: $4\ layers$, $35\ \mu m$.
- Minimum board size: $55x70\ mm$.
- Power planes and signal traces should not cross the layers beneath the module to maximize heat flow from the module.

Those recommendations allow the design to achieve a thermal characterization parameter of $\psi_{JB} = 7.24\ °C/W$, where JB refers to the “module’s junction to main PCB bottom side”.

The following additional hardware techniques can be used to improve the thermal performance of the module in customer applications:

- Maximize the return loss of the antenna to reduce reflected RF power to the module.
- Improve the efficiency and the thermal design of any component that generates heat in the application, including power supplies and processor, to spread the generated heat distribution over the application device.
- Design the mechanical enclosure of the application device properly to provide ventilation and good thermal dissipation.
- For continuous operation at high temperatures, high-power density applications, or reduced PCB size, the designer can consider including a heat sink on main bottom side of the PCB. The heat sink should be connected using electrically insulated / high thermal conductivity adhesive[12].

[12] Typically not required.

2.9 ESD guidelines

JODY-W3 modules are manufactured through a highly automated process, which complies with IEC61340-5-1 [6] (STM5.2-1999 Class M1 devices) standard. A manufacturing process on the customer's manufacturing site that implements a basic ESD control program is considered sufficient to guarantee the necessary precautions[13] for handling the modules. The ESD ratings for JODY-W3 module pins are defined in the JODY-W3 series data sheet, UBX-19010615 [1].

The designer must implement proper measures to protect from ESD events on any pin that may be exposed to the end user in compliance with the following European regulations:

- ESD testing standard CENELEC EN 61000-4-2 [4]
  Radio equipment standard ETSI EN 301 489-1 [5]

The minimum requirements as per these European regulations are summarized in Table 23.

Application	Category	Immunity level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration of the end product.	Contact discharge	4 kV
	Air discharge	8 kV

Table 23: Minimum ESD immunity requirements based on EN 61000-4-2

Compliance with standard protection level as specified in EN 61000-4-2 [4] is achieved by including proper ESD protection in parallel to the line and close to areas that are accessible to the end user.

⚠ Special care should be taken if the **ANT** pins must be protected by choosing an ESD absorber with adequate parasitic capacitance. For 5 GHz operation, a protection with maximum internal capacitance of 0.1 pF is recommended.

[13] Minimum ESD protection level for safe handling is specified in JEDEC JEP155 (HBM) and JEP157 (CDM) for ±500 V and ±250 V respectively.

2.10 Design-in checklists

2.10.1 Schematic checklist

☐ JODY-W3 module pins are properly numbered and designated on the schematic (including thermal pins). See Pin list.
☐ Power supply design complies with the voltage supply requirements in Table 3 and the power supply requirements described in the JODY-W3 series data sheet [1].
☐ The power sequence is properly implemented. See Power-up sequence.
☐ Adequate bypassing is present in front of each power pin. See Component placement.
☐ Each signal group is consistent with its own power rail supply or proper signal translation has been provided. See Pin list.
☐ Configuration pins are properly set at bootstrap. See Configuration pins.
☐ SDIO bus includes series resistors and pull-ups. See SDIO 3.0.
☐ Unused pins are properly terminated. See Unused pins.
☐ A pi-filter is provided in front of each antenna for final matching. See Antenna design.
☐ Additional RF co-location filters have been considered in the design. See Block diagrams.

2.10.2 Layout checklist

☐ PCB stack-up and controlled impedance traces follow PCB manufacturer's recommendation. See RF Transmission line design.
☐ All pins are properly connected, and the footprint follows u-blox pin design recommendations. See Module footprint and paste mask.
☐ Proper clearance has been provided between RF section and digital section. See Layout and manufacturing.
☐ Proper isolation is provided between Antennas (RF co-location, diversity, MIMO, or multi-antenna design). See Antenna design.
☐ Bypass capacitors are placed close to the module. See Component placement.
☐ Low impedance power path has been provided to the module. See Module supply design.
☐ Controlled impedance traces are properly implemented on the layout (both RF and digital) and follow PCB manufacturer recommendations. See Layout and manufacturing.
☐ 50 Ω RF traces and connectors follow the rules in Antenna interfaces.
☐ Antenna design has been reviewed by the antenna manufacturer.
☐ Proper grounding is provided to the module for low impedance return path and heat sink. See Module supply design.
☐ Reference plane skipping is minimized for high frequency busses. See Layout and manufacturing.
☐ All traces and planes are routed inside the area defined by the main ground plane. See Layout and manufacturing.
☐ u-blox has reviewed and approved the PCB[14].

[14] This is applicable only for end-products based on u-blox reference designs.

3 Software

The instructions in this chapter describe how to set up the JODY-W3 series module on a Linux operating system. Including several examples, it also describes how the reference driver packages are compiled and deployed in the target system.

The described configuration is based on the proprietary driver for the 88Q9098 chipset family from NXP that has been integrated onto an i.MX 8QuadMax Multisensory Enablement Kit (MEK) from NXP. The board connects to the JODY-W3 series module through the PCIe host interface and uses a USB-to-UART adapter to connect to the Bluetooth UART resident in the module.

☞ The proprietary driver developed by NXP and distributed by u-blox is only made available to customers that have signed a limited use license agreement (LULA-M) [3] with u-blox. The driver package and additional documentation can also be obtained directly from NXP.

☞ Open-source drivers for mainstream use are made available free of charge by NXP and are already pre-integrated into the Linux BSPs for the NXP i.MX application processors. See also Open-source Linux/Android drivers.

3.1 Available software packages

3.1.1 Open-source Linux/Android drivers

JODY-W3 series modules are based on the NXP 88Q9098/88W9098/AW690 chipsets. The drivers and firmware required to operate JODY-W3 series modules are developed by NXP and are already integrated into the Linux BSP for the NXP i.MX application processors [13].

The documentation for the software releases from NXP contains Wi-Fi and Bluetooth release notes and a list of supported software features. The driver source code is provided free of charge as open source under NXP license terms. Being open source allows the drivers to be integrated or ported to other non-NXP based host platforms. Yocto recipes for the driver and firmware, that can be used to develop custom Linux-based systems, are part of the NXP i.MX Linux BSP.

The latest version of the driver source code and Wi-Fi/Bluetooth firmware are available from the following open-source repositories:

- Wi-Fi driver: https://github.com/nxp-imx/mwifiex
- Firmware: https://github.com/NXP/imx-firmware
  - PCIe firmware: /nxp/FwImage_9098_PCIE
  - SDIO firmware: /nxp/FwImage_9098_SD
- i.MX meta-layer: https://github.com/nxp-imx/meta-imx
  - ./meta-bsp/recipes-connectivity/nxp-wlan-sdk
  - ./meta-bsp/recipes-kernel/kernel-modules/kernel-module-nxp89xx.bb
  - ./meta-bsp/recipes-kernel/linux-firmware/linux-firmware_%.bbappend

☞ Use the repository branches matching to the latest Linux BSP release version. At the time of publication, this is release 6.1.1_1.0.0.

The Wi-Fi driver uses the TCP/IP stack from the Linux kernel for data transmission and the `cfg80211` subsystem in the kernel for configuration and control. The `hci_uart` driver from the Linux kernel and BlueZ host stack are used for the Bluetooth part. For further information about initialization and configuration of the Wi-Fi and Bluetooth features, see also the NXP User Manual UM11490 [14].

3.1.2 Proprietary drivers

As described in Configuration pins, JODY-W3 series modules can be operated through different host interfaces. Each operation mode must use a dedicated host driver package. For information about the various components and the structure of the driver packages, see also Driver package structure.

The proprietary NXP driver package is available for the **PCIE-UART** host interface combination (PCIE-WLAN-UART-BT-9098), which uses the PCIe interface to operate Wi-Fi and the UART interface for Bluetooth.

The NXP driver packages are typically provided as two different licensing options:

- MGPL package: Full source code with GPLv2 license
- GPL package: Source code with proprietary license – except for the part of the Linux driver that binds to the kernel

For further information about license usage, see the license texts included in the driver package.

3.1.3 Additional u-blox software deliverables

A Yocto/OpenEmbedded meta layer for JODY-W3 is provided by u-blox. See also Yocto meta layer.

☞ JODY-W3 series software deliverables are available from your local support team. See Contact.

3.2 Supported kernel versions

Due to constant changes in the kernel subsystem APIs for different kernel releases, the driver source code must be aligned with each major and minor kernel release.

The driver packages have been verified on the following platforms and kernel versions:

Platform	SoC	Kernel version
NXP i.MX 8 MEK	i.MX 8QuadMax	4.14.98, 5.4.3, 5.10.72
NXP i.MX 8M EVK	i.MX 8mQuad	4.14.98, 5.4.3, 5.10.72
Renesas R-Car H3 Starter Kit	R-Car H3	5.10.41
Intel NUC10i3	Core-i3	5.4.115

Table 24: Tested Linux kernel versions for the JODY-W3 series modules reference drivers

The supplied software package supports Linux kernel from 2.6.32 to 6.0.0. As long as there is no change in the kernel API, this package can also support the latest kernel versions. If there are any changes to the kernel APIs you choose to use, you must make the necessary changes using patches. In case of any discrepancy, contact your local support team.

3.3 Driver package structure

The NXP driver packages include different components, depending on the supported host interfaces. The content of the packages is described in Table 25.

Component	Folder	Description
Release Notes and features	-	Release notes describing all of the supported features, changes and all known issues associated with the release.
FwImage	FwImage	Binary firmware images. For details about the firmware images, see also Table 26.
PCIE/SDIO-WIFI-*-app-src	wlan_src/mapp	Source code for the user space applications necessary to set up the different modes for Wi-Fi operation.

Component	Folder	Description
PCIE/SDIO-WIFI-*-src	wlan_src/mlinux	Source code for the driver module `moal.ko`, which implements the Linux-specific part of the Wi-Fi driver. This container also includes the driver, `Makefile` and `README` files.
PCIE/SDIO-WIFI-*-mlan-src	wlan_src/mlan	Source code for the driver module `mlan.ko`, which implements the chipset specific functionality of the Wi-Fi driver.
UART-*-src	muart_src	Source code for the HCI UART Bluetooth driver module `hci_uart.ko`.
UART-FW-LOADER-*-src	uartfwloader_src	Source code for the `fw_loader` firmware download tool used to download the Bluetooth firmware over UART in parallel mode.

Table 25: Components of the NXP driver package

3.4 Software architecture

From the software point of view, JODY-W3 series modules contain only on-board OTP memory with calibration parameters and MAC addresses. Consequently, the modules require a host-side driver and device firmware to run.

At startup and at every reset or power cycle, the host driver needs to download the firmware binary file to the module. The host driver interfaces the bus drivers with the upper layer protocol stacks of the operating system.

Figure 13 shows the different software components and upper layers required for the operation of JODY-W3 series modules.

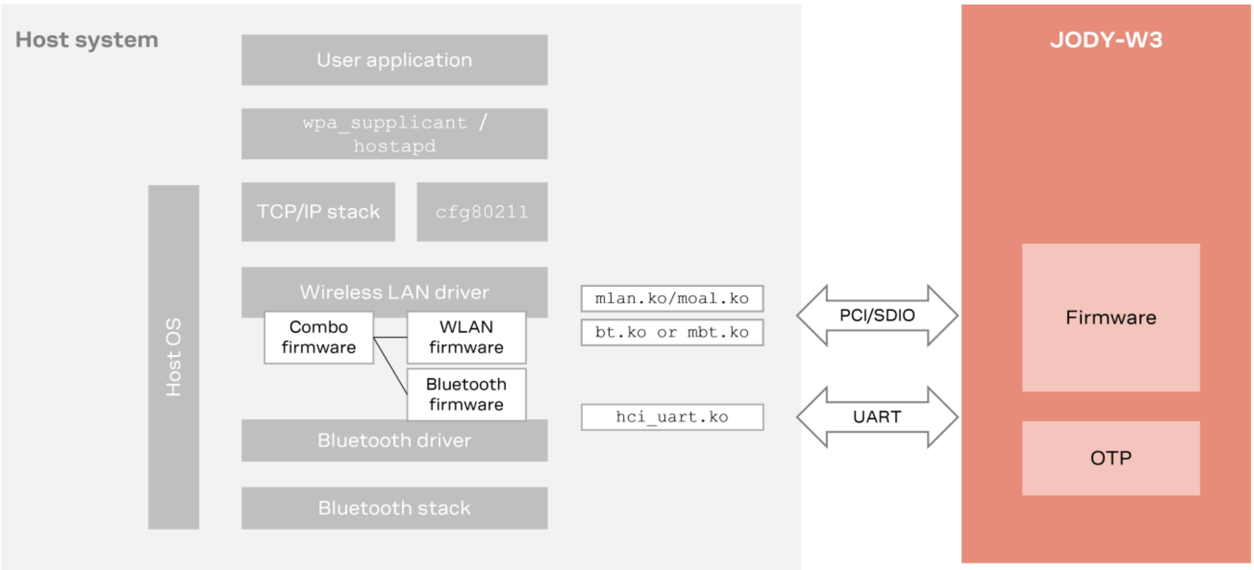

Figure 13: Basic software overview

3.4.1 Wi-Fi driver

The JODY-W3 series software package includes a dedicated Wi-Fi driver that has both Wireless Extension (WEXT) and Netlink-based (nl80211/cfg80211) driver configuration interfaces.

The Wi-Fi driver implementation is spread between two kernel modules – `moal` and `mlan`, where:

- `moal` implements the operating system (OS) specific bindings and handles the standard interfaces from the OS such as the network interface and manages to load the firmware to the JODY-W3 during the initialization phase.
- `mlan` implements the chipset specific functions and is independent from the OS.

Figure 14 shows the basic architecture of the Wi-Fi driver.

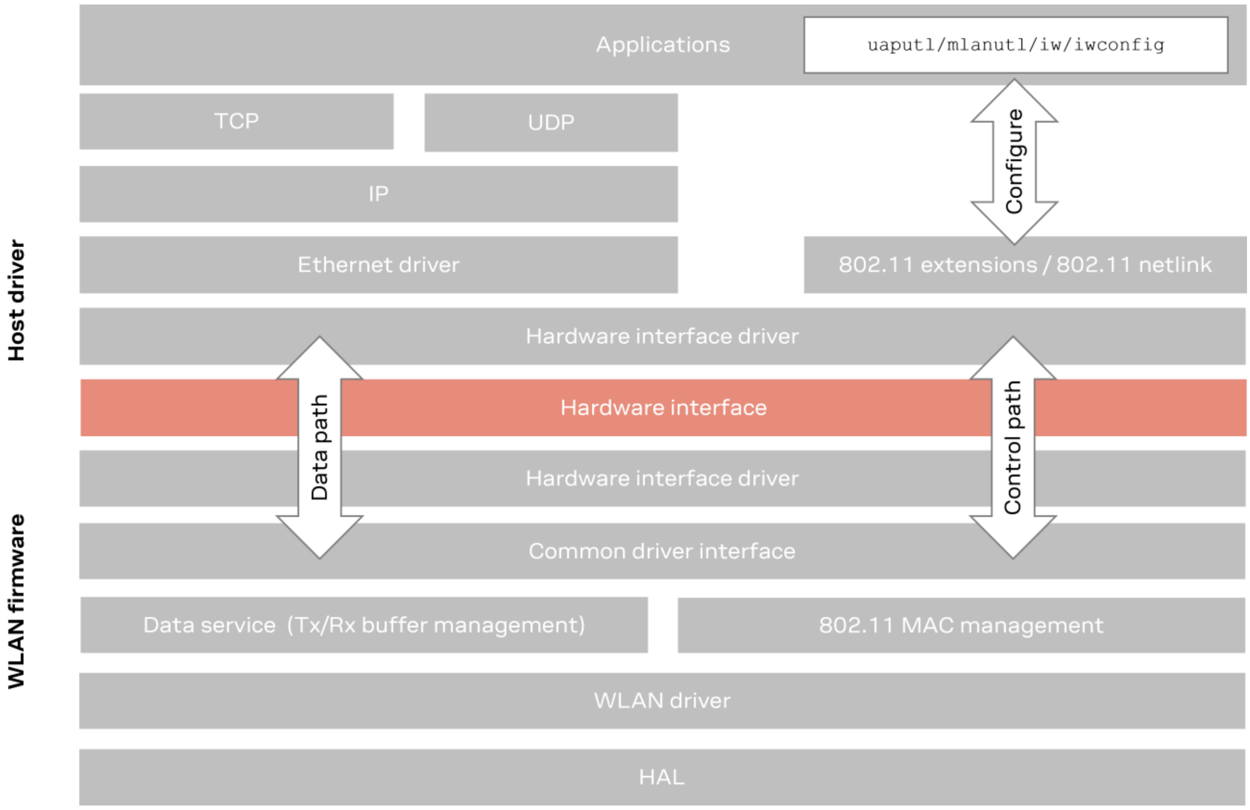

Figure 14: Basic Wi-Fi host driver and firmware architecture

3.4.2 Bluetooth driver

The standard Bluetooth protocol stack in Linux is provided by BlueZ. The reference driver package provides a Bluetooth driver for the JODY-W3 series module that performs the following functions:

- Data and command forwarding between upper protocol stack layers and the firmware
- Private command handling used between the driver and firmware handshakes only

The host system can access JODY-W3 series Bluetooth logic functions through the UART interface.

The Bluetooth driver `hci_uart` is included in the Linux kernel distribution to which NXP adds additional functionality. We recommend use of the `hci_uart` driver included in the NXP driver package over the Linux kernel variant. The `hci_uart` from the kernel must be disabled or compiled as a module.

The architecture of the Bluetooth driver and protocol stack is shown in Figure: 15.

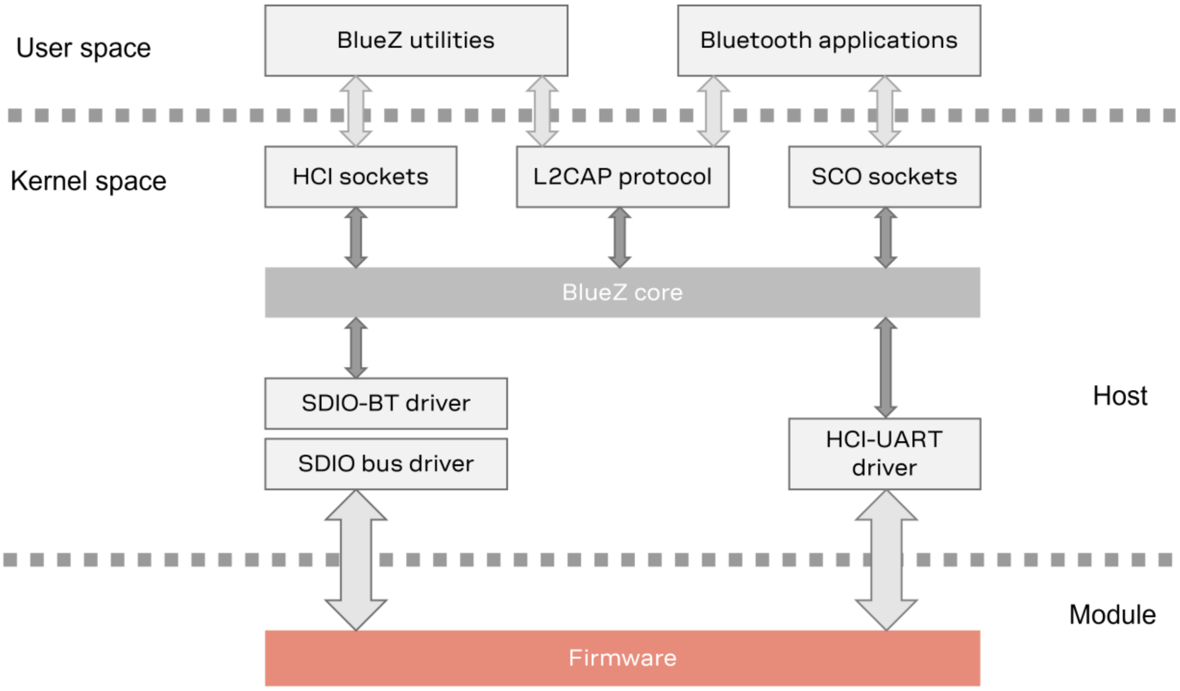

Figure: 15: Bluetooth driver and protocol stack

3.5 Compiling the drivers

The `README` files included in the driver package contain basic steps of the compilation procedure.

☞ The recipes in the Yocto/OpenEmbedded meta layer provided by u-blox are used to integrate the software package into Yocto projects. These also make useful references with which to better understand the process of compiling and deploying the software package more fully. See also Yocto meta layer.

3.5.1 Prerequisites

The appropriate Wi-Fi driver for use with JODY-W3 series modules depends on the PCI or MMC/SDIO subsystem of the Linux kernel. Consequently, support for the respective subsystem and the correct host controller driver must be enabled in the target kernel configuration of the system.

The driver supports the cfg80211 wireless configuration API for configuration management and it must be selected in the kernel configuration using the `CONFIG_CFG80211` option.

In order to use Bluetooth implementation in the Linux BlueZ stack, the kernel options `CONFIG_BT_HCIUART`, `CONFIG_BT_HCIUART_H4` must be enabled along with other Bluetooth protocols.

Prior to building the driver, the kernel needs to be prepared for the compilation of external kernel modules. To do this, change to the source directory of the kernel and run the following command:

```
$ make modules_prepare
```

3.6 Deploying the drivers

The drivers, firmware and additional software tools can be deployed at reasonable locations in the target root file system.

Using the Yocto recipes provided by u-blox, the utilities and modules typically install like this:

```
\
├── etc
│   └── modprobe.d
│       └── jody-w3-driver-pcieuart.conf
├── lib
│   ├── firmware
│   │   └── nxp
│   │       └── jody-w3-pcieuart
│   │           ├── pcie9098_wlan_v1.bin
│   │           ├── pcieuart9098_combo_v1.bin
│   │           └── uart9098_bt_v1.bin
│   └── modules
│       └── 4.14.98-imx[…]
│           └── updates
│               └── nxp
│                   └── 88q9098
│                       ├── hci_uart_jody-w3-pcieuart.ko
│                       ├── mlan_jody-w3-pcieuart.ko
│                       └── moal_jody-w3-pcieuart.ko
└── opt
    └── jody-w3
        └── pcieuart
            ├── mlanutl
            └── uaputl
```

☞ All kernel modules include a package name suffix, which is shown in the example above as `jody-w3-pcieuart`. The utilities and module files shown in this structure are for the PCIE-UART variant of the driver package. The structure for other packages will be similar. Refer to the Yocto recipes to learn more about the install path and names of the files.

3.6.1 Firmware

JODY-W3 series modules can be configured to download the firmware in two different modes:

- Parallel mode: Dedicated interfaces are used to download the firmware for Wi-Fi and Bluetooth radios separately.
- Serial mode: Wi-Fi host interface is used to download the combo firmware which is applicable to both the radios.

Table 26 shows the mapping between the various firmware images and their respective download modes.

Firmware image	Type of image	Download mode	Wi-Fi interface	Bluetooth interface
pcieuart9098_combo_v1.bin	Combo (Wi-Fi + Bluetooth)	Serial	PCIe	UART
pcie9098_wlan_v1.bin	Wi-Fi	Parallel	PCIe	-
uart9098_bt_v1.bin	Bluetooth	Parallel	-	UART
sd9098_wlan_v1.bin	Wi-Fi	Parallel	SDIO	-
sduart9098_combo_v1.bin	Combo (Wi-Fi + Bluetooth)	Serial	SDIO	UART

Table 26: Firmware images and their respective usage

⚠ JODY-W3 series modules must use firmware images that include the suffix "`_v1`" that denotes the A0/A1 revision of the 88Q9098/88W9098/AW690 chipset.

3.6.2 Configuration utilities

NXP driver package provides the source code for building various applications to configure the different modes and features of the module, including configuration of the firmware embedded supplicant and authenticator functions.

Application	Functionality
mlanutl	Features and configuration related to station mode in Wi-Fi
uaputl	Features and configuration related to AP mode in Wi-Fi

Table 27: Utilities to configure Wi-Fi modes

3.6.3 Additional software requirements

Although the NXP configuration utilities provide the necessary interface to configure features at granular levels, most product vendors prefer open-source applications and stacks. Some additional packages that are recommended for installation on the target system are shown in Table 28.

Package	Comment
bluez	Contains the user space parts of the Linux Bluetooth stack
wpa_supplicant	WPA supplicant. Handles key negotiation, like roaming on the client side.
iw	CLI configuration utility for wireless devices
hostapd	User space daemon for access point and authentication servers
crda	User space udev helper to handle regulatory domain

Table 28: Recommended additional software packages

3.7 Yocto meta layer

Yocto is an open-source project aimed at helping the development of custom Linux-based systems for embedded products. It provides a complete development environment with tools, documentation, and metadata like recipes, classes, and configuration. Yocto is based on the OpenEmbedded build system.

A Yocto/OpenEmbedded meta layer, "meta-ublox-modules", is provided by u-blox for all host-based modules. This layer is used in Yocto projects to build the image for most host platforms that run Linux kernels. It contains the recipes used to build the Linux drivers, support tools, and any configuration files that are needed to operate the modules. The recipes serve also as an integration example for other build environments.

Item	Description
Build recipe	Includes all the instructions to extract, compile and install the drivers, firmware and tools in the root file system of the host system image.
Patches	Used to fix bugs in ublox-distributed drivers seen either locally or reported by the vendor.
Calibration files	Calibration files, provided by u-blox, used while loading the driver. These files store the tuning parameters needed for RF parts present in the module, like the crystal.
Output power configuration	RF power specific files for the different bands, rates and countries are stored in configuration files provided by u-blox.
Modprobe rules	Configuration files for the modprobe utility used to store the driver load parameters.
Manufacturing package recipes	Includes different recipes for building the manufacturing tools. These recipes are used in production and RF-related tests.

Table 29: Content of the Yocto layer

☞ Calibration files are needed for the modules during the prototype stage of development. After prototyping, all required calibrations are programmed into the OTP on the module.

☞ Further information about the Yocto layer and how to integrate it into the development environment is provided in the `README` files of the meta layer.

3.8 Runtime usage

This section describes how to load specific drivers in different modes and configurations. It also provides examples for operating the module in several typical use-cases, such as station, access-point, and so on.

3.8.1 Device detection

Prior to loading the drivers, make sure that the JODY-W3 series module is detected by the host system.

☞ **PD#** must not be asserted to enable the JODY-W3 series module.

The `lspci` command lists connected PCIe devices in the system. The command output below shows two connected Ethernet controllers for the JODY-W3 series module. A single controller is listed for each of the two radio MACs.

```
$ lspci
01:00.0 Ethernet controller: Marvell Technology Group Ltd. Device 2b43 (rev 01)
01:00.1 Ethernet controller: Marvell Technology Group Ltd. Device 2b44 (rev 01)
```

When a JODY-W3 series module connects to the host system through the SDIO bus, the event is reported in the kernel log, as shown in the example below.

```
mmc1: new ultra high speed SDR104 SDIO card at address 0001
```

3.8.2 Driver and firmware loading

JODY-W3 series module supports parallel and serial options for downloading the Wi-Fi and Bluetooth radio firmware, as described in Firmware. Although the driver and firmware loading operation is different for each option, the normal Wi-Fi and Bluetooth operation is the same.

3.8.2.1 Serial mode

As shown in Table 26, the Wi-F interface is used to download Wi-Fi and Bluetooth combo images in serial mode. The firmware in these combo image includes the code for both the logical Wi-Fi and Bluetooth parts of the chip.

In the following example, the Wi-Fi driver modules `mlan.ko` and `moal.ko` are inserted into the Linux kernel to download the PCIE-UART combo image. Information about the loaded driver modules is then displayed using the `lsmod` command:

```
$ insmod mlan.ko
$ insmod moal.ko fw_name=nxp/pcieuart9098_combo_v1.bin cfg80211_wext=0xf auto_ds=2
   ps_mode=2
$ lsmod
Module                    Size    Used by
moal                      655360  0
cfg80211                  380928  1 moal
mlan                      499712  1 moal
```

The driver expects the firmware to be relative to the path `/lib/firmware`. Be sure to use the correct combo firmware image for the respective driver package. See also Table 26.

The following log example shows the firmware request and loading operation of the PCIe driver.

```
[  187.830477] mlan: loading out-of-tree module taints kernel.
[  187.995594] wlan: Loading MWLAN driver
[  188.000731] wlan_pcie 0000:01:00.0: enabling device (0000 -> 0002)
[  188.007113] Attach moal handle ops, card interface type: 0x206
[  188.012991] No module param cfg file specified
[  188.017477] rx_work=1 cpu_num=6
[  188.020672] Attach mlan adapter operations.card_type is 0x206.
[  188.033816] Request firmware: nxp/jody-w3-pcieuart/pcieuart9098_combo_v1.bin
[  188.706540] FW download over, size 661328 bytes
[  190.221805] WLAN FW is active
[  190.238578] VDLL image: len=138656
[  190.242184] fw_cap_info=0xc8fcffa3, dev_cap_mask=0xffffffff
[  190.247849] max_p2p_conn = 8, max_sta_conn = 64
[  190.290702] wlan: version = PCIE9098-17.68.1.p38-MXM4X17222.P1-GPL-(FP68)
[  190.302365] wlan_pcie 0000:01:00.1: enabling device (0000 -> 0002)
[  190.308754] Attach moal handle ops, card interface type: 0x206
[  190.314760] No module param cfg file specified
[  190.319228] rx_work=1 cpu_num=6
[  190.322577] Attach mlan adapter operations.card_type is 0x206.
[  190.349922] Request firmware: nxp/jody-w3-pcieuart/pcieuart9098_combo_v1.bin
[  190.358426] WLAN FW already running! Skip FW download
[  190.363722] WLAN FW is active
[  190.380792] VDLL image: len=138656
[  190.384298] fw_cap_info=0x68fcffa3, dev_cap_mask=0xffffffff
[  190.389942] max_p2p_conn = 8, max_sta_conn = 64
[  190.401149] wlan: version = PCIE9098-17.68.1.p38-MXM4X17222.P1-GPL-(FP68)
[  190.409893] wlan: Driver loaded successfully
```

After downloading the combo firmware using the Wi-Fi driver, it is not necessary to specify the Bluetooth firmware when loading the Bluetooth driver `hci_uart.ko`.

The `insmod` command below inserts the `hci_uart.ko` Bluetooth driver module into the Linux kernel, which is then used for Bluetooth communication over the UART host interface:

```
$ insmod hci_uart.ko
[  898.714631] HCI UART driver ver 2.2-M2614100
[  898.714670] HCI H4 protocol initialized
[  898.722842] HCI BCSP protocol initialized
```

☞ The `hci_uart.ko` kernel module is also distributed with the kernel sources, which means that `CONFIG_BT_HCIUART` option might already be enabled in the kernel. If this is the case, it is not possible to load the kernel module provided by NXP. To load the proprietary `hci_uart` module provided by NXP, the kernel configuration must set `CONFIG_BT_HCIUART=m` and not `CONFIG_BT_HCIUART=y`.

3.8.2.2 Parallel mode

In parallel mode, two different firmware binary images are used together with the respective driver. Set the driver parameter `fw_serial=0` to configure the download operation in parallel mode, as shown below for the SDIO Wi-Fi driver.

```
$ insmod mlan.ko
$ insmod moal.ko fw_name=nxp/sd9098_wlan_v1.bin cfg80211_wext=0xf auto_ds=2 ps_mode=2
  fw_serial=0
```

An example log of a successful SDIO driver loading and firmware download is shown below.

```
[   16.396004] wlan: Loading MWLAN driver
[   16.400727] vendor=0x02DF device=0x914D class=0 function=1
[   16.406453] Attach moal handle ops, card interface type: 0x106
[   16.424872] Attach mlan adapter operations.card_type is 0x106.
[   16.448778] Request firmware: mrvl/sd9098_wlan_v1_jody-w3-sdio.bin
[   16.750144] Wlan: FW download over, firmwarelen=593348 downloaded 487372
```

```
[   17.257260] WLAN FW is active
[   17.330706] wlan: version = SD9098---17.68.0.p159-MXM4X17153-GPL-(FP68)
[   17.337810] vendor=0x02DF device=0x914E class=0 function=2
[   17.358325] Attach moal handle ops, card interface type: 0x106
[   17.376908] Attach mlan adapter operations.card_type is 0x106.
[   17.426684] Request firmware: mrvl/sd9098_wlan_v1_jody-w3-sdio.bin
[   17.434397] WLAN FW already running! Skip FW download
[   17.440017] WLAN FW is active
[   17.482183] wlan: version = SD9098---17.68.0.p159-MXM4X17153-GPL-(FP68)
[   17.490179] wlan: Driver loaded successfully
```

To download the Bluetooth firmware over UART, we need the `fw_loader` application, built from the `uartfwloader_src` directory in the respective driver packages.

An example of a firmware download, showing all the parameters associated with the operation, is shown below. The initial baud rate is 115 200 baud, which is switched to 3 000 000 baud for the actual firmware download.

```
$ ./fw_loader /dev/ttyUSB0 115200 0 /lib/firmware/nxp/uart9098_bt_v1.bin 3000000

FW Loader Version: M317
ComPort : /dev/ttyUSB0
BaudRate: 115200
FlowControl: 0
Filename: /lib/firmware/nxp/uart9098_bt_v1.bin
Second BaudRate: 3000000

ChipID is : 5c01, Version is : 0
File downloaded:   150768:  150768
Download Complete
time:3018
CTS is low

$ insmod hci_uart.ko
[  208.037130] HCI UART driver ver 2.2-M2614100
[  208.037173] HCI H4 protocol initialized
[  208.045354] HCI BCSP protocol initialized
```

☞ Note the sequence. Firmware is downloaded first followed by the `hci_uart` driver.

☞ The example uses `/dev/ttyUSB0` as the serial device port. Replace it with the port to which the JODY-W3 series UART interface is connected on the host system.

3.8.3 Verification

3.8.3.1 Firmware version

The version of the loaded Wi-Fi driver and firmware can be verified using the following command:

```
$ mlanutl mlan0 version
Version string received: PCIE9098-17.68.1.p38-MXM4X17222.P1-GPL-(FP68)
```

3.8.3.2 Network interfaces

Use command `iw dev` to display the available Wi-Fi interfaces (excerpt):

```
phy#1
        Interface mwfd0
                addr 02:50:43:02:fe:02
                type managed
        Interface muap0
                addr 00:50:43:02:00:02
                type AP
        Interface mmlan0
                addr 00:50:43:02:fe:02
```

```
                type managed
phy#0
        Interface wfd0
                addr 02:50:43:02:fe:01
                type managed
        Interface uap0
                addr 00:50:43:02:00:01
                type AP
        Interface mlan0
                addr 00:50:43:02:fe:01
                type managed
```

Table 30 describes the functions of the Wi-Fi interfaces.

Interface	MAC/PHY	Function
mlan0	1	Network interface used for station mode functionality. Can be configured using mlanutl.
uap0	1	Network interface used for access-point functionality. Can be configured using uaputl.
wfd0	1	Network interface used for P2P functionality. Can operate in both group owner (GO) and group client (GC) modes.
mmlan0	2	Network interface used for station mode functionality. Can be configured using mlanutl.
muap0	2	Network interface used for access-point functionality. Can be configured using uaputl.
mwfd0	2	Network interface used for P2P functionality. Can operate in both group owner (GO) and group client (GC) modes.

Table 30: Available Wi-Fi network interfaces

☞ JODY-W3 series modules include two radios – 2.4 and 5 GHz – and two MACs for concurrent dual Wi-Fi use cases, where Wi-Fi interfaces from MAC 1 and 2 operate concurrently in different bands.

☞ The system/udev managers in modern Linux distributions automatically try to assign predictable, stable network interface names for all local Ethernet and Wi-Fi interfaces. This can result in different names being used for the network interfaces. Use the kernel command line option `net.ifnames=0` to override this behavior and use the driver default names.

3.8.4 Assigning MAC addresses

JODY-W3 series has four unique MAC addresses reserved for each module. The first MAC address is used for Bluetooth and the second and third addresses are used for the two Wi-Fi radio MACs. The fourth MAC address is reserved for use with other local interfaces.

Example

00:9C:38:00:4B:40 – Bluetooth interface (hci0)

00:9C:38:00:4B:41 – Wi-Fi station interface for radio MAC1 (mlan0)

00:9C:38:00:4B:42 – Wi-Fi station interface for radio MAC2 (mmlan0)

00:9C:38:00:4B:43 – Reserved for use with other interfaces

☞ The Wi-Fi driver automatically assigns locally unique MAC addresses to any additional Wi-Fi network interfaces, which are derived from the radio's primary Wi-Fi station interface MAC address. The use of reserved unique MAC addresses is recommended to avoid possible collisions with the MAC addresses of other modules.

You can change the MAC addresses of the interfaces by configuring the `init_cfg.conf` file while loading the driver. Note that the driver expects the `init_cfg.conf` file to be present in the directory relative to `/lib/firmware/`.

In the following example, the MAC addresses of the Wi-Fi interfaces have been changed in the `init_cfg.conf` file. The changes have been implemented to meet the application requirements so that each interface is assigned with a unique MAC address to avoid conflicts. The addresses are assigned to the uap0 and muap0 interfaces.

```
# File: /lib/firmware/nxp/init_cfg.conf
# MAC address (interface: address)
mac_addr=uap0: D4:CA:6E:00:1B:18
mac_addr=muap0: D4:CA:6E:00:1B:19

$ insmod moal.ko fw_name=nxp/pcieuart9098_combo_v1.bin cfg80211_wext=0xf auto_ds=2
   ps_mode=2 init_cfg=nxp/init_cfg.conf
```

3.8.5 Antenna configuration

The default antenna configuration after reset is to use 2x2 on both radios for 2.4 GHz and 5 GHz. Since JODY-W354 and JODY-W374 support only 1x1 for the 2.4 GHz radio on path A, the antenna configuration must be updated accordingly using the following commands:

```
mlanutl mlan0 antcfg 0x301        # set PHY#1 to path A+B for 5GHz and path A for 2.4GHz
mlanutl mmlan0 antcfg 0x301       # set PHY#2 to path A+B for 5GHz and path A for 2.4GHz
```

The same can be achieved by using the iw tool to configure the antennas:

```
iw phy mwiphy0 set antenna 0x301 # set PHY#1 to path A+B for 5GHz and path A for 2.4GHz
iw phy mwiphy1 set antenna 0x301 # set PHY#2 to path A+B for 5GHz and path A for 2.4GHz
```

3.8.6 Access point

3.8.6.1 Using hostapd

`hostapd`[15] is an open-source user space daemon for access point and authentication servers. 802.11ax configuration is supported with Linux kernel 5.x and hostapd 2.9.

The `hostapd` configuration file example below shows the parameters for 802.11ax operation in the 5 GHz band with 80 MHz channel width and WPA2 security:

```
# File: hostapd_ax5g.conf
interface=uap0
driver=nl80211
ctrl_interface=/var/run/hostapd
ctrl_interface_group=0
ieee80211d=1
country_code=US
beacon_int=100
dtim_period=1
wmm_enabled=1
uapsd_advertisement_enabled=1
ssid=JODY-W3-AX5G
ignore_broadcast_ssid=0
hw_mode=a
channel=36
auth_algs=1
max_num_sta=10
ieee80211n=1
require_ht=0
ht_capab=[LDPC][GF][SHORT-GI-20][SHORT-GI-40][TX-STBC][RX-STBC1][HT40+]
ieee80211ac=1
require_vht=0
vht_capab=[RXLDPC][SHORT-GI-80][SOUNDING-DIMENSION-2][BF-ANTENNA-4][TX-STBC-2BY1][RX-STBC-
   1][SU-BEAMFORMER][SU-BEAMFORMEE][MAX-A-MPDU-LEN-EXP7][RX-ANTENNA-PATTERN][TX-ANTENNA-
   PATTERN]
```

[15] https://w1.fi/hostapd/

```
vht_oper_chwidth=1
vht_oper_centr_freq_seg0_idx=42
ieee80211ax=1
he_su_beamformer=1
he_bss_color=1
he_oper_chwidth=1
he_oper_centr_freq_seg0_idx=42
eapol_version=1
wpa_key_mgmt=WPA-PSK
wpa=2
rsn_pairwise=CCMP
wpa_passphrase=1234567890
```

The access point is started with the command:

```
hostapd hostapd_ax5g.conf -B
```

☞ Use the command with the options `-dddt` to generate detailed log files for debugging purpose.

A hostapd configuration file example for 802.11ax operation in the 2.4 GHz band and WPA2 security is shown below.

```
# File: hostapd_ax2g.conf
interface=uap0
driver=nl80211
ctrl_interface=/var/run/hostapd
ctrl_interface_group=0
ieee80211d=1
country_code=US
beacon_int=100
dtim_period=1
wmm_enabled=1
uapsd_advertisement_enabled=1
ssid= JODY-W3-AX2G
ignore_broadcast_ssid=0
hw_mode=g
channel=11
auth_algs=1
max_num_sta=10
ieee80211n=1
require_ht=0
ht_capab=[LDPC][GF][SHORT-GI-20][TX-STBC][RX-STBC1][HT20]
ieee80211ac=0
ieee80211ax=1
he_su_beamformer=1
he_bss_color=1
eapol_version=1
wpa_key_mgmt=WPA-PSK
wpa=2
wpa_pairwise=CCMP
wpa_passphrase=1234567890
```

3.8.6.2 Using internal authenticator

Access point can be configured using the `uaputl` configuration tool provided by NXP. NXP firmware has internal authenticator functionalities that are used in this case.

In the following example, two concurrent access points are created. The first access point is configured for 802.11ax operation in the 5 GHz band using the uap0 interface. It uses an SSID value - "JODY-W3-5G" and the passphrase "12345678" for WPA2 based security. The second access point is configured for 802.11n in the 2.4 GHz band using the muap0 interface. It uses an SSID value - "JODY-W3-2G" and no security. The description of the individual commands is provided in the `README_UAP` file in the driver package.

The following commands set up the 5 GHz 802.11ax access point and the security mechanisms:

```
uaputl -i uap0 bss_stop
uaputl -i uap0 htstreamcfg 0x22
uaputl -i uap0 sys_cfg_rates 0x8c 0x98 0xb0 0x12 0x24 0x48 0x60 0x6c
uaputl -i uap0 sys_cfg_channel 44
# 20/40MHz, SGI, Rx LDPC, Rx STBC, GF, Tx STBC, MCS0-15
uaputl -i uap0 httxcfg 0x11ff
uaputl -i uap0 sys_cfg_11n 1 0x11ff 3 0 0xffff
# no beamformee
uaputl -i uap0 vhtcfg 2 3 1 0x338161B0 0xfffa 0xfffa
uaputl -i uap0 sys_cfg_ssid JODY-W3-5G
uaputl -i uap0 sys_cfg_auth 0
uaputl -i uap0 sys_cfg_protocol 32
uaputl -i uap0 sys_cfg_wpa_passphrase 12345678
uaputl -i uap0 sys_cfg_cipher 8 8
uaputl -i uap0 bss_start
```

The following commands set up the 2.4 GHz 802.11n access point:

```
uaputl -i muap0 bss_stop
uaputl -i muap0 sys_cfg_rates 0x82 0x84 0x8b 0x96 0x0C 0x12 0x18 0x24 0x30 0x48 0x60 0x6c
uaputl -i muap0 sys_cfg_channel 6
# 20/40MHz, SGI, Rx LDPC, Rx STBC, Tx STBC, MCS0-15
uaputl -i muap0 sys_cfg_11n 1 0x01ef 3 0 0xffff
uaputl -i muap0 sys_cfg_ssid JODY-W3-2G
uaputl -i muap0 sys_cfg_auth 0
uaputl -i muap0 sys_cfg_protocol 1
uaputl -i muap0 sys_cfg_cipher 0 0
uaputl -i muap0 bss_start
```

The following commands assign IP addresses to the two interfaces:

```
ifconfig uap0 192.168.1.1 up
ifconfig muap0 192.168.2.1 up
```

It is normally appropriate to run a DHCP server on the network interfaces to automatically assign IP addresses to the connected clients, as shown below for the uap0 interface:

```
# File: udhcpd.conf
interface uap0
start 192.168.1.10
end 192.168.1.200
option subnet 255.255.255.0
```

Command to start the DHCP server:

```
udhcpd udhcpd.conf
```

3.8.6.3 Configuration of 802.11ax for kernel 4.x

Additional configuration must be applied for Linux kernel 4.x to enforce 802.11ax operation before starting the access point. This is due to missing 802.11ax definitions in the 4.x kernel.

```
# File: config/11axcfg_80-2x2.conf
# Band config
[Band]
# band config, 1: 2.4G, 2: 5G
02
[/Band]
# HE Capability
[HECap]
# ID
ff 00
# Length
1a 00
```

```
# he capability id
23
# HE MAC capability info
00 00 00 82 00 08
# HE PHY capability info, first byte 04: 80MHz, 02: 20MHz
04 70 7e c9 fd 01 a0 0e 03 3d 00
# Tx Rx HE-MCS NSS support
fa ff fa ff
# PPE Thresholds (optional)
# PE: 16 us
e1 ff c7 71
[/HECap]
```

While starting the access point on 4.x kernel, use the following `mlanutl` command with respective configuration file before starting the access point:

```
mlanutl uap0 11axcfg config/11axcfg_80-2x2.conf
```

3.8.7 Station mode

3.8.7.1 Using wpa_supplicant

`wpa_supplicant`[16] is an open source WPA Supplicant that is used in the client stations for key negotiation with a WPA Authenticator. It also controls the roaming and authentication/association of the Wi-Fi driver. No additional external configuration is required to support 802.11ax operation.

Here are set of commands used to connect to an access point. Initially prepare the configuration file with some primitive settings:

```
$ cat > /etc/wpa_supplicant.conf << EOF
ctrl_interface=/var/run/wpa_supplicant
ctrl_interface_group=0
update_config=1
EOF
```

Set wireless network settings such as SSID `<ssid>` and the passphrase `<passphrase>`:

```
$ wpa_passphrase <ssid> <passphrase> >> /etc/wpa_supplicant.conf
```

Run the `wpa_supplicant` daemon:

```
$ wpa_supplicant -B -D nl80211 -i mlan0 -c /etc/wpa_supplicant.conf
```

☞ Use the command with the options `-dddt` to generate detailed log files for debugging purpose.

To acquire an IP address via DHCP:

```
$ udhcpc -i mlan0
```

3.8.7.2 Using internal supplicant

The following example shows how to connect to an access point using the `mlanutl` configuration tool provided by NXP . NXP firmware has internal supplicant functionalities that are used in this case.

To connect to an 802.11ax access point in the 5 GHz band with SSID `<ssid>` and passphrase `<passphrase>` and automatically assign an IP address via DHCP:

```
mlanutl mlan0 passphrase "1;ssid=<ssid>;passphrase=<passphrase>"
mlanutl mlan0 assocessid <ssid>
mlanutl mlan0 reassoctrl 1
udhcpc -i mlan0
```

[16] https://w1.fi/wpa_supplicant/

3.8.8 Bluetooth usage

☞ Once the Bluetooth drivers are loaded for the UART interface, it is necessary to bind the serial interface to the Bluetooth stack. For this, use the `hciattach` tool in the *BlueZ* package.

The following code snippet shows how to attach to *BlueZ* through the `/dev/ttyUSB0` serial device. In the example below, Bluetooth is connected to the host using USB cable connected through FTDI.

```
$ hciattach /dev/ttyUSB0 any 3000000 flow
[  442.667056] ps_init_work...
[  442.675963] ps_init_timer...
[  442.684716] ps_init...
[  442.816845] Bluetooth: BNEP (Ethernet Emulation) ver 1.3
[  442.825928] Bluetooth: BNEP socket layer initialized
[  443.234456] Bluetooth: RFCOMM TTY layer initialized
[  443.245865] Bluetooth: RFCOMM socket layer initialized
[  443.254362] Bluetooth: RFCOMM ver 1.11
Device setup complete
```

An HCI interface (shown here as `hci0`) is then available for further transactions.

```
$ hciconfig -a hci0 up
hci0:   Type: Primary  Bus: UART
        BD Address: D4:CA:6E:00:1B:16 ACL MTU: 1021:7  SCO MTU: 120:6
        UP RUNNING PSCAN
        RX bytes:918 acl:0 sco:0 events:62 errors:0
        TX bytes:1115 acl:0 sco:0 commands:62 errors:0
        Features: 0xff 0xfe 0x8f 0xfe 0xdb 0xff 0x7b 0x87
        Packet type: DM1 DM3 DM5 DH1 DH3 DH5 HV1 HV2 HV3
        Link policy: RSWITCH HOLD SNIFF
        Link mode: SLAVE ACCEPT
        Name: 'apalis-tk1'
        Class: 0x200000
        Service Classes: Audio
        Device Class: Miscellaneous,
        HCI Version: 5.0 (0x9)  Revision: 0x8300
        LMP Version: 5.0 (0x9)  Subversion: 0x10bc
```

A Bluetooth inquiry can be issued to scan for remote devices and verify that Bluetooth is working. L2CAP echo requests are used to ping the remote devices.

```
$ hcitool -i hci0 scan
Scanning ...
00:22:58:F8:86:BB ae-sho-bln-test
$ l2ping -i hci0 00:22:58:F8:86:BB
Ping: 00:22:58:F8:86:BB from 00:06:C6:46:DF:7B (data size 44) ...
4 bytes from 00:22:58:F8:86:BB id 0 time 69.75ms
4 bytes from 00:22:58:F8:86:BB id 1 time 56.76ms
[...]
```

3.8.8.1 Changing the UART baud rate

The vendor specific HCI command HCI_CMD_MARVELL_UART_BAUD can be used to switch to a different baud rate, for example to 3 000 000 baud, as shown in the following example. The `hciattach` tool needs to be restarted with the new baud rate.

```
$ hcitool -i hci0 cmd 0x3F 0x0009 0xC0 0xC6 0x2D 0x00
< HCI Command: ogf 0x3f, ocf 0x0009, plen 4
  C0 C6 2D 00
> HCI Event: 0x0e plen 4
  01 7A 0C 00
$ killall hciattach
$ hciattach /dev/ttyUSB0 any 3000000 flow
$ hciconfig hci0 up
```

3.9 Configuration of TX power limits and energy detection

3.9.1 Wi-Fi power table

The Wi-Fi TX power table defines the transmit power levels for the Wi-Fi radio. The power levels are based on regulatory compliance, IEEE 802.11 requirements, and product design constraints. The TX power table can be adjusted to achieve the highest transmit power level for each Wi-Fi channel, bandwidth, and modulation within the constraints defined by the certification.

⚠ The correct TX power limits must be applied to the module after startup of the host system and adjusted after some change of the regulatory domain or country specific requirements during runtime.

The Wi-Fi TX power levels are configured with the `txpwrlimit_2g_cfg_set` and `txpwrlimit_5g_cfg_set` data structures defined in the `txpwrlimit_cfg.conf` configuration file. The configuration file allows integrators to fine tune specific transmit power levels for the Wi-Fi radio, including:

- Band (2.4, 5 GHz)
- Channel
- Modulation rate (CCK, OFDM, HT, VHT, HE)
- Channel bandwidth (20, 40, 80 MHz)
- SISO (1x1) or MIMO (2x2) operation

☞ Transmit power limit configuration files are provided by u-blox for the certified regulatory domains accommodated in the available reference designs and Approved antennas. The configuration files for completed certifications are included in the Yocto meta layer.

An example of the `txpwrlimit_2g_cfg_set` structure for the 2.4 GHz band channels 2 and 3 is shown below:

```
## 2G Tx power limit CFG
txpwrlimit_2g_cfg_set={
        CmdCode=0x00fb           # do NOT change this line
        Action:2=1               # 1 - SET
        SubBand:2=0              # do NOT use this member in set cmd

        ChanTRPC.TlvType:2=0x0189
        ChanTRPC.TlvLength:2={
            TLVStartFreq:2=2407
            TLVChanWidth:1=20
            TLVChanNum:1=2

   TLVPwr:72='0,19,1,16,2,16,3,16,4,15,5,15,6,15,7,0,8,0,9,0,10,14,11,14,12,14,13,0,14,0,1
   5,0,16,14,17,0,18,0,19,0,20,0,21,0,22,13,23,0,24,0,25,0,26,0,27,0,28,15,29,14,30,0,31,0
   ,32,13,33,13,34,0,35,0'
        }

        ChanTRPC.TlvType:2=0x0189
        ChanTRPC.TlvLength:2={
            TLVStartFreq:2=2407
            TLVChanWidth:1=20
            TLVChanNum:1=3

   TLVPwr:72='0,19,1,17,2,17,3,16,4,16,5,16,6,16,7,13,8,13,9,13,10,15,11,15,12,15,13,12,14
   ,12,15,12,16,14,17,13,18,0,19,0,20,0,21,0,22,14,23,12,24,0,25,0,26,0,27,0,28,15,29,14,3
   0,13,31,0,32,14,33,14,34,12,35,0'
        }

        […]
}
```

The parameters inside `txpwrlimit_cfg.conf` are described in Table 31.

Parameter	Description
TLVType	Internal parameter set to 0x189. Do not change this value.

TLVStartFreq	• Starting frequency of the band for this channel
	  • 2407, 2414 or 2400 for 2.4 GHz
	  • 5000 for 5 GHz

TLVChanWidth	Channel bandwidth in MHz (20)
TLVChanNum	Logical 5 MHz channel number (1-255). Channel of the center frequency for HT40 operation in the 2.4 GHz band and primary channel for 40/80 MHz operation in 5 GHz.
TLVPwr:<Length>	Specifies the transmit power limits for specific modulations as a list with the length: <length> of (`ModulationGroup,Power`) tupels, where `ModulationGroup` specifies the mapping for the modulation. See also Table 32. `Power` specifies the Tx power limit at the module antenna pin in dBm. Note: For 5 GHz band, bonded channels (40, 80 MHz) must have the same Tx power.

Table 31: Parameters in `txpwrlimit_cfg.conf` file

The mapping of multiple wireless data rates into `ModulationGroup` values is shown in Table 32.

Modulation Group	Mode	Bandwidth [MHz]	Description	Notes on re-use for other modes
0	802.11b	20	CCK (1,2,5.5,11 Mbps)	
1	802.11g/a	20	OFDM (6,9,12,18 Mbps)	
2			OFDM (24,36 Mbps)	
3			OFDM (48,54 Mbps)	
4	802.11n	20	HT20 (MCS 0,1,2)	802.11ac/ax 20 MHz MCS 0-7
5			HT20 (MCS 3,4)	
6			HT20 (MCS 5,6,7)	
7		40	HT40 (MCS 0,1,2)	802.11ac/ax 40 MHz MCS 0-7
8			HT40 (MCS 3,4)	
9			HT40 (MCS 5,6,7)	
10	802.11n (2x2)	20	HT2_20 (MCS 8,9,10)	802.11ac/ax (2x2) 20 MHz MCS 0-7
11			HT2_20 (MCS 11,12)	
12			HT2_20 (MCS 13,14,15)	
13		40	HT2_40 (MCS 8,9,10)	802.11ac/ax (2x2) 40 MHz MCS 0-7
14			HT2_40 (MCS 11,12)	
15			HT2_40 (MCS 13,14,15)	
16	802.11ac	20	VHT_QAM256 (MCS 8)	
17		40	VHT_40_QAM256 (MCS 8,9)	802.11ax 40 MHz MCS 8,9
18		80	VHT_80_PSK (MCS 0,1,2)	802.11ax 80 MHz MCS 0-9
19			VHT_80_QAM16 (MCS 3,4)	
20			VHT_80_QAM64 (MCS 5,6,7)	
21			VHT_80_QAM256 (MCS 8,9)	
22	802.11ac (2x2)	20	VHT2_20_QAM256 (MCS 8,9)	
23		40	VHT2_40_QAM256 (MCS 8,9)	802.11ax (2x2) 40 MHz MCS 8,9
24		80	VHT2_80_PSK (MCS 0, 1, 2)	802.11ax (2x2) 80 MHz MCS 0-9
25			VHT2_80_QAM16 (MCS 3,4)	
26			VHT2_80_QAM64 (MCS 5,6,7)	
27			VHT2_80_QAM256 (MCS 8,9)	

Modulation Group	Mode	Bandwidth [MHz]	Description	Notes on re-use for other modes
28	802.11ax	20	HE_20_QAM256 (MCS 8,9)	
29			HE_20_QAM1024 (MCS 10,11)	
30		40	HE_40_QAM1024 (MCS 10,11)	
31		80	HE_80_QAM1024 (MCS 10,11)	
32	802.11ax (2x2)	20	HE2_20_QAM256 (MCS 8,9)	
33			HE2_20_QAM1024 (MCS 10,11)	
34		40	HE2_40_QAM1024 (MCS 10,11)	
35		80	HE2_80_QAM1024 (MCS 10,11)	

Table 32: ModulationGroup information

☞ For HT40 operation in the 2.4 GHz band, the TX power limits are selected from the channel of the center frequency. For example, the first 40 MHz channel at the center frequency 2422 MHz (20 MHz channels 1+5) uses the TX power limits from HT40 values of channel 3.

☞ For 40/80 MHz operation in the 5 GHz band, the same TX power limits must be specified for all bonded 20 MHz channels. For example, for the 40 MHz channel at the center frequency 5190 MHz, the 20 MHz channels 36 and 40 must have the same 40 MHz TX power limits.

An example of the `txpwrlimit_5g_cfg_set` structure for the 5 GHz channel 36 is shown below:

```
## 5G Tx power limit CFG
txpwrlimit_5g_cfg_set={
        CmdCode=0x00fb          # do NOT change this line
        Action:2=1              # 1 - SET
        SubBand:2=0             # do NOT use this member in set cmd

        ChanTRPC.TlvType:2=0x0189
        ChanTRPC.TlvLength:2={
            TLVStartFreq:2=5000
            TLVChanWidth:1=20
            TLVChanNum:1=36

   TLVPwr:72='0,0,1,16,2,16,3,16,4,14,5,14,6,14,7,13,8,13,9,13,10,14,11,14,12,14,13,12,14,
   12,15,12,16,14,17,13,18,12,19,12,20,12,21,12,22,14,23,12,24,11,25,11,26,11,27,11,28,14,
   29,13,30,13,31,12,32,14,33,13,34,12,35,11'
        }

        […]
}
```

The configuration file example above sets the following TX power limits for channel 36:

- 16 dBm for 802.11a rates
- 14 dBm for 20 MHz 802.11n/ac/ax SISO/MIMO rates, except 13 dBm for 802.11ax MCS10,11
- 13 dBm for 40 MHz 802.11n/ac/ax SISO rates
- 12 dBm for 40 MHz 802.11n/ac/ax MIMO rates
- 12 dBm for 80 MHz 802.11ac/ax SISO rates
- 11 dBm for 80 MHz 802.11ac/ax MIMO rates

For the exact power limits used in the u-blox reference design for the various certifications, see the Appendix: Wi-Fi Tx output power limits.

3.9.1.1 Applying the TX power limit configuration

The TX power configuration file `txpwrlimit_cfg.conf` must first be converted to a binary format before the Wi-Fi driver can use it. The following example command uses the `mlanutl` tool to create the binary file `txpower_US.bin` from the configuration file:

```
mlanutl mlan0 hostcmd txpwrlimit_cfg.conf generate_raw txpower_US.bin
```

To apply the TX power limit configuration when the driver is loaded, copy the binary file to the firmware directory and add the `txpwrlimit_cfg` parameter to the `insmod` driver load command, or in the `wifi_mod_para.conf` driver parameter configuration file as shown in the example below:

```
PCIE9098_0 = {
   […]
   fw_name=nxp/pcieuart9098_combo_v1.bin
   txpwrlimit_cfg=nxp/txpower_US.bin
}
```

The Wi-Fi driver can also be configured with the driver option `cntry_txpwr=1` to automatically load the corresponding binary TX power configuration file whenever the regulatory domain is changed. For this, the file name of the TX power files should be `txpower_XX.bin`, where “`XX`” is the ISO/IEC 3166 alpha2 country code. The files are expected to reside in the same folder as the firmware.

3.9.1.2 Reading the TX power limit configuration

The current TX power limit configuration can be read from the firmware using the `mlanutl` tool as shown below:

```
mlanutl mlan0 get_txpwrlimit <n> [raw_data_file]
   where <n>
      0:      Get 2.4G txpwrlimit table
      0x10:   Get 5G sub0 txpwrlimit table
      0x11:   Get 5G sub1 txpwrlimit table
      0x12    Get 5G sub2 txpwrlimit table
      0x1f    Get all 5G txpwrlimit table
      0xff    Get both 2G and 5G txpwrlimit table
   <raw_data_file> driver will save fw raw data to this file.
```

3.9.2 Bluetooth TX power levels

The vendor specific HCI command `HCI_CMD_UPDATE_TX_MAX_PWR_LVL` can be used to update the maximum transmit power level for Bluetooth BR/EDR, as shown in the following usage example:

```
# hcitool -i hci0 cmd 0x3F 0xEE 0x01 <signed TX power value in dBm>
# Example for setting max. TX power level to 10 dBm:
hcitool -i hci0 cmd 0x3F 0xEE 0x01 0x0A
hciconfig hci0 reset
```

☞ HCI reset is required after this command for the TX power change to take effect. Valid TX power level can be in the range of -20 to 12 dBm.

Bluetooth LE transmit power level can be set using the vendor specific HCI command `HCI_CMD_BLE_WRITE_TRANSMIT_POWER_LEVEL`, as shown in the following example:

```
# hcitool -i hci0 cmd 0x3F 0x87 <signed TX power value in dBm>
# Example for setting BLE TX power level to 10 dBm:
hcitool -i hci0 cmd 0x3F 0x87 0x0A
```

☞ Bluetooth LE TX power setting will be cleared with HCI reset. Valid TX power level can be in the range of -30 to 10 dBm.

3.9.3 Adaptivity configuration (energy detection)

JODY-W3 modules support the adaptivity requirements (energy detection) from EN 300 328 and EN 301 893 for Wi-Fi. The Energy Detect mechanism must be explicitly enabled after the startup of the module, and correct detection threshold values must be configured. These threshold values depend on the combined gain of the antenna and antenna trace used in the end-product.

Energy detection is enabled and threshold values are configured through a configuration file, as shown below:

```
## Set Energy Detect Threshold for EU Adaptivity test
ed_mac_ctrl_v2={
    CmdCode=0x0130                 # Command code, DO NOT change this line
    ed_ctrl_2g.enable:2=0x1        # 0 - disable EU adaptivity for 2.4GHz band
                                   # 1 - enable EU adaptivity for 2.4GHz band
    ed_ctrl_2g.offset:2=0x8        # Energy Detect threshold
                                   # offset value range: 0x80 to 0x7F
    ed_ctrl_5g.enable:2=0x1        # 0 - disable EU adaptivity for 5GHz band
                                   # 1 - enable EU adaptivity for 5GHz band
    ed_ctrl_5g.offset:2=0x8        # Energy Detect threshold
                                   # offset value range: 0x80 to 0x7F
    ed_ctrl_txq_lock:4=0x1e00FF    # DO NOT Change this line
}
```

The offset values `ed_ctrl_2g.offset` and `ed_ctrl_5g.offset` are used to adjust the energy detection thresholds during the EU adaptivity test. Increasing the values results in a more sensitive behavior to compensate for additional attenuation in the antenna path. Decreasing the values lowers the sensitivity.

The following command enables energy detection and configures the detection thresholds according to the settings in the `ed_mac_ctrl_V2.conf` configuration file:

```
mlanutl mlan0 hostcmd ed_mac_ctrl_V2.conf ed_mac_ctrl_v2
```

Alternatively, the configuration file can be converted to a binary format and loaded by the Wi-Fi driver. The following example command uses the `mlanutl` tool to create the binary file `ed_mac.bin` from the configuration file:

```
mlanutl mlan0 hostcmd ed_mac_ctrl_V2.conf generate_raw ed_mac.bin
```

To apply the energy detection configuration when the driver is loaded, copy the binary file to the firmware directory and add the `init_hostcmd` parameter to the `insmod` driver load command, or in the `wifi_mod_para.conf` driver parameter configuration file as shown in the example below:

```
PCIE9098_0 = {
   […]
   fw_name=nxp/pcieuart9098_combo_v1.bin
   init_hostcmd=nxp/ed_mac.bin
}
```

3.9.4 OFDMA resource unit TX power configuration for 802.11ax

This section describes how to configure the TX Power levels for UL-OFDMA that apply only for the 802.11ax modes. On the NXP chipset, the TX Power level of each resource unit (RU) type can be configured using the `rutxpower_limit.conf` config file. In this file, the TX Power level of each RU type is set on a "per channel" and "per channel width" basis, using the power type-length-value (`TlvPwr`) encoding parameters for 2.4 and 5 GHz bands in dBm.

Example 2.4 GHz band TX Power configuration structure:

```
rutxpowerlimit_cfg_set={
    CmdCode=0x026d          # do not change this line
    Action:2=1              # 1 - SET
    SubID:2=0x117           # RU POWER
    PwrVal.TlvType:2=0x0244
    PwrVal.TlvLength:2={
        TLVStartFreq:2=2407
        TlvChanWidth:1=20
        TlvChanNum:1=1
        TlvPwr:6='-1,2,5,8,0,0'
    }
    […]
}
```

The parameters inside `rutxpower_limit.conf` are described in Table 33.

Parameter	Description
TLVType	Internal parameter set to 0x0244. Do not change this value.
TLVStartFreq	Starting frequency of the band for this channel (2407 for 2.4 GHz, 5000 for 5 GHz)
TLVChanWidth	Channel width in MHz (20/40/80)
TLVChanNum	Channel number
TLVPwr:<Length>	Specifies the RU-based TX Power limit integer values (in dBm) range from -64 dBm to +63 dBm in steps of 1 dBm. The values should be given in the following format: `TlvPwr:6='<RU26_pwr_lvl>,<RU52_pwr_lvl>,<RU106_pwr_lvl>,<RU242_pwr_lvl>,<RU484_pwr_lvl>,<RU996_pwr_lvl>'`

Table 33: Parameters in rutxpower_limit.conf file

3.9.4.1 Loading the RU TX power configurations

Use the following commands to load the RU based TX Power level data to the firmware.

For 2.4 GHz RU TX Power levels update:

```
mlanutl mlan0 hostcmd rutxpower_limit.conf rutxpowerlimit_cfg_set
```

For 2.4 GHz RU TX Power levels update:

```
mlanutl mlan0 hostcmd rutxpower_limit.conf rutxpowerlimit_5g_cfg_set
```

3.10 Driver debugging

Driver debugging is provided through the kernel print function `printk` and the proc file system. Driver states are recorded and are retrieved through the proc file system during runtime.

The `printk` command output includes the following debug information files:

- `/proc/mwlan/config or /proc/net/mwlan/config`
- `/proc/mwlan/mlanX/info or /proc/net/mwlan/mlanX/info`
- `/proc/mwlan/mlanX/debug or /proc/net/mwlan/mlanX/debug`

☞ Note that the physical file location is dependent on the Linux kernel version.

☞ `mlanX` is the name of the device node created at runtime. Other file name possibilities include `uapX` and `wfdX` for the access point and Wi-Fi Direct interfaces respectively.

Debug messages are also printed to the kernel ring buffer through `printk` calls. These messages are accessed using the `/proc/kmsg` interface or by the `dmesg` command. Alternatively, this can also be handled by more advanced logging facilities.

3.10.1 Compile-time debug options

The extent to which the debug messages can be printed at runtime is controlled by the `CONFIG_DEBUG` variable in the driver `Makefile`. The `CONFIG_DEBUG` variable can have any of the following values:

- `n`: debug messages are disabled and not compiled into the driver module
- `1`: all kinds of debug messages can be configured except for `MENTRY`, `MWARN` and `MINFO`. By default, `MMSG`, `MFATAL` and `MERROR` are enabled.
- `2`: all kinds of debug messages can be configured

3.10.2 Runtime debug options

Once debugging is enabled in the `Makefile`, debug messages can be selectively enabled or disabled at runtime. Set or clear the corresponding bits of the `drvdbg` parameter accordingly:

```
bit 0:  MMSG           PRINTM(MMSG,...)
bit 1:  MFATAL         PRINTM(MFATAL,...)
bit 2:  MERROR         PRINTM(MERROR,...)
bit 3:  MDATA          PRINTM(MDATA,...)
bit 4:  MCMND          PRINTM(MCMND,...)
bit 5:  MEVENT         PRINTM(MEVENT,...)
bit 6:  MINTR          PRINTM(MINTR,...)
bit 7:  MIOCTL         PRINTM(MIOCTL,...)
...
bit 16: MDAT_D         PRINTM(MDAT_D,...), DBG_HEXDUMP(MDAT_D,...)
bit 17: MCMD_D         PRINTM(MCMD_D,...), DBG_HEXDUMP(MCMD_D,...)
bit 18: MEVT_D         PRINTM(MEVT_D,...), DBG_HEXDUMP(MEVT_D,...)
bit 19: MFW_D          PRINTM(MFW_D,...),  DBG_HEXDUMP(MFW_D,...)
bit 20: MIF_D          PRINTM(MIF_D,...),  DBG_HEXDUMP(MIF_D,...)
...
bit 28: MENTRY         PRINTM(MENTRY,...), ENTER(), LEAVE()
bit 29: MWARN          PRINTM(MWARN,...)
bit 30: MINFO          PRINTM(MINFO,...)
```

To change the value of the `drvdbg` parameter, give it as a module parameter when the driver is loaded, or write to the debug file in the proc file system, or set it using either the `iwpriv` or `mlanutl` tools.

```
iwpriv mlan0 drvdbg                             # Get the current driver debug mask
iwpriv mlan0 drvdbg 0                           # Disable all debug messages
echo "drvdbg=0x7" > /proc/mwlan/mlan0/debug     # enable MMSG, MFATAL and MERROR
mlanutl mlan0 drvdbg -1                         # Enable all debug messages
```

4 Handling and soldering

⚠ JODY-W3 series modules are Electrostatic Sensitive Devices that demand the observance of precautions against electrostatic discharge. Failure to observe precautions can result in severe damage to the product. Standard ESD safety practices must be applied.

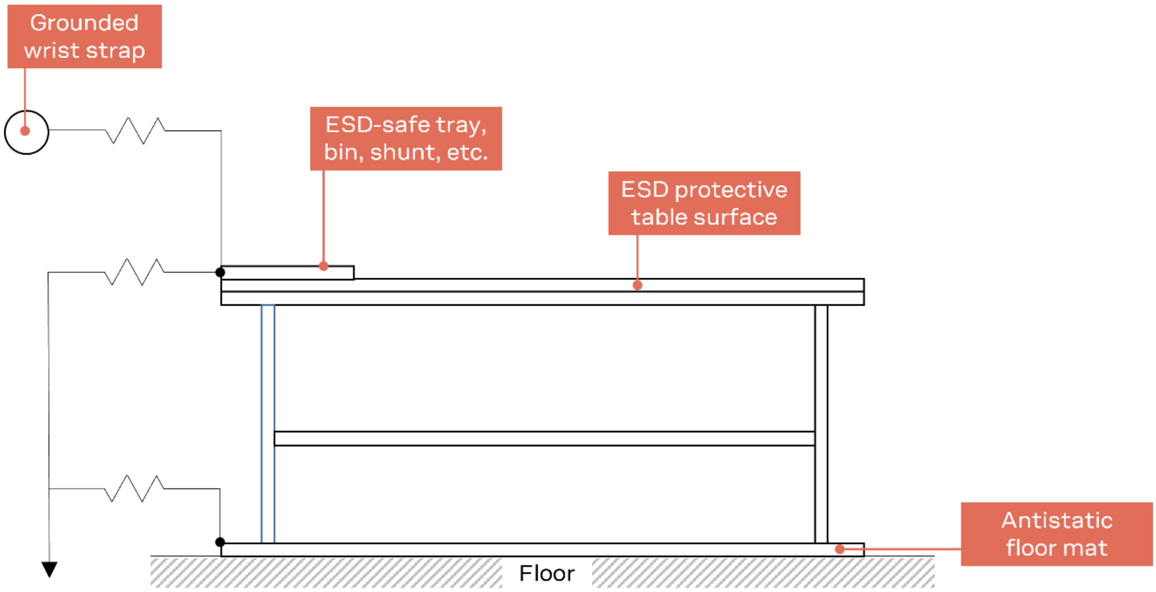

Figure 16: Standard workstation setup for safe handling of ESD-sensitive devices

4.1 Special ESD handling precautions

The risk of introducing electrostatic discharge in the RF transceiver through the RF pins is of special concern and the following bullets must carefully be observed:

- When connecting test equipment or any other electronics to the module (as a standalone or PCB-mounted device), the first point of contact must always be to local GND.
- Before mounting an antenna, connect the device to ground.
- When handling the RF pin, do not touch any charged capacitors. Be especially careful when handling materials like patch antennas (~10 pF), coaxial cables (~50-80 pF/m), soldering irons, or any other materials that can develop charges.
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk of the exposed antenna being touched in an unprotected ESD work area, be sure to implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the RF pin on the transceiver, be sure to use an ESD-safe soldering iron (tip).

4.2 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to reels, tapes, or trays, moisture sensitivity levels (MSL), storage, shipment, and drying preconditioning, see the JODY-W3 series modules data sheet [1] and Packaging information reference guide [2].

4.3 Reflow soldering process

JODY-W3 series modules are surface mounted devices supplied on a multi-layer FR4-type PCB with gold-plated connection pads. The modules are produced in a lead-free process using lead-free soldering paste. The thickness of solder resist between the host PCB top side and the bottom side of JODY-W3 series modules must be considered for the soldering process.

JODY-W3 series modules are compatible with industrial reflow profile for RoHS solders, and "no-clean" soldering paste is strongly recommended.

☞ JODY-W3 series modules comply to two reflow soldering cycles when mounted on a host board. For further information, contact your local support team.

The reflow profile used is dependent on the thermal mass of the entire populated PCB, the heat transfer efficiency of the oven, and the type of solder paste that is used. The optimal soldering profile must be trimmed for the specific process and PCB layout

⚠ The target values shown in Table 34 and Figure 17 are given as general guidelines for a Pb-free process only. For further information, see also the JEDEC J-STD-020E [7] standard.

Process parameter		Unit	Target
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_S (from 25°C)	s	150
	t_S (Pre-heat)	s	110
Peak	T_L	°C	217
	t_L (time above T_L)	s	90
	T_P (absolute max)	°C	260
	t_P (time above T_P -5°C)	s	30
Cooling	Ramp-down from T_L	K/s	6
General	$T_{to\ peak}$	s	300
	Allowed soldering cycles	-	2

Table 34: Recommended reflow profile

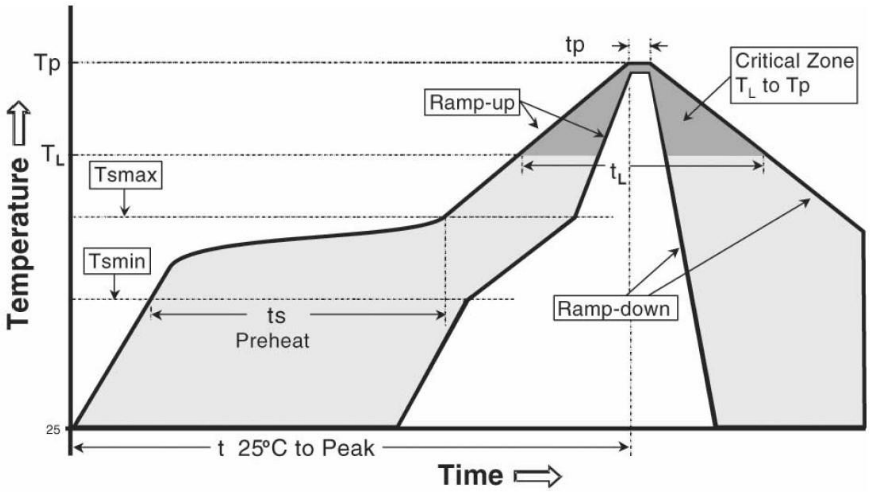

Figure 17: Reflow profile

☞ Lower value of T_P and slower ramp down rate is preferred.

4.3.1 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pins. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housing, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module and the crystal oscillators in particular.

For best results use a "no clean" soldering paste and circumvent the need for a cleaning stage after the soldering process.

4.3.2 Other notes

- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices may require wave soldering to solder the THT components. Only a single wave soldering process is allowed for boards populated with the modules. Miniature Wave Selective Solder process is preferred over traditional wave soldering process.
- Hand soldering is not recommended.
- Rework is not recommended.
- Conformal coating can affect the performance of the module, which means that it is important to prevent the liquid from flowing into the module. The RF shields do not provide protection for the module from coating liquids with low viscosity; therefore, care is required while applying the coating. Conformal Coating of the module will void the warranty.
- Grounding metal covers: Attempts to improve grounding by soldering ground cables, wick, or other forms of metal strips directly onto the EMI covers is done at the customer's own risk and voids the module warranty. The numerous ground pins are adequate to provide optimal immunity to interferences.
- The modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may damage the module. Use of ultrasonic processes during the integration of the module into an end product will void the warranty.

5 Regulatory compliance

5.1 General requirements

JODY-W3 series modules are designed to comply with the regulatory demands of Federal Communications Commission (FCC), Innovation, Science and Economic Development Canada (ISED)[17], UK Conformity Assessed (UKCA), Radio Equipment Directive (RED) 2014/53/EU and the CE mark. This section contains instructions on the process needed for an integrator when including the JODY-W3 module into an end-product.

- Any deviation from the process described may cause the JODY-W3 series module not to comply with the regulatory authorizations of the module and thus void the user's authority to operate the equipment.
- Any changes to hardware, hosts or co-location configuration may require new radiated emission and SAR evaluation and/or testing.
- The regulatory compliance of JODY-W3 does not exempt the end-product from being evaluated against applicable regulatory demands; for example, FCC Part 15B criteria for unintentional radiators [9].
- The end-product manufacturer must follow all the engineering and operating guidelines as specified by the grantee (u-blox).
- The JODY-W3 is for OEM integrators only.
- Only authorized antenna(s) may be used. Refer to JODY-W3 series data sheet [1] for the list of authorized antennas. In the end-product, the JODY-W3 module must be installed in such a way that only authorized antennas can be used.
- The end-product must use the specified antenna trace reference design, as described in the JODY-W3 antenna reference design application note [22].
- Any notification to the end user about how to install or remove the integrated radio module is NOT allowed.

⚠ If these conditions cannot be met or any of the operating instructions are violated, the u-blox regulatory authorization will be considered invalid. Under these circumstances, the integrator is responsible to re-evaluate the end-product including the JODY-W3 series module and obtain their own regulatory authorization, or u-blox may be able to support updates of the u-blox regulatory authorization. See also Antenna requirements.

5.2 European Union regulatory compliance

JODY-W3 series modules comply with the essential requirements and other relevant provisions of Radio Equipment Directive (RED) 2014/53/EU.

For information about the regulatory compliance of JODY-W3 series modules against requirements and provisions in the European Union, see the JODY-W3 series Declaration of Conformity [18].

5.2.1 CE End-product regulatory compliance

5.2.1.1 Safety standard

In order to fulfill the safety standard EN 60950-1 [8], the JODY-W3 module must be supplied with a Class-2 Limited Power Source.

[17] Formerly known as IC (Industry Canada).

5.2.1.2 CE Equipment classes

In accordance with Article 1 of Commission Decision 2000/299/EC[18], JODY-W3 is defined as either Class-1 or Class-2 radio equipment, the end-product integrating JODY-W3 inherits the equipment class of the module.

☞ Guidance on end product marking, according to the RED can be found at: http://ec.europa.eu/

⚠ The EIRP of the JODY-W3 module must not exceed the limits of the regulatory domain that the module operates in. Depending on the host platform's implementation and antenna gain, integrators have to limit the maximum output power of the module through the host software. See Approved antennas for the list of approved antennas and Wi-Fi transmit output power limits for the corresponding maximum transmit power levels.

5.2.2 Compliance with the RoHS directive

JODY-W3 series modules comply with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

5.3 Great Britain regulatory compliance

For information about the regulatory compliance of JODY-W3 series modules against requirements and provisions in Great Britain, see also the JODY-W3 UKCA Declaration of Conformity [17].

5.3.1 UK Conformity Assessed (UKCA)

☞ The United Kingdom is made up of the Great Britain (including England, Scotland, and Wales) and Northern Ireland. Northern Ireland continues to accept the CE marking. The following notice is applicable to Great Britain only.

JODY-W3 series modules have been evaluated against the essential requirements of the Radio Equipment Regulations 2017 (SI 2017 No. 1206, as amended by SI 2019 No. 696).

For guidance on end product marking in accordance with UKCA, see
https://www.gov.uk/guidance/using-the-ukca-marking.

5.4 United States/Canada end-product regulatory compliance

u-blox represents that the modular transmitter fulfills the FCC/ISED regulations when operating in authorized modes on any host product given that the integrator follows the instructions as described in this document. Accordingly, the host product manufacturer acknowledges that all host products referring to the FCC ID or ISED certification number of the modular transmitter and placed on the market by the host product manufacturer need to fulfil all of the requirements mentioned below. Non-compliance with these requirements may result in revocation of the FCC approval and removal of the host products from the market. These requirements correspond to questions featured in the FCC guidance for software security requirements for U-NII devices, FCC OET KDB 594280 D02 [16].

⚠ The modular transmitter approval of JODY-W3, or any other radio module, does not exempt the end product from being evaluated against applicable regulatory demands.

[18] 2000/299/EC: Commission Decision of 6 April 2000 establishing the initial classification of radio equipment and telecommunications terminal equipment and associated identifiers.

The evaluation of the end product shall be performed with the JODY-W3 module installed and operating in a way that reflects the intended end product use case. The upper frequency measurement range of the end product evaluation is the 10th harmonic of 5.8 GHz as described in KDB 996369 D04.

The following requirements apply to all products that integrate a radio module:

- Subpart B - UNINTENTIONAL RADIATORS
  To verify that the composite device of host and module comply with the requirements of FCC part 15B, the integrator shall perform sufficient measurements using ANSI 63.4-2014.
- Subpart C - INTENTIONAL RADIATORS
  It is required that the integrator carries out sufficient verification measurements using ANSI 63.10-2013 to validate that the fundamental and out of band emissions of the transmitter part of the composite device complies with the requirements of FCC part 15C.

When the items listed above are fulfilled, the end product manufacturer can use the authorization procedures as mentioned in Table 1 of 47 CFR Part 15.101, before marketing the end product. This means the customer has to either market the end product under a Suppliers Declaration of Conformity (SDoC) or to certify the product using an accredited test lab.

The description is a subset of the information found in applicable publications of FCC Office of Engineering and Technology (OET) Knowledge Database (KDB). We recommend the integrator to read the complete document of the referenced OET KDB’s.

- KDB 178919 D01 Permissive Change Policy
- KDB 447498 D01 General RF Exposure Guidance
- KDB 594280 D01 Configuration Control
- KDB 594280 D02 U-NII Device Security
- KDB 784748 D01 Labelling Part 15 18 Guidelines
- KDB 996369 D01 Module certification Guide
- KDB 996369 D02 Module Q&A
- KDB 996369 D04 Module Integration Guide

5.4.1 United States compliance statement (FCC)

Table 35 shows the FCC IDs allocated to JODY-W3 series modules.

Model[19]	FCC ID
JODY-W354-00A, JODY-W374-00A, JODY-W374-00B, JODY-W354-20A, JODY-W374-20A	XPYJODYW374
JODY-W377-00A, JODY-W377-00B	XPYJODYW377

Table 35: FCC IDs for different variants of JODY-W3 series modules

JODY-W3 series modules have modular approval and comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

⚠ Any changes or modifications NOT explicitly APPROVED by u-blox could cause the JODY-W3 series module to cease to comply with FCC rules part 15 thus void the user's authority to operate the equipment.

[19] The model name is identical to the ordering code. For details, see the JODY-W3 series data sheet [1].

The internal / external antenna(s) used for this module must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

For FCC end poduct labeling requirements, see End product labeling requirements.

5.4.2 Canada compliance statement (ISED)

JODY-W3 series modules are certified for use in accordance with the Canada Innovation, Science and Economic Development Canada (ISED) Radio Standards Specification (RSS) RSS-247 Issue 2 and RSS-Gen. Table 36 shows the ISED certification IDs allocated to JODY-W3 series modules.

Model	ISED certification ID
JODY-W354-00A, JODY-W374-00A, JODY-W374-00B, JODY-W354-20A, JODY-W374-20A	8595A-JODYW374
JODY-W377-00A, JODY-W377-00B	8595A-JODYW377

Table 36: ISED IDs for different variants of JODY-W3 series modules

JODY-W3 series complies with ISED (Innovation, Science and Economic Development Canada)[20] license-exempt RSSs. Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

☞ Any notification to the end user of installation or removal instructions about the integrated radio module is NOT allowed. Unauthorized modification could void authority to use this equipment.

This equipment complies with ISED RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

This radio transmitter IC: 8595A-JODYW374 / IC: 8595A-JODYW377 has been approved by ISED to operate with the antenna types listed in Approved antennas with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

☞ Operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

☞ Operation in the 5600-5650 MHz band is not allowed in Canada. High-power radars are allocated as primary users (i.e., priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

Le présent appareil est conforme aux CNR d'ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Cet équipement est conforme aux limites d'exposition de rayonnement d'ISED RSS-102 déterminées pour un environnement non contrôlé. Cet équipement devrait être installé et actionné avec la distance minimum 20 cm entre le radiateur et votre corps.

[20] Formerly known as IC (Industry Canada).

Cet émetteur radio, IC: 8595A-JODYW374 / IC: 8595A-JODYW377 été approuvé par ISED pour fonctionner avec les types d'antenne énumérés dans la section Approved antennas avec le gain maximum autorisé et l'impédance nécessaire pour chaque type d'antenne indiqué. Les types d'antenne ne figurant pas dans cette liste et ayant un gain supérieur au gain maximum indiqué pour ce type-là sont strictement interdits d'utilisation avec cet appareil.

☞ Le dispositif de fonctionnement dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur pour réduire le risque d'interférences nuisibles à la co-canal systèmes mobiles par satellite

☞ Opération dans la bande 5600-5650 MHz n'est pas autorisée au Canada. Haute puissance radars sont désignés comme utilisateurs principaux (c.-àutilisateurs prioritaires) des bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer des interférences et / ou des dommages à dispositifs LAN-EL.

The internal / external antenna(s) used for this module must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

For ISED end poduct labeling requirements, see End product labeling requirements.

☞ The approval type for all JODY-W3 series variants is a single modular approval. Due to ISED Modular Approval Requirements (Source: RSP-100 Issue 10), any application which includes the module must be approved by the module manufacturer (u-blox). The application manufacturer must provide design data for the review procedure.

5.4.3 Referring to the u-blox FCC/ISED certification ID

If the General requirements, FCC/ISED End-product regulatory compliance regulations, and all Antenna requirements are met, the u-blox modular FCC/ISED regulatory authorization is valid and the end-product may refer to the u-blox FCC ID and ISED certification number. u-blox may be able to support updates to the u-blox regulatory authorization; for example, adding new antennas to the u-blox authorization.

⚠ To use the u-blox FCC / ISED grant and refer to the u-blox FCC ID / ISED certification ID, the integrator must confirm with u-blox that all requirements associated with the Configuration control and software security of end-products are fulfilled.

5.4.4 Obtaining own FCC/ISED certification ID

Integrators who do not want to refer to the u-blox FCC/ISED certification ID, or who do not fulfil all requirements to do so may instead obtain their own certification. With their own certification, the integrator has full control of the grant to make changes.

Integrators who want to base their own certification on the u-blox certification can do so via a process called "Change in ID" (FCC) / "Multiple listing" (ISED). With this, the integrator becomes the grantee of a copy of the u-blox FCC/ISED certification. u-blox will support with an approval letter that shall be filed as a Cover Letter exhibit with the application.

☞ For modules where the FCC ID / ISED certification ID is printed on the label, the integrator must replace the module's label with a new label containing the new FCC/ISED ID. For more information about the labeling requirements, see also End product labeling requirements.

⚠ It is the responsibility of the integrator to comply with any upcoming regulatory requirements.

5.4.5 Antenna requirements

In addition to the general requirement to use only authorized antennas, the u-blox grant also requires a separation distance of at least 20 cm from the antenna(s) to all persons. The antenna(s) must not be co-located with any other antenna or transmitter (simultaneous transmission) as well. If this cannot be met, a Permissive Change as described below must be made to the grant.

☞ In order to support verification activities that may be required by certification laboratories, customers applying for Class-II Permissive changes must implement the setup described in the Radio test guide application note [12].

5.4.5.1 Separation distance

If the required separation distance of 20 cm cannot be fulfilled, a SAR evaluation must be performed. This consists of additional calculations and/or measurements. The result must be added to the grant file as a Class II Permissive Change.

5.4.5.2 Co-location (simultaneous transmission)

If the module is to be co-located with another transmitter, additional measurements for simultaneous transmission are required. The results must be added to the grant file as a Class II Permissive Change.

5.4.5.3 Adding a new antenna for authorization

If the authorized antennas and/or antenna trace design cannot be used, the new antenna and/or antenna trace designs must be added to the grant file. This is done by a Class I Permissive Change or a Class II Permissive Change, depending on the specific antenna and antenna trace design.

- Antennas of the same type and with less or same gain as those included in the list of Approved antennas can be added under a Class I Permissive Change.
- Antenna trace designs deviating from the u-blox reference design and new antenna types are added under a Class II Permissive Change.
- For 5 GHz modules, the combined minimum gain of antenna trace and antenna must be greater than 0 dBi to comply with DFS testing requirements.

⚠ Integrators with the intention to refer to the u-blox FCC ID / ISED certification ID must Contact their local support team to discuss the Permissive Change Process. Class II Permissive Changes will be subject to NRE costs.

5.4.6 Configuration control and software security of end-products

☞ “Modular transmitter” hereafter refers to JODY-W354, JODY-W374 (FCC ID XPYJODYW374), and JODY-W377 (FCC ID XPYJODYW377).

As the end-product must comply with the requirements addressed by the OET KDB 594280 [15], the host product integrating the JODY-W3 must comply with the following requirements:

- Upon request from u-blox, the host product manufacturer will provide all of the necessary information and documentation to demonstrate how the requirements listed below are met.
- The host product manufacturer will not modify the modular transmitter hardware.
- The configuration of the modular transmitter when installed into the host product must be within the authorization of the modular transmitter at all times and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host product. The Wi-Fi Tx output power limits must be followed. In particular, the modular transmitter installed in the host product will not have the capability to operate on the operating channels/frequencies referred to in the section(s) below, namely one or several of the following channels: 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz). The channels 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz) are allowed to be used only for modules that are certified for the usage (“modular transmitter”). Customers must verify that the module in use is certified as supporting DFS client/master functionality.
- The host product uses only authorized firmware images provided by u-blox and/or by the manufacturer of the RF chipset used inside the modular transmitter.
- The configuration of the modular transmitter must always follow the requirements specified in Operating frequencies and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host product.
- The modular transmitter must when installed into the host product have a regional setting that is compliant with authorized US modes and the host product is protected from being modified by third parties to configure unauthorized modes of operation for the modular transmitter, including the country code.
- The host product into which the modular transmitter is installed does not provide any interface for the installer to enter configuration parameters into the end product that exceeds those authorized.
- The host product into which the modular transmitter is installed does not provide any interface to third parties to upload any unauthorized firmware images into the modular transmitter and prevents third parties from making unauthorized changes to all or parts of the modular transmitter device driver software and configuration.

☞ The OET KDB 594280 D01 [15] lists the topics that must be addressed to ensure that the end-product specific host meets the Configuration Control requirements.

☞ The OET KDB 594280 D02 [16] lists the topics that must be addressed to ensure that the end-product specific host meets the Software Security Requirements for U-NII Devices.

5.4.7 Operating frequencies

JODY-W3 802.11b/g/n/ax operation outside the 2412–2462 MHz band is prohibited in the US and Canada and 802.11a/n/ac/ax operation in the 5600–5650 MHz band is prohibited in Canada. Configuration of the module to operate on channels 12–13 and 120–128 must be prevented accordingly. The channels allowed are described in Table 37.

Channel number	Channel center frequency [MHz]	Master device	Client device	Remarks
1 – 11	2412 – 2462	Yes	Yes	
12 – 13	2467 – 2472	No	No	
36 – 48	5180 – 5240	Yes	Yes	Canada (ISED): Devices are restricted to indoor operation only and the end product must be labelled accordingly.
52 – 64	5260 – 5320	No[21]	Yes	
100 – 116	5500 – 5580	No[21]	Yes	
120 – 128	5600 – 5640	No	No	USA (FCC): Client device operation allowed under KDB 905462
132 – 144	5660 – 5720	No[21]	Yes	
149 – 165	5745 – 5825	Yes	Yes	

Table 37: Allowed channel usage under FCC/ISED regulation

☞ 15.407 (j) Operator Filing Requirement:
Before deploying an aggregate total of more than one thousand outdoor access points within the 5.15–5.25 GHz band, parties must submit a letter to the Commission acknowledging that, should harmful interference to licensed services in this band occur, they will be required to take corrective action. Corrective actions may include reducing power, turning off devices, changing frequency bands, and/or further reducing power radiated in the vertical direction. This material shall be submitted to Laboratory Division, Office of Engineering and Technology, Federal Communications Commission, 7435 Oakland Mills Road, Columbia, MD 21046. Attn: U-NII Coordination, or via Web site at https://www.fcc.gov/labhelp with the subject line: “U-NII-1 Filing”.

5.4.8 End product labeling requirements

For an end-product using the JODY-W3, there must be a label containing, at least, the following information:

This device contains FCC ID: (XYZ)(UPN) IC: (CN)-(UPN)

(XYZ) represents the FCC "Grantee Code", this code may consist of Arabic numerals, capital letters, or other characters, the format for this code will be specified by the Commission's Office of Engineering and Technology[22]. (CN) is the Company Number registered at ISED. (UPN) is the Unique Product Number decided by the grant owner.

The label must be affixed on an exterior surface of the end product such that it will be visible upon inspection in compliance with the modular labeling requirements of OET KDB 784748. The host user manual must also contain clear instructions on how end users can find and/or access the FCC ID of the end product.

[21] DFS master certification is pending.
[22] 47 CFR 2.926

The label on the JODY-W3 module containing the original FCC/ISED ID acquired by u-blox can be replaced with a new label stating the end-product's FCC/ISED ID in compliance with the modular labeling requirements of OET KDB 784748.

FCC end product labeling

The outside of final products containing the JODY-W3 module must display in a user accessible area a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: XPYJODYW374" or "Contains FCC ID: XPYJODYW374".

In accordance with 47 CFR § 15.19, the end product shall bear the following statement in a conspicuous location on the device:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: This device may not cause harmful interference, and This device must accept any interference received, including interference that may cause undesired operation.

ISED end product labeling

The ISED certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host device must be labeled to display the ISED certification number for the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows: "Contains transmitter module IC: 8595A-JODYW374".

L'étiquette d'homologation d'ISED d'un module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette sur laquelle figure le numéro d'homologation du module d'ISED, précédé des mots « Contient un module d'émission », ou du mot « Contient », ou d'une formulation similaire allant dans le même sens et qui va comme suit : « Contient le module d'émission IC: 8595A-JODYW374».

The end product shall bear the following statement in both English and French in a conspicuous location on the device:

Operation is subject to the following two conditions: This device may not cause interference, and This device must accept any interference, including interference that may cause undesired operation of the device.

Son utilisation est soumise aux deux conditions suivantes: Cet appareil ne doit pas causer d'interférences et il doit accepter toutes interférences reçues, y compris celles susceptibles d'avoir des effets indésirables sur son fonctionnement.

Labels of end products capable to operate within the band 5150–5250 MHz shall also include:

For indoor use only

Pour usage intérieur seulement

When the end-product is so small or for such use that it is not practical to place the above FCC/ISED statements on it, the information shall be placed in a prominent location in the instruction manual or pamphlet supplied to the user or on the container in which the device is marketed. However, the FCC/ISED ID label must be displayed on the device.

If the end-product will be installed in locations where the end-user is not able to see the FCC/ISED ID and/or this statement, the FCC/ISED ID and the statement shall also be included in the end-product manual.

5.5 Approved antennas

Refer to the JODY-W3 antenna reference design application note [22] for the specifications that must be fulfilled in the end product that uses radio type approval of the JODY-W3 module. The JODY-W3 antenna reference design application note provides PCB layout details and electrical specifications.

For Bluetooth and Wi-Fi operation in the 2.4 GHz band and Wi-Fi operation in the 5 GHz band, JODY-W3 has been tested and approved for use with the antennas listed in Table 38.

Manufacturer	**Part number**	**Antenna type**	**Peak gain [dBi] / band**		**Validated regulatory domain**
			2.4 GHz	**5 GHz**	
TE connectivity	2195630-1 [19]	Dual-band dipole antenna	2.0	2.0	US/Canada (FCC/ISED)
TE connectivity	001-0009 [20]	Dual-band dipole antenna	2.0	2.0	US/Canada (FCC/ISED)
TE connectivity	001-0012 [21]	Dual-band dipole antenna	2.0	2.0	US/Canada (FCC/ISED)
-	-	-	0	0	EU/Great Britain (RED/UKCA)

Table 38: List of approved antennas

☞ No antennas have been used for RED/UKCA certifications. All radiated measurements were performed with 50 Ω terminations. The power limits in Wi-Fi transmit output power limits are valid for the antenna gains stated in Table 38.

⚠ For compliance with FCC §15.407(a), the EIRP is not allowed to exceed 125 mW (21 dBm) at any elevation angle above 30° (measured from the horizon) when operated as an outdoor access point in U-NII-1 band, 5.150-5.250 GHz.

6 Product testing

6.1 u-blox in-line production testing

As part of our focus on high quality products, u-blox maintain stringent quality controls throughout the production process. This means that all units in our manufacturing facilities are fully tested and that any identified defects are carefully analyzed to improve future production quality.

The Automatic test equipment (ATE) deployed in u-blox production lines logs all production and measurement data – from which a detailed test report for each unit can be generated. Figure 18 shows the ATE typically used during u-blox production.

u-blox in-line production testing includes:

- Digital self-tests (firmware download, MAC address programming)
- Measurement of voltages and currents
- Functional tests (host interface communication)
- Digital I/O tests
- Measurement and calibration of RF characteristics in all supported bands, including RSSI calibration, frequency tuning of reference clock, calibration of transmitter power levels, etc.
- Verification of Wi-Fi and Bluetooth RF characteristics after calibration, like modulation accuracy, power levels, and spectrum, are checked to ensure that all characteristics are within tolerance when the calibration parameters are applied.

Figure 18: Automatic test equipment for module test

6.2 OEM manufacturer production test

As all u-blox products undergo thorough in-line production testing prior to delivery, OEM manufacturers do not need to repeat any firmware tests or measurements that might otherwise be necessary to confirm RF performance. Testing over analog and digital interfaces is also unnecessary during an OEM production test.

OEM manufacturer testing should ideally focus on:

- Module assembly on the device; it should be verified that:
    - Soldering and handling process did not damage the module components
    - All module pins are well soldered on the customer application board
    - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
    - Communication with host controller can be established
    - The interfaces between module and device are working
    - Overall RF performance test of the device including antenna

In addition to this testing, OEMs can also perform other dedicated tests to check the device. For example, the measurement of module current consumption in a specified operating state can identify a short circuit if the test result deviates that from that taken against a “Golden Device”.

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and perform basic RF performance testing.

Appendix

A Reference schematic

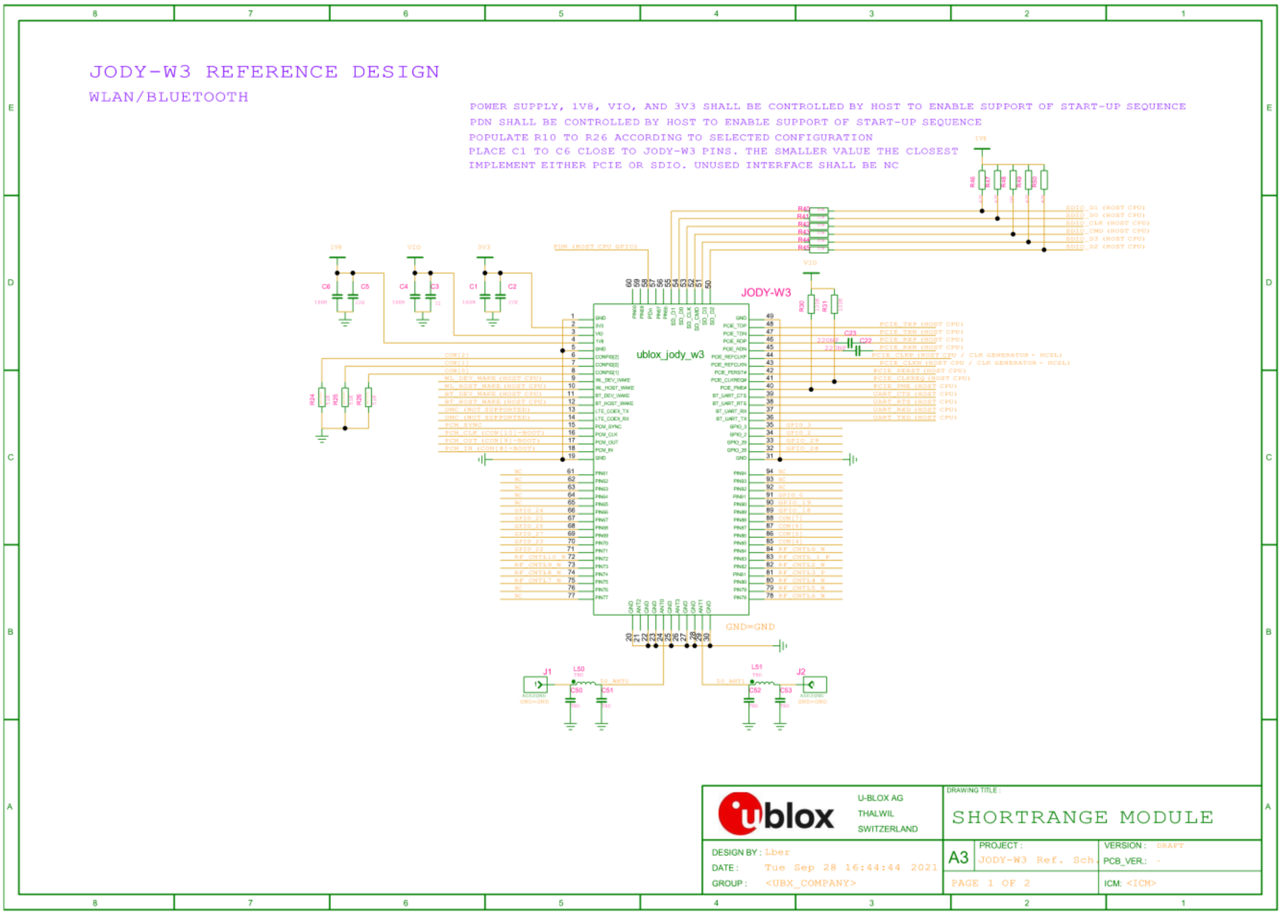

Figure 19: JODY-W3 reference schematic

B Wi-Fi transmit output power limits

B.1 FCC/ISED regulatory domain

Table 39 and Table 40 list the maximum allowable conducted output power limits for operation in the FCC/ISED regulatory domains. The output power limits are applicable with an external antenna gain of 2 dBi.

B.1.1 Wi-Fi output power for 2.4 GHz band

	TX power [dBm]									
	SISO (1x1)						MIMO (2x2)			
Channel	802.11b	802.11g	802.11n 20 MHz	802.11n 40 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11n 20 MHz	802.11n 40 MHz	802.11ax 20 MHz	802.11ax 40 MHz
1	19	14	14	n/a	13	n/a	13	n/a	12	n/a
2	21	16	15	n/a	15	n/a	14	n/a	13	n/a
3	21	17	16	13	15	13	15	12	14	12
4	21	17	17	13	16	13	15	12	15	12
5	21	17	17	13	17	13	15	12	16	12
6	21	17	17	13	17	13	15	12	16	12
7	21	17	17	13	17	12	15	12	16	11
8	21	17	17	13	17	12	15	12	16	11
9	21	16	16	12	16	12	15	11	14	11
10	16	15	14	n/a	14	n/a	13	n/a	13	n/a
11	16	13	12	n/a	12	n/a	12	n/a	11	n/a

Table 39: FCC / ISED Wi-Fi power table for operation in the 2.4 GHz band

B.1.2 Wi-Fi output power for 5 GHz band

	TX power [dBm]																
	SISO (1x1)									MIMO (2x2)							
Channel	802.11a	802.11n 20 MHz	802.11n 40 MHz	802.11ac 20 MHz	802.11ac 40 MHz	802.11ac 80 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11ax 80 MHz	802.11n 20 MHz	802.11n 40 MHz	802.11ac 20 MHz	802.11ac 40 MHz	802.11ac 80 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11ax 80 MHz
36	16	14	13	14	13	12	14	13	12	14	12	14	12	11	14	12	11
40	17	17	13	17	13	12	15	13	12	15	12	15	12	11	14	12	11
44	17	17	16	17	16	12	15	15	12	15	15	15	15	11	14	14	11
48	17	17	16	17	16	12	15	15	12	15	15	15	15	11	14	14	11
52	18	17	16	17	16	12	15	15	12	17	16	17	16	11	15	15	11
56	18	17	16	17	16	12	15	15	12	17	16	17	16	11	15	15	11
60	18	17	13	17	13	12	15	13	12	17	12	17	12	11	15	12	11
64	16	14	13	14	13	12	14	13	12	14	12	14	12	11	14	12	11
100	15	15	12	15	12	12	14	12	12	14	11	14	11	11	14	11	11
104	18	17	12	17	12	12	15	12	12	17	11	17	11	11	15	11	11
108	18	17	16	17	16	12	15	15	12	17	16	17	16	11	15	15	11
112	18	17	16	17	16	12	15	15	12	17	16	17	16	11	15	15	11
116	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
120	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
124	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
128	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
132	18	17	15	17	15	16	15	15	15	17	15	17	15	16	15	15	15
136	18	17	15	17	15	16	15	15	15	17	15	17	15	16	15	15	15
140	15	15	16	15	16	16	15	15	15	14	16	14	16	16	14	15	15
144	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
149	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
153	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
157	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
161	18	17	16	17	16	16	15	15	15	17	16	17	16	16	15	15	15
165	18	17	n/a	17	n/a	n/a	15	n/a	n/a	17	n/a	17	n/a	n/a	15	n/a	n/a

Table 40: FCC / ISED Wi-Fi power table for operation in the 5 GHz band

B.1.3 802.11ax OFDMA power limits

Worst case OFDMA with 26-tone RU

- 2.4 GHz FCC/ISED (SISO and MIMO)
  - 802.11ax 20 MHz: 9 dBm
  - 802.11ax 40 MHz: 6 dBm
- 5 GHz ISED (SISO and MIMO)
  - 802.11ax 20/40/80 MHz, channels 36 – 48: 5 dBm
  - 802.11ax 40 MHz channel 102, 802.11ax 80 MHz channel 106: 7 dBm
  - 802.11ax 20/40/80 MHz all other channels: 9 dBm

- 5 GHz FCC (SISO and MIMO):
  - 802.11ax 40/80 MHz channels 36 – 48: 8 dBm
  - 802.11ax 40 MHz channel 102, 802.11ax 80 MHz channel 106: 7 dBm
  - 802.11ax 20/40/80 MHz all other channels: 9 dBm

B.2 RED regulatory domain

Table 41 and Table 42 list the maximum allowable conducted output power limits for operation in the RED/UKCA regulatory domains. The output power limits are applicable with an external antenna gain of 0 dBi.

B.2.1 Wi-Fi output power for 2.4 GHz band

	TX power [dBm]									
	SISO (1x1)						MIMO (2x2)			
Channel(s)	802.11b	802.11g	802.11n 20 MHz	802.11n 40 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11n 20 MHz	802.11n 40 MHz	802.11ax 20 MHz	802.11ax 40 MHz
1 – 13	17	17	17	17	17	17	15	15	15	15

Table 41: RED Wi-Fi power table for operation in the 2.4 GHz band

B.2.2 Wi-Fi output power for 5 GHz band

	TX power [dBm]																
	SISO (1x1)									MIMO (2x2)							
Channel(s)	802.11a	802.11n 20 MHz	802.11n 40 MHz	802.11ac 20 MHz	802.11ac 40 MHz	802.11ac 80 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11ax 80 MHz	802.11n 20 MHz	802.11n 40 MHz	802.11ac 20 MHz	802.11ac 40 MHz	802.11ac 80 MHz	802.11ax 20 MHz	802.11ax 40 MHz	802.11ax 80 MHz
36 – 48	18	17	16	17	16	16	15	15	15	15	15	15	15	15	15	15	15
52 – 64	18	17	16	17	16	16	15	15	15	15	15	15	15	15	15	15	15
100 – 140	18	17	16	17	16	16	15	15	15	15	15	15	15	15	15	15	15
149 – 165	18	17	16	17	16	16	15	15	15	15	15	15	15	15	15	15	15

Table 42: RED Wi-Fi power table for operation in the 5 GHz band

B.2.3 802.11ax OFDMA power limits

Worst case OFDMA with 26-tone RU

- 2.4 GHz SISO/MIMO 802.11ax 20/40 MHz: 9 dBm
- 5 GHz SISO 802.11ax 20/40/80 MHz: 12 dBm
- 5 GHz MIMO 802.11ax 20/40/80 MHz: 9 dBm

C Glossary

Abbreviation	Definition
AEC	Automotive Electronics Council
AP	Access Point
API	Application Programming Interface
ATE	Automatic Test Equipment
BT	Bluetooth
CDM	Charged Device Model
CE	European Conformity
CLI	Command Line Interface
CTS	Clear to Send
DC	Direct Current
DDR	Double Data Rate
DFS	Dynamic Frequency Selection
DHCP	Dynamic Host Configuration Interface
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIRP	Equivalent Isotropic Radiated Power
ESD	Electro Static Discharge
FCC	Federal Communications Commission
GND	Ground
GPIO	General Purpose Input/Output
HBM	Human Body Model
HS	High-Speed
HCI	Host Controller Interface
ISED	Innovation, Science and Economic Development Canada
I2C	Inter-Integrated Circuit
KDB	Knowledge Database
LAN	Local Area Network
LDO	Low Drop Out
LED	Light-Emitting Diode
LPO	Low Power Oscillator
LTE	Long Term Evolution
MAC	Medium Access Control
MMC	Multi Media Card
MWS	Mobile Wireless Standards
NRE	Non-recurring engineering
NSMD	Non Solder Mask Defined
OEM	Original equipment manufacturer
OET	Office of Engineering and Technology
OFDMA	Orthogonal Frequency-Division Multiple Access
OS	Operating System
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express

Abbreviation	Definition
PCM	Pulse-code modulation
PHY	Physical layer (of the OSI model)
PMU	Power Management Unit
RF	Radio Frequency
RSDB	Real Simultaneous Dual Band
RST	Request to Send
SDIO	Secure Digital Input Output
SMD	Solder Mask Defined
SMPS	Switching Mode Power Supply
SMT	Surface-Mount Technology
SSID	Service Set Identifier
STA	Station
TBD	To be Decided
THT	Through-Hole Technology
UART	Universal Asynchronous Receiver-Transmitter
VCC	IC power-supply pin
VIO	Input offset voltage
VSDB	Virtual Simultaneous Dual Band
VSWR	Voltage Standing Wave Ratio
WFD	Wi-Fi Direct
WLAN	Wireless local area network
WPA	Wi-Fi Protected Access

Table 43: Explanation of the abbreviations and terms used

Related documents

[1] JODY-W3 series data sheet, UBX-19010615
[2] Product packaging guide, UBX-14001652
[3] u-blox Limited Use License Agreement, LULA-M
[4] IEC EN 61000-4-2 - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
[5] ETSI EN 301 489-1 - Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
[6] IEC61340-5-1 - Protection of electronic devices from electrostatic phenomena – General requirements
[7] JEDEC J-STD-020E - Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices
[8] ETSI EN 60950-1:2006 - Information technology equipment – Safety – Part 1: General requirements
[9] FCC Regulatory Information, Title 47 – Telecommunication
[10] JESD51 – Overview of methodology for thermal testing of single semiconductor devices
[11] Antenna Integration application note, UBX-18070466
[12] Radio test guide for NXP based modules, UBX-15014433
[13] Embedded Linux for i.MX Applications Processors
[14] NXP UM11490, Feature Configuration Guide for NXP-based Wireless Modules on i.MX 8M Quad EVK
[15] FCC guidance 594280 D01 Configuration Control v02 r01,
[16] FCC guidance 594280 D02 U-NII Device Security v01r03
[17] JODY-W3 UKCA Declaration of Conformity, UBX-22036490
[18] JODY-W3 EU declaration of conformity, UBX- 22018374
[19] 2195630-1, TE connectivity, Data Sheet
[20] 001-0009, TE connectivity, Data Sheet
[21] 001-0012, TE connectivity, Data Sheet
[22] JODY-W3 antenna reference design application note, UBX-22022630

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Revision history

Revision	Date	Name	Comments
R01	5-June-2020	lber, mzes	Initial release.
R02	26-Aug-2020	lber, mzes	Updated reference schematic in Appendix A. Fixed PCIe signal descriptions in Table 10.
R03	29-Jan-2021	lber, mzes	Added professional grade product variants JODY-W374 and JODY-W377. Updated pin list and descriptions in Table 4. Corrected configuration pins in Table 7. Added section 1.4.6 Sleep clock. Added GPIO usage in section 1.7.2. Marked SDIO-SDIO support pending. Updated section 3.8.4 with MAC address assignment.
R04	12-May-2021	lber	Peak current consumption updated in section 1.3.1 table 5. Configuration information updated in section 1.4.5 table 7. Power supply voltage ripple limits updated in section 1.3.1 table 5.
R05	29-Nov-2021	lber	HCSL voltage levels specified for PCIe_CLK added to table in PCIe interface. Reference schematic updated in Appendix A. Internal PU/PD information added in Configuration pins. Pad state in power down mode updated in the Pin list. Revised Handling and soldering and Product testing information. Thermal characteristic parameter value added in section 2.8.
R06	16-Feb-2022	mzes	Added automotive grade product variant JODY-W354. Revised block diagrams in Module architecture. Updated Bluetooth specification from 5.1 to 5.3. Removed product features section. Updated version in Open-source drivers. Removed SDIO-SDIO host interface combination.
R07	08-Aug-2022	lber, mzes	Updated Figure 3 and Table 2 to reflect changes in the module pinout and pinout assignments, namely: GPIO_12: added UART_DSRn/W_DISABLE2n alternate functions, GPIO_13: added UART_DTRn alternate function, GPIO_1/2/17/18/19: added PTA coex interface, GPIO_18: added independent software reset for Wi-Fi, GPIO_19: added independent software reset for Bluetooth, PCIE_RDN/RDP: added note about coupling capacitor, LPO_IN: Removed (DNC). Added information about coupling capacitors on PCIe_RDN and RDP, and added PTA information in the pin list. Revised description of power-off sequence and updated block diagrams in Module architecture. Added Coexistence interfaces section. Removed section 1.4.6 Sleep clock. Updated requirements for FCC/ISED End-product regulatory compliance and Configuration control and software security of end-products. Updated contact information.
R08	11-Oct-2022	lber	Included reference to module variants with dedicated LTE filter in Module architecture. Added Pre-approved antennas section.
R09	04-May-2023	lber, mzes	Power-up sequence with VIO =1.8 V added. Updated Reference schematic. Added module variants with dedicated LTE filter in Module architecture. Updated Open-source Linux/Android drivers. Added Configuration of TX power limits and energy detection and Wi-Fi transmit output power limits. Updated FCC/ISED Operating frequencies. Added Implementation details of PCIE_PERST# in PCIe interface. Restructured and rationalized the Regulatory compliance chapter (including content ported from the datasheet). Included corrections to ESD guidelines.

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