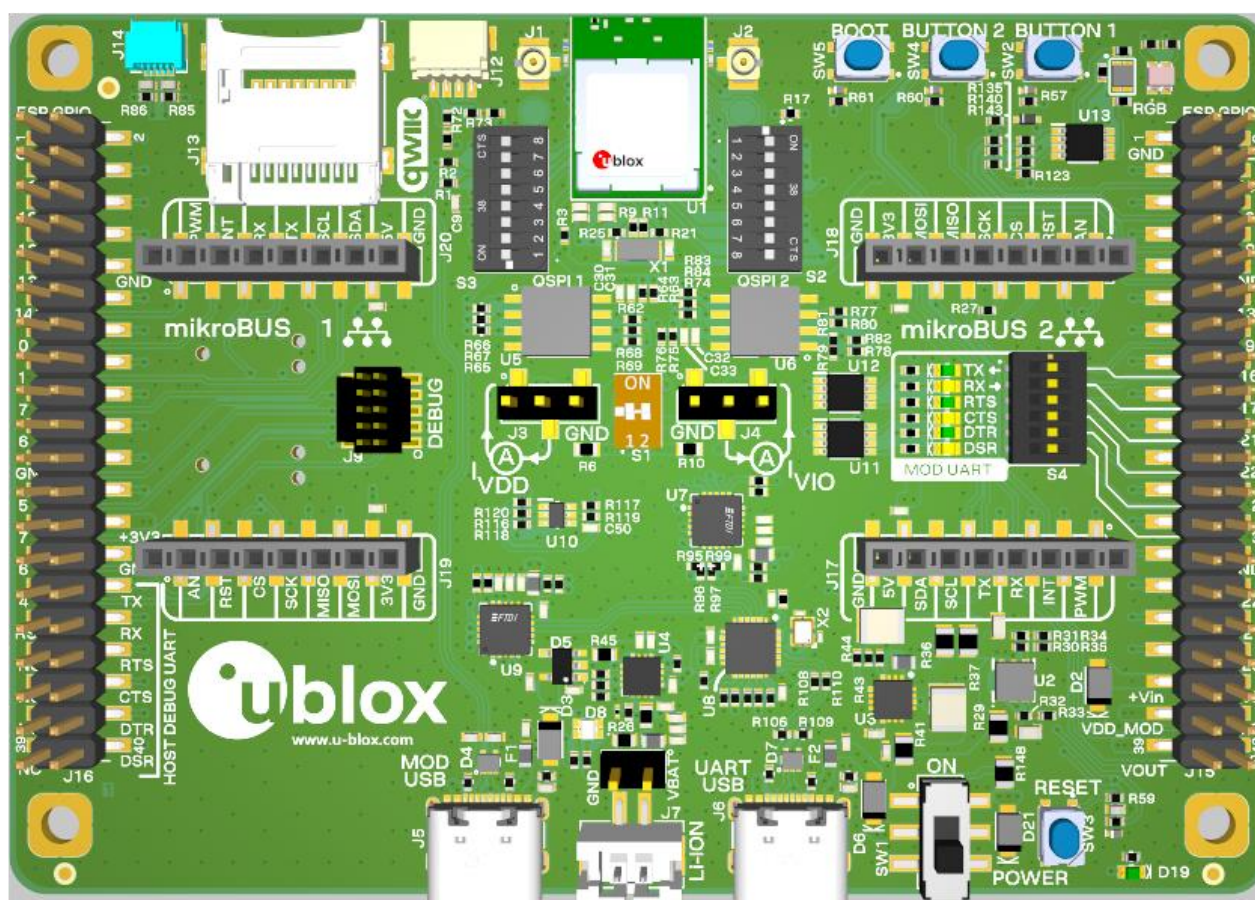


EVK-NORA-W40

Evaluation kit for NORA-W40 series modules

User guide



Abstract

The document describes how to set up and use the EVK-NORA-W401 and EVK-NORA-W406 evaluation kits for prototyping NORA-W40 open CPU, multiradio modules. It also describes the different options for debugging and the development capabilities included in the evaluation board.

Document information

Title	EVK-NORA-W40	
Subtitle	Evaluation kit for NORA-W40 series modules	
Document type	User guide	
Document number	UBXDOC-465451970-3360	
Revision and date	R01	19-Nov-2024
Disclosure restriction	C1-Public	

Product status	Corresponding content status	
In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production/ End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Document status
EVK-NORA-W401	Advance information
EVK-NORA-W406	Advance information

 For information about the hardware, software, and status of the available product types, see the NORA-W40 data sheet [\[1\]](#).

u-blox or third parties may hold intellectual property rights in the products, names, logos, and designs included in this document. Copying, reproduction, or modification of this document or any part thereof is only permitted with the express written permission of u-blox. Disclosure to third parties is permitted for clearly public documents only. The information contained herein is provided “as is” and u-blox assumes no liability for its use. No warranty, either express or implied, is given, including but not limited to, with respect to the accuracy, correctness, reliability, and fitness for a particular purpose of the information. This document may be revised by u-blox at any time without notice. For the most recent documents and product statuses, visit www.u-blox.com.
Copyright © u-blox AG

Contents

Document information	2
Contents	3
1 Product description	5
1.1 Overview	5
1.2 Kit includes	6
1.2.1 EVK-NORA-W401	6
1.2.2 EVK-NORA-W406	6
1.3 Key features	6
1.4 Block diagram	7
2 Setting up the evaluation board	8
2.1 Prerequisites	8
2.2 Setting up the evaluation board	8
2.2.1 Getting started	8
2.2.2 COM port assignment	8
2.3 Setting up the development environment	9
2.3.1 Installing ESP-IDF	9
2.3.2 Creating and flashing your first application	9
2.4 Measuring current consumption	10
2.4.1 Using an ammeter	10
2.4.2 Using a voltmeter	10
2.4.3 Using an external power supply or power analyzer	10
3 Hardware description	11
3.1 Connectors	11
3.2 Powering options	12
3.2.1 Default power configuration, 3.3 V	13
3.2.2 Battery powered, 3.7 V	13
3.2.3 External supply, 3.0 – 3.6 V	14
3.3 Switches, buttons and LEDs	15
3.3.1 Reset	15
3.3.2 Push buttons	16
3.3.3 DIP switches	16
3.3.4 LEDs	16
3.4 USB interfaces	17
3.4.1 COM USB interface	18
3.4.2 MOD USB interface	18
3.5 Interface DIP switch	19
3.5.1 Module power switch	20
3.5.2 GPIO DIP switch	20
3.5.3 UART DIP switch	21
3.6 Multipurpose GPIO header	22

3.7 mikroBUS interfaces	25
3.8 Other interfaces	28
3.8.1 Low frequency clock.....	28
3.8.2 JTAG debug interface.....	29
3.8.3 SPI interface	29
3.8.4 I2C / Qwiic	30
Appendix	31
A Schematics	31
B Assembly drawing	35
C Glossary	36
Related documentation	37
Revision history	37
Contact.....	37

1 Product description

EVK-NORA-W40 is designed for developers to explore and build custom applications for use with the NORA-W40 module, which integrates a Wi-Fi 6 multiradio CPU. As the modules are delivered without pre-flashed software, users must develop and deploy their own firmware using the kit.

NORA-W40 open CPU modules offer flexibility that allows users to leverage the Espressif ESP-IDF toolchain for development.

1.1 Overview

The EVK-NORA-W40 evaluation kit provides a versatile development platform for prototyping NORA-W40 stand-alone modules with a variety of low-powered Internet of Things (IoT) applications, using Wi-Fi 802.11b/g/n/ax in the 2.4 GHz ISM band, Bluetooth 5.3 (Low Energy), Zigbee and Thread (802.15.4).

Two EVK board variants accommodate alternative antenna and software solutions:

- EVK-NORA-W401 comes with an open CPU NORA-W401 module and U.FL antenna connector for connecting to external antennas.
- EVK-NORA-W406 comes with an open CPU NORA-W406 module that includes an internal, 2.4 GHz PCB Trace antenna.

All GPIOs supported on the NORA-W40 series modules are conveniently exposed and can be accessed through the various connectors and headers on the evaluation board, as shown in [Figure 1](#).

EVK-NORA-W40 supports two USB interfaces for programming, debugging, and communicating with the NORA-W4 module, both of which can be used to power the evaluation board. The board also supports mikroBUS Click add-on boards, GPIO, and Extended I2C interfaces, current measurement, and several configuration switches and buttons.

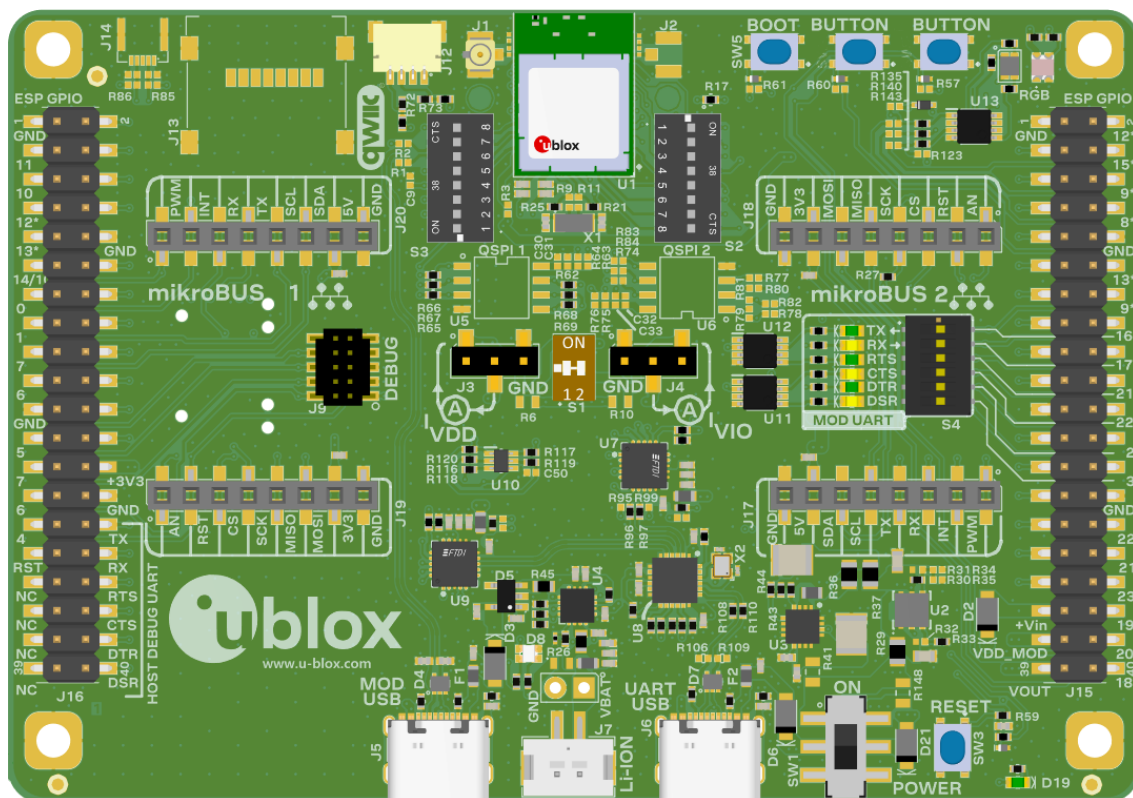


Figure 1: EVK-NORA-W40 evaluation board (top view)

1.2 Kit includes

1.2.1 EVK-NORA-W401

- EVK-NORA-W40 evaluation board with NORA-W401-10B module
- USB-A to USB-C adapter cable
- 2.4 GHz U.FL antenna

1.2.2 EVK-NORA-W406

- EVK-NORA-W40 evaluation board with NORA-W406-10B module
- USB-A to USB-C adapter cable
- A 2.4 GHz integrated antenna (external antenna not supplied)

1.3 Key features

NORA-W40 Open CPU modules:

- Based on SoC Espressif ESP32-C6 with support for 2.4GHz Wi-Fi 6 and Bluetooth® Low Energy, Zigbee 3.0 and Thread 1.3 (802.15.4):
- IEEE 802.11 b/g/n/ax protocol Wi-Fi subsystem.
- Bluetooth® LE subsystem supporting Bluetooth 5.3 and Bluetooth mesh.
- 32-bit HP RISC -V single core processor up to 160MHz operation.
- Memory 320KB ROM and 512 KB SRAM.
- 8 MByte FLASH (NORA-W40X-10B variant) for code storage, including hardware encryption to protect programs.
- Global certification

EVK-NORA-W40 evaluation kit:

- Evaluation board for NORA-W401 or NORA-W406 modules.
- 32.768 kHz crystal.
- COM ports and debug ports over USB connectors.
- 22 GPIOs accessible on pin headers and test points.
- Buttons and status LEDs for user interaction.
- 2x mikroBUS compatible pin socket interfaces.
- USB peripheral connector.
- Power input through USB-C or pin headers.
- Current measurement access points from pin headers and jumpers.
- Hardware interfaces:
 - 2 UARTs: The UART0 interface is already used to communicate via the USB connector with the module, so to avoid conflicts the UART0 shouldn't be used to communicate with other devices.
 - 1 Low-Power UART
 - SPI
 - I2C
 - I2S
 - USB 2.0 full speed (OTG + serial/JTAG controller)

1.4 Block diagram

Figure 2 shows the major interfaces and internal connections supported on EVK-NORA-W40.

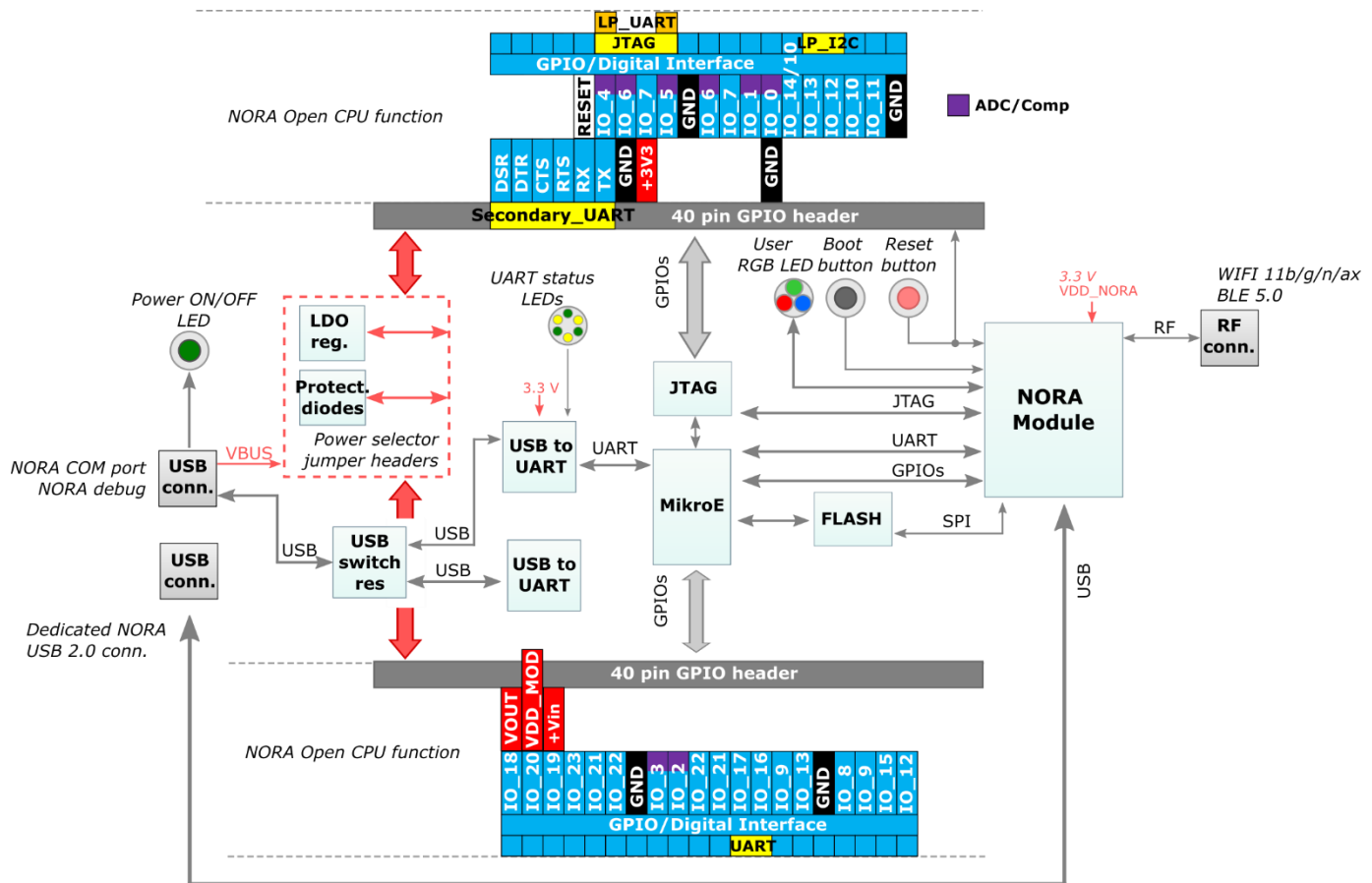


Figure 2: EVK-NORA-W40 block diagram

2 Setting up the evaluation board

The EVK-NORA-W40 is delivered without any software (open CPU) and the software must be developed by the user. The following EVK variants are available:

- [EVK-NORA-W401](#)
- [EVK-NORA-W406](#)

2.1 Prerequisites

- Windows, macOS or Linux computer
- EVK-NORA-W40
- USB cable to connect the EVK-NORA-W40 to the computer.
- Espressif IoT Development Framework (ESP-IDF) version 5.1 or up.

2.2 Setting up the evaluation board

-  Before powering up the EVK-NORA-W401, be sure to connect the 2.4 GHz antenna to the U.FL antenna connector (J1). Failure to do so can cause module malfunction.
-  Note that the inrush current when powering-up the EVK can be significantly higher than it is during normal operation.

2.2.1 Getting started

To start the EVK-NORA-W40 evaluation board:

1. Connect the EVK-NORA-W40 to your computer using a USB cable. The kit should automatically be recognized as a serial device. Typically, it appears as COM port COM_{xx} on Windows or /dev/ttyUSB_x on Linux and macOS. See also [COM port assignment](#).
2. EVK-NORA-W406 only: Connect the 2.4 GHz antenna to the U.FL antenna connector (J1).
3. Connect the external power supply to the EVK, as described in [Connectors](#).
4. The green status LED (D19) is lit when the internal EVK 3.3 V supply is active.
5. Check the [COM port assignment](#).

2.2.2 COM port assignment

The operating system installs the correct COM port drivers automatically. The drivers need to be installed only when you connect the unit to a new computer for the first time. For more information about the COM ports and their configuration, see the FTDI FT231XQ-R Datasheet [\[3\]](#).

Windows OS automatically assigns one COM port to the unit.

To view the assigned COM ports on Windows 10:

1. Open the Control Panel and select **Hardware and Sound**.
2. Click **Device Manager** in **Devices and Printers**. This opens the Device Manager window where you can view the assigned COM ports.

2.3 Setting up the development environment

NORA-W40 open CPU modules are used for developing custom software based on the Espressif IoT Development Framework (ESP-IDF). As the NORA-W40 is built on the Espressif ESP32 architecture, you must use this framework to develop your application. This development environment provides an integrated SDK and API for application development.

Follow this workflow to set up the development environment:

- [Install ESP-IDF](#)
- [Connect EVK-NORA-W40](#)
- [Create and flash your first application](#)

2.3.1 Installing ESP-IDF

The open-source ESP-IDF provides the essential toolchain, libraries, and APIs for developing the ESP32-based modules. To install all the necessary components, follow the instructions in the ESP-IDF Programming Guide [7].

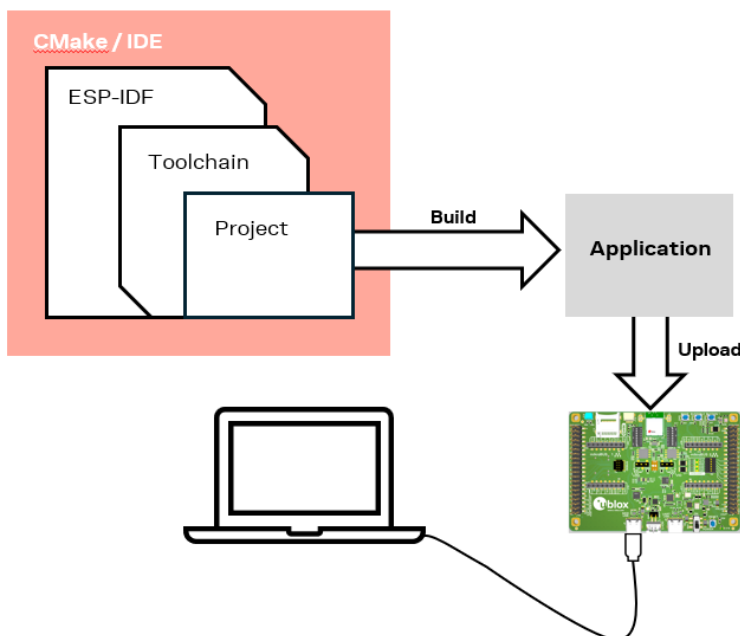


Figure 3: NORA-W40 configuration in ESP-IDF application development

Once the ESP-IDF is installed, you'll need to configure it to work with the NORA-W40, as described in the ESP-IDF Programming Guide [7]. When accessing this document, be sure to select the *ESP32-C6* chipset.

2.3.2 Creating and flashing your first application

To create and flash an application to EVB-NORA-W4:

1. Launch the ESP-IDF environment, as described in the ESP-IDF Programming Guide [7].
2. Create a new project using one of the available examples, such as the "Hello World" or one of the available pre-configured ITWT (Individual Target Wake Time) projects, which include a ready-to-use code base for developing applications for utilizing power-saving wake-up schedules in Wi-Fi communication.
3. Compile the application and flash it to the EVK-NORA-W40 via the ESP-IDF CLI. Espressif recommend using the Eclipse IDE or Visual Studio (VS) code, since the Eclipse IDE has a plugin and VS code has an extension for installing ESP-IDF.

2.4 Measuring current consumption

You use pin headers J3 and J4 to measure current consumption on the NORA-W40 power supply pins.

2.4.1 Using an ammeter

To measure current, connect an ammeter in series between the power source and the device being measured. In this way, the current can be measured when the NORA module is supplied from either the onboard 3.3 V regulator or an external supply.

Figure 4 shows the connection pattern of ammeter at jumper J3 and J4. Make sure to turn off switch S1.

2.4.2 Using a voltmeter

The EVK board must be modified before the module current can be measured with a voltmeter.

To modify the board, solder a low resistance, high tolerance, 0603 sized resistor to the footprint labeled R6 and R10. This resistor replaces the jumpers, and any current running through it produces a voltage drop across its terminals. Measure this voltage with the voltmeter and calculate the current using Ohm's law.

Figure 4 shows the connection pattern of voltmeter at jumper J3 and J4. Be sure to turn off the switch S1.

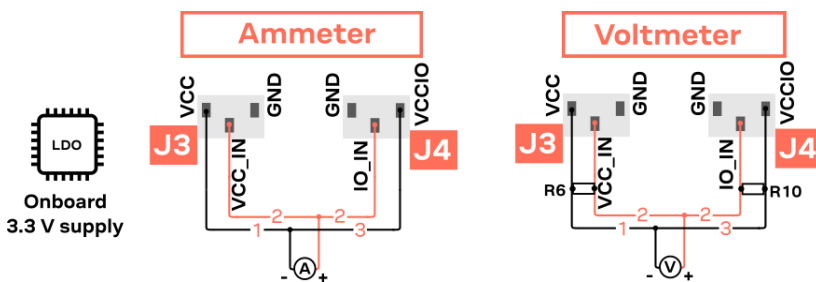


Figure 4: Measuring module current consumption with an ammeter and voltmeter

2.4.3 Using an external power supply or power analyzer

Connect the terminals of the instrument to the EVK pins, as shown in Figure 5. An ammeter can also be added in-series.

Since the external voltage of any connected instrument can never perfectly match the 3.3 V generated by the EVK, some small current leakage is apparent whenever the signal from the NORA module is connected to an EVK peripheral. The leakage is typically in the order of 100's of nano amps.

To reduce leakage current, use a second external power channel to supply EVK peripherals. This second channel must also be used to enable PC communication when using NORA supply voltages other than 3.3 V.

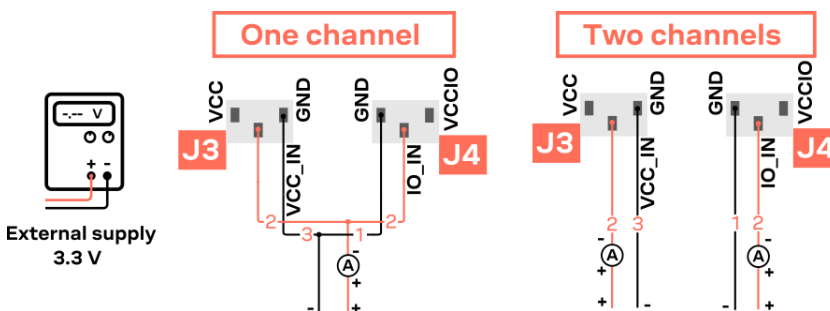


Figure 5: Measuring module current consumption using power analyzer

3 Hardware description

Design files for the EVK-NORA-W40 PCB are available from your local [u-blox support team](#).

3.1 Connectors

EVK-NORA-W40 is equipped with several connectors for power (J5-J8) and antenna (J10) connections, current measurement (J3-J4), various I/O interfaces for mikroBUS Click add-on boards (J17-J20), flash and debug ports (J9), multi-purpose GPIOs (J15-J16), and extended I2C communication (J12).

Figure 6 shows the location and function of each connector on the board.

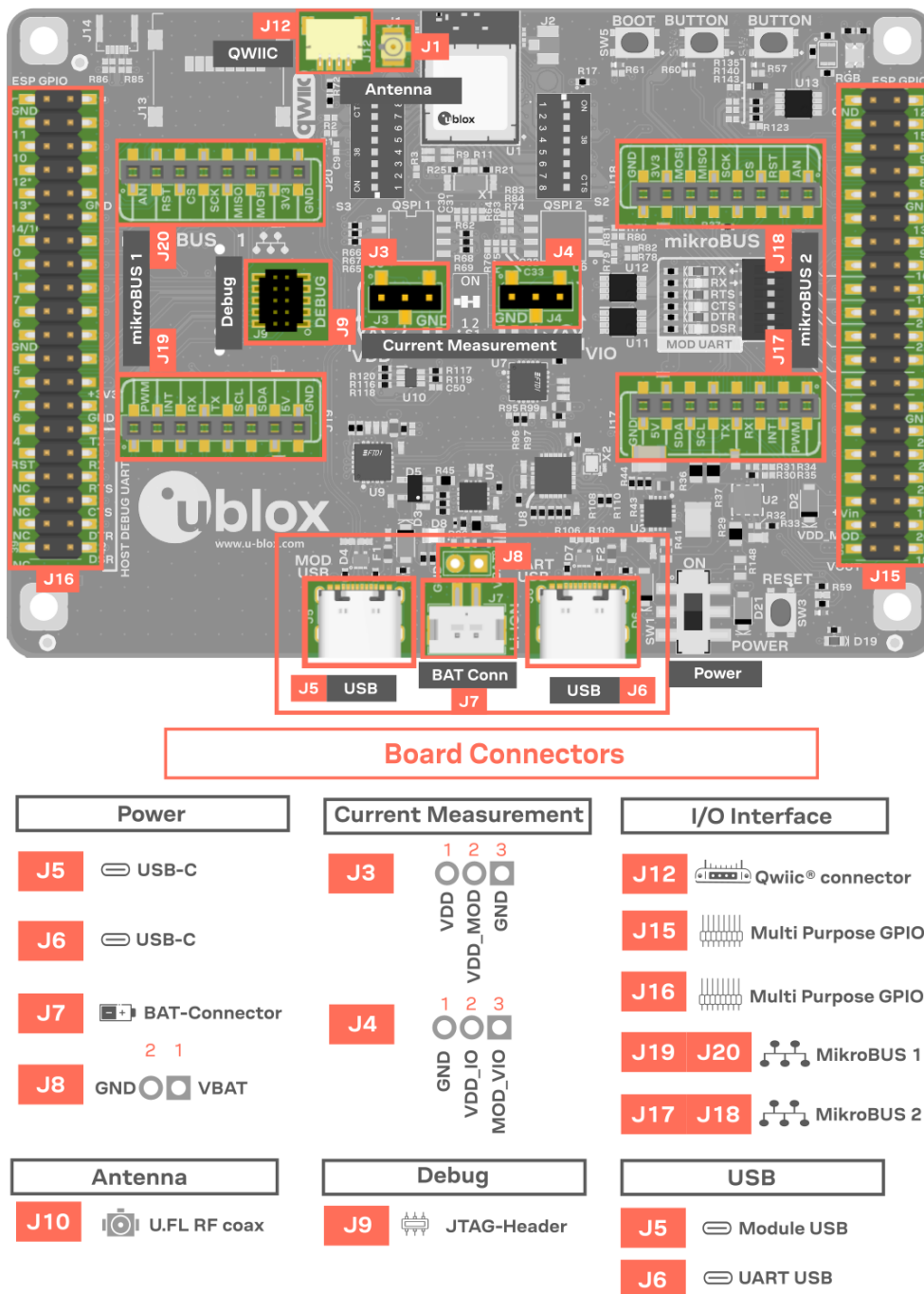


Figure 6: Available connectors and their pinout

Table 1 describes the available connectors of the EVK-NORA-W40.

Connector	Function	Description
(J1)	2.4 GHz RF antenna connector	U.FL coaxial connector that can be used to connect antennas or RF equipment. This connector is only included in the EVK-NORA-W401.
J3	Current consumption header	Pin header that can be used to measure the current consumption across the input voltage (VCC) for NORA-W4 module.
J4	Current consumption header	Pin header that can be used to measure the current consumption across I/O voltage (VCCIO) for NORA-W4 module.
J5	Power supply, COM port and debug USB	The main USB connector is used to program, debug, and communicate with the NORA-W4 module. It is the primary connector to power the entire board.
J6	Power supply and NORA USB port	An additional USB connector directly connected to the NORA-W4 USB interface. It can also be used to power the entire board.
J7	Li-Ion battery connector	2-pin JST Li-Ion battery connector. Can be used to supply power with 3.7V Li-Ion rechargeable battery.
(J8)	Generic 2-pin header	2.54mm 2-pin header position. Can be used to connect a battery without a standard JST connector. This connector is not mounted by default.
J9	Cortex Debug connector	10-pin, 50 mil pitch connector that can be used to connect external debuggers to the NORA module. The NORA-W4 module supports JTAG debug interface.
J12	QWIIC connector	4-pin connector compatible with the Qwiic connect system defined by SparkFun Electronics for extending I2C interface.
J15	Generic 40-pin header	2.54 mm 40-pin header, connected to multi-purpose GPIOs of NORA-W4 module.
J16	Generic 40-pin header	2.54 mm 40-pin header, connected to multi-purpose GPIOs of NORA-W4 module.
J17, J18	mikroBUS™ connector	mikroBUS socket 2 allows NORA-W4 module to host mikroBUS add-on boards.
J19, J20	mikroBUS™ connector	mikroBUS socket 1 allows NORA-W4 module to host mikroBUS add-on boards.

Table 1: EVK-NORA-B4 connector description

3.2 Powering options

EVK-NORA-W40 can be powered through either:

- USB connectors (J5 or J6).
- 5 V pin, J15.39 (J15 pin 39).
- 3 V pins on J15.35 and J16.26 pin headers (J15 pin 35 and J16 pin 26)
- Battery connection (J7 or J8).

These power supply sources are distributed to the rest of the board as shown [Figure 7](#).

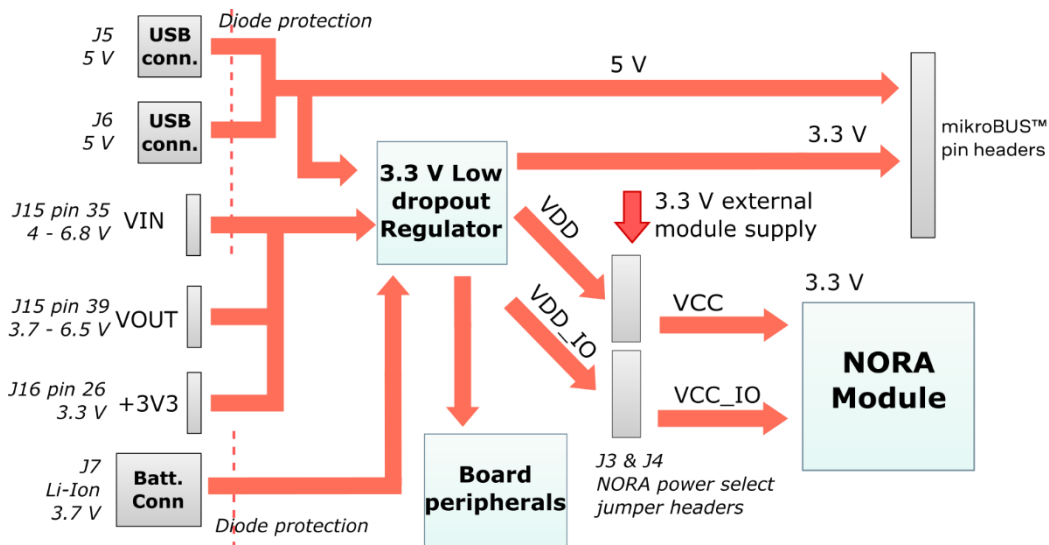


Figure 7: Block diagram of the power net distribution

The power sources are separated using the protection diodes that prevent reverse voltage to any of the other supplies, as shown in [Figure 7](#).

The USB type C connectors are only capable of handling 5 V input. The 12 V/20 V voltage rails are disabled.

3.2.1 Default power configuration, 3.3 V

[Figure 8](#) shows the default “out-of-the-box” power configuration for the evaluation board. In this configuration, all board peripherals are powered up and the module is directly supplied by the board. Everything runs at 3.3 V.

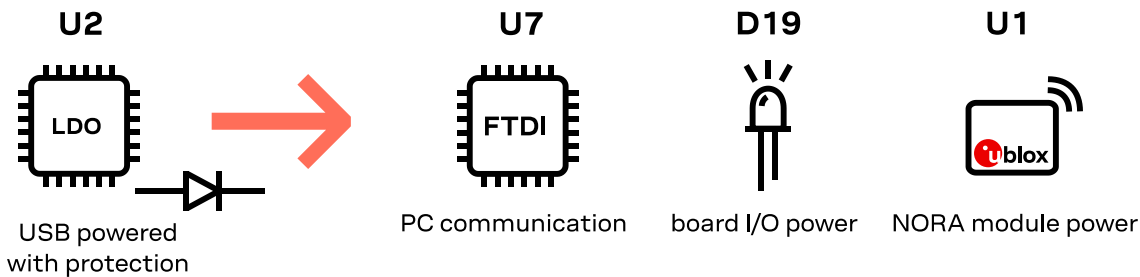


Figure 8: Jumper positions for default power configuration

3.2.2 Battery powered, 3.7 V

The configuration for using EVK-NORA-W40 with a battery is shown [Figure 9](#). In this configuration, the battery voltage is connected to **VDD_NORA**, which in turn, is connected to the VCC supply in the NORA-W40 module.

For battery-powered operation, communication between the EVK and module can be configured for:

- PC communication through USB connectors J5 and J6, where the battery supply is discontinued automatically and input power is supplied over USB. The battery supply is restored when the USB connector is disconnected.
- JTAG debugging through the debug header J9.
- External FTDI cable connection over the UART0 interface using header J15. To identify the UART0 interface on the NORA module, see also [Multipurpose GPIO header](#).

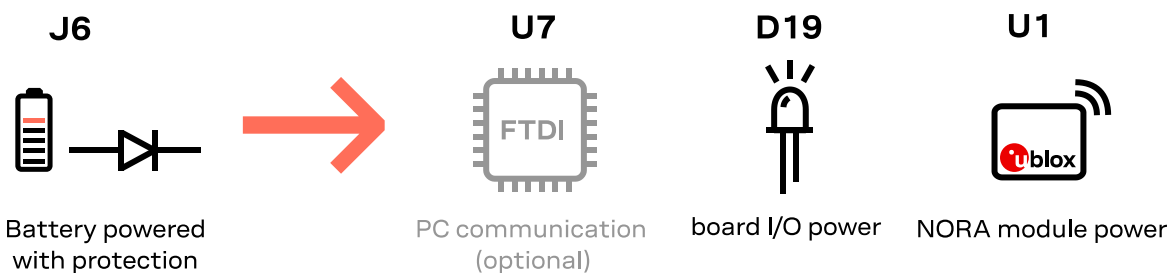


Figure 9: Jumper positions for battery powered operation

3.2.3 External supply, 3.0 – 3.6 V

When measuring current consumption or performing other NORA-W40 module characterization measurements, it can be useful to power the module with an external source such as a lab power supply. In such cases, the required supply nets can be fed externally by connecting to the pin headers. For example, the NORA-W40 module can be powered by connecting an external supply directly to connectors J3.2 and J4.2 to VCC, and J3.3 or J4.1 to GND. For more information about how to connect external power supplies, see also [Using an external power supply or power analyzer](#).

 Make sure that unpowered parts of the board are properly isolated from the NORA module. If a voltage is applied to the signal of an unpowered device/component, current might leak through the various protection circuits in this device. This might give false readings when measuring current consumption. Isolation can be achieved by turning off the Switch S1.

Figure 10 below shows a few optional jumper connections that can be helpful when supplying the module with an external supply.

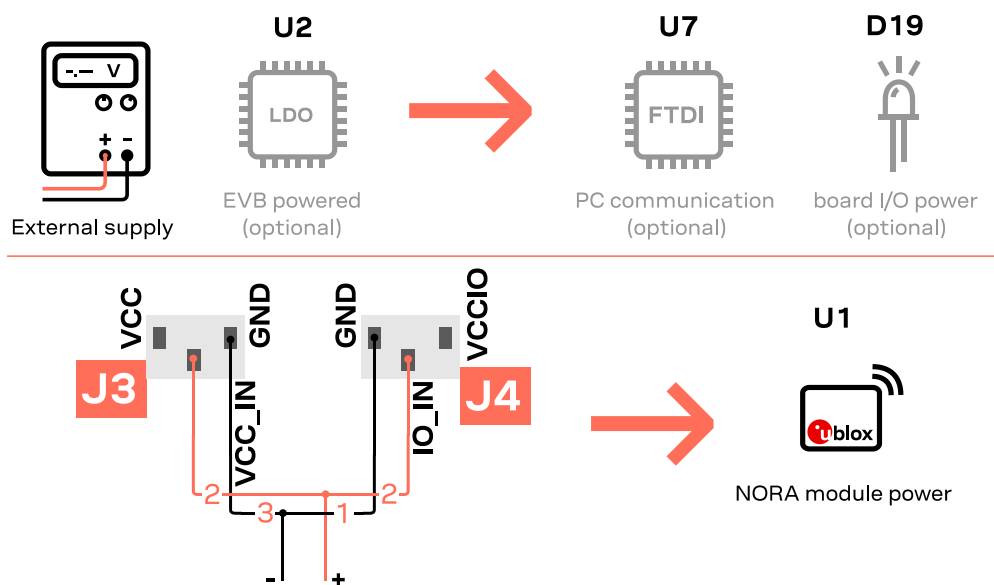
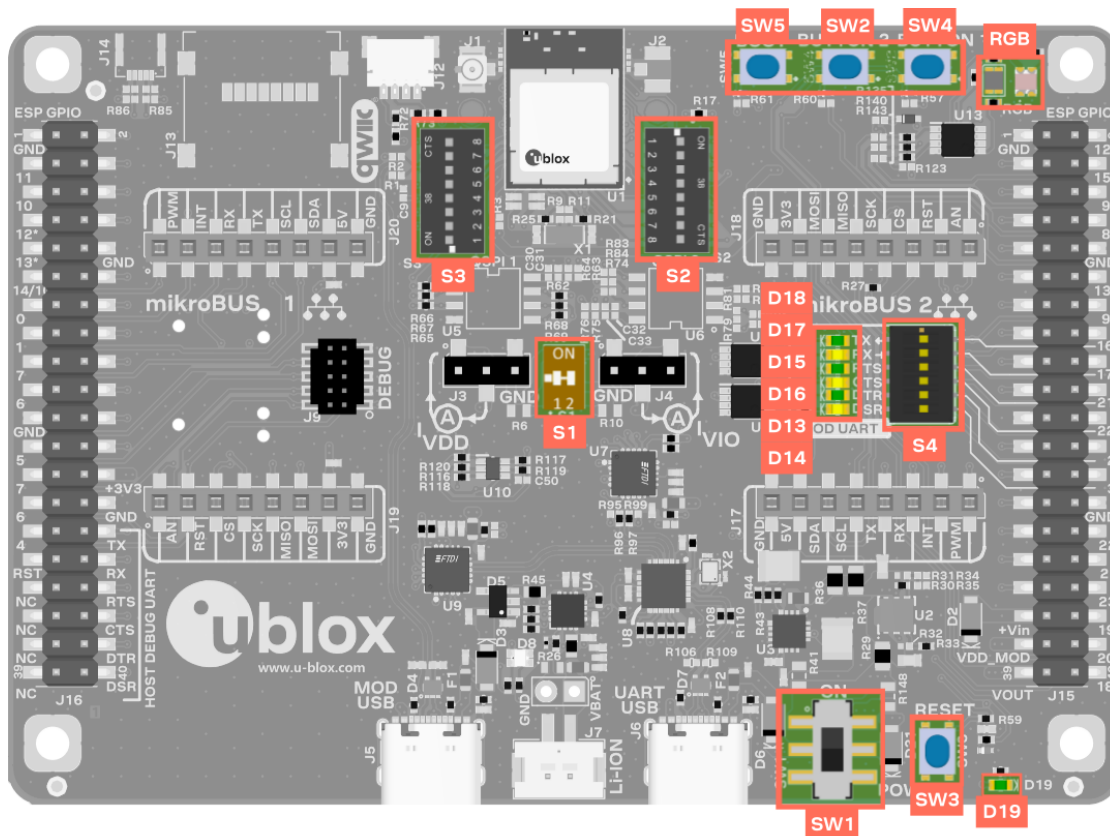


Figure 10: Using an external power supply

3.3 Switches, buttons and LEDs

EVK-NORA-W40 board is equipped with four DIP switches (S1, S2 S3 and S4), one switch (SW1), four buttons (SW2, SW3, SW4 and SW5), one RGB LED (RGB), and seven LEDs (from D13 to D19). [Figure 11](#) shows the location of these components on the board.



Buttons and LEDs

SW1 ON/OFF

SW3	Reset	D19	Power LED
SW5	Boot	RGB	Status LED
SW4	User button 1	D18	TXD LED
SW2	User button 2	D17	RXD LED
S1	Module Power	D15	RTS LED
S2	GPIO select	D16	CTS LED
S3	GPIO select	D13	DTR LED
S4	UART select	D14	DSR LED

Figure 11: Position of the push buttons and LEDs on the evaluation board

3.3.1 Reset

EVK-NORA-W40 provides a hardware reset to the NORA-W40 module:

- The Reset button (SW3) is connected to the module **RESETn** signal.
- To enter the programming mode, assert a reset in bootloader mode.
- To enter bootloader mode, hold down the Boot button (SW5) while the EVK is powered on.

3.3.1.1 Automatic bootloader

The `esptool.py` flash tool supports automatic entry to the bootloader on the EVK-NORA-W40. The tool allows the board to be reset without the need to press the Boot button. It is not possible to use the Hardware Flow control or the DSR signals on the UART using this setup.

For more information about the tool, visit the GitHub esptool repository [\[5\]](#).

3.3.1.1 Manual bootloader

It is also possible to enter the bootloader manually. To enter bootloader mode, Hold down the RESET button (SW3) and the Boot button (SW5) together. Wait for a few seconds, release the RESET button, and then the Boot button while the module powers on.

3.3.2 Push buttons

In addition to the RESET button, the evaluation board also supports two user buttons (SW2 and SW4) that are connected to ground when pressed. The functionality of these buttons is controlled by the software application through the GPIO interface. The buttons and the associated GPIO signals are shown in [Figure 11](#).

[Table 2](#) describes the user buttons, the corresponding GPIO signals and protection diodes. For proper operation, the internal pull-up resistor of each NORA-W40 GPIO pin must be enabled.

Button	Switch	GPIO	Protection diode	Function
1	SW2	GPIO12	D10	No predefined function (software controlled)
2	SW4	GPIO13	D11	No predefined function (software controlled)

Table 2: User button components

3.3.3 DIP switches

The EVK-NORA-W40 evaluation board also includes several different Dual in-line (DIP) switches. The purpose of these switches is to control different functionalities such as, power input to module, module primary UART and multipurpose GPIOs.

[Table 3](#) describes the various DIP switches and their relationship with the corresponding NORA signals. See also [Interface DIP switch](#).

Switch	Function
S1	Module VCC, VCC-IO control
S2	Multipurpose GPIO select
S3	Multipurpose GPIO select
S4	Primary UART connect

Table 3: DIP switch functions

3.3.4 LEDs

EVK-NORA-W40 supports eight LEDs to indicate Power, UART0, and System status:

- **Power status** (D19): Indicates power on the board when lit (green)
- **UART0 status** (D13–D18): Indicates UART0 signal status under GPIO control, as shown in [Table 4](#).
- **System status** (RGB LED strip): Supplied from the **+5V** net and controlled by the associated GPIO (GPIO8) RMT peripheral. The operation of this RGB LED can be customized in the customer application by configuring GPIO8. If there is a need to disconnect the LED from the GPIO8, remove resistor R146.

Table 4 describes each of the UART0 LEDs and their relationship with corresponding pin sockets, GPIO and serial UART0 signals.

LED	Color	GPIO	DIP switch	Comments
D18	Green	GPIO16/UART0-TxD	S4.1	UART0-TxD activity indicator
D17	Orange	GPIO17/UART0-RxD	S4.2	UART0-RxD activity indicator
D15	Green	GPIO21/UART0-RTS	S4.3	UART0-RTS activity indicator
D16	Orange	GPIO22/UART0-CTS	S4.4	UART0-CTS activity indicator
D13	Green	GPIO2/UART0-DTR	S4.5	UART0-DTR activity indicator
D14	Orange	GPIO3/UART0-DSR	S4.6	UART0-DSR activity indicator
D19	Green	-	-	Power ON indicator
RGB	Red/Green/Blue	GPIO8/LED_RED	-	REG LED to test module applications

Table 4: UART0 LEDs and associated signals

3.4 USB interfaces

There are two physical USB interfaces on the EVK: COM USB (J6) and a MOD USB (J5). The location of these interfaces on the EVK-NORA-W40 PCB are shown in Figure 12.

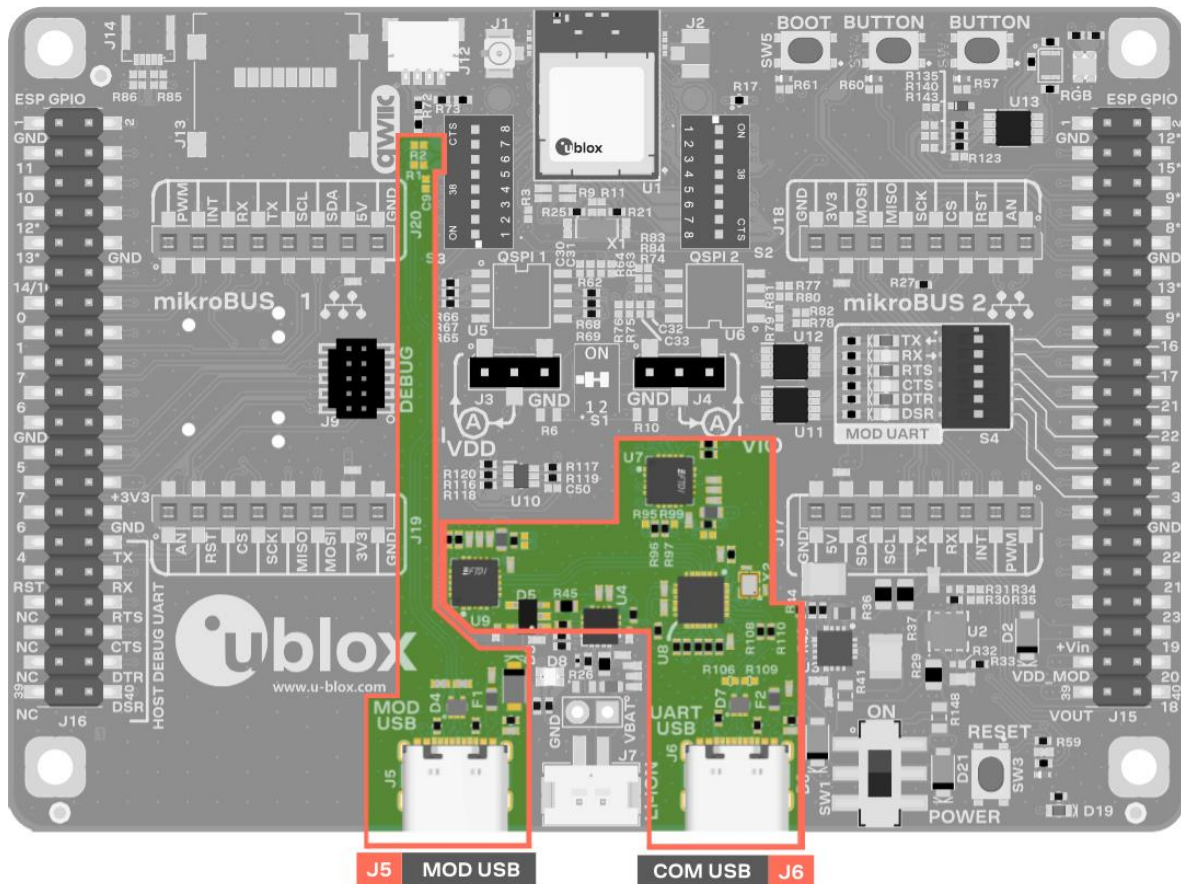


Figure 12: NORA-W40 USB interface

3.4.1 COM USB interface

For easy serial communication with the NORA-W40 module, you can connect a computer to the evaluation board through either of the two COM ports, which transfer the serial data via two different FTDI USB-to-UART ICs, as shown in [Figure 12](#).

The COM USB interface (J6) is connected to two USB-to-UART converters (FTDI IC, U7 and U9) via a USB hub (USB IC, U8).

FTDI IC (U7) is connected to the module (U1) via DIP switch (S4). The switch (S4) allows FTDI IC (U7) to communicate with the UART0 interface of the module. If external connectivity of UART0 is required, switch (S4) can be turned off to isolate the module UART0 pins from on-board FTDI IC (U7). The UART0 interface from the module can only be used for either FTDI IC (U7), or externally through header J15.

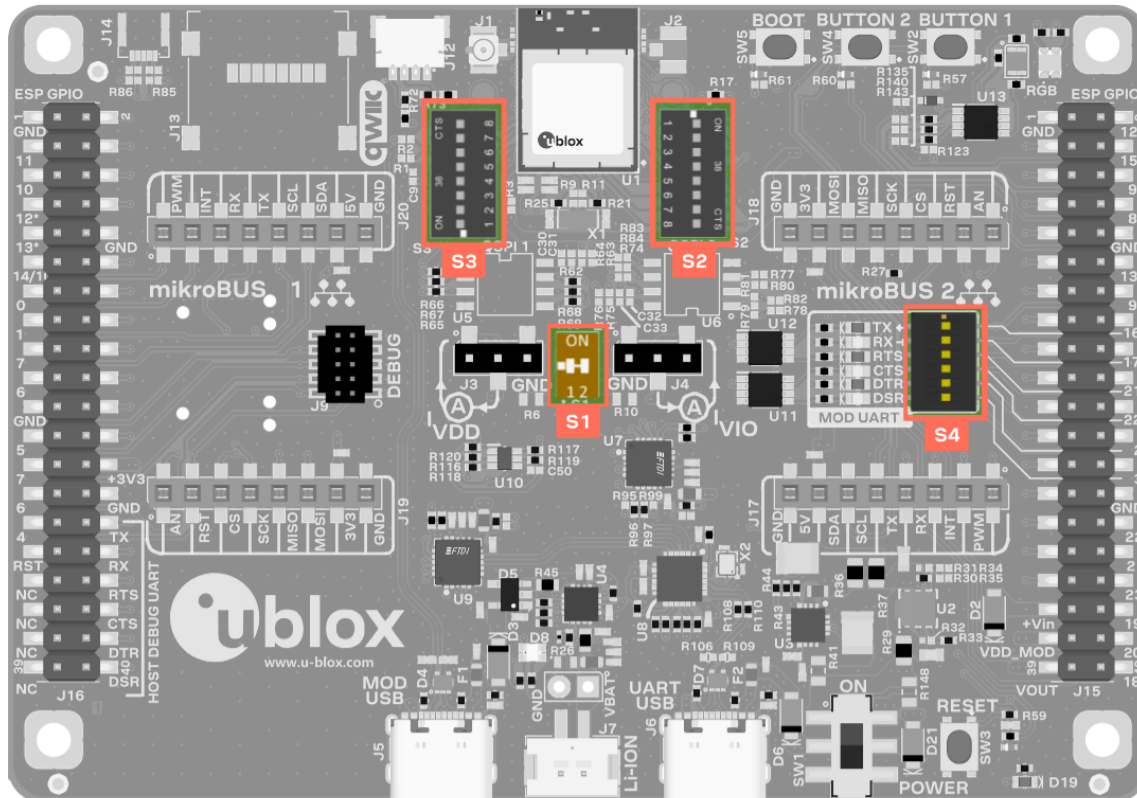
FTDI IC U9 connections are exposed to pin socket J16 and not connected internally to any interface. It can be utilized to connect to module UART1 or LP-UART or as an external UART for debugging purposes. See also [UART DIP switch](#).

3.4.2 MOD USB interface

The MOD USB (J5) is directly connected to the module providing easy communication. A USB Serial/JTAG controller resides in NORA-W40, which allows it to act as a USB to serial converter as well as a USB-to-JTAG adapter for communication with CPU debug core. However, NORA-W40 is set to USB serial controller by default.

3.5 Interface DIP switch

The EVK-NORA-B4 includes a set of DIP switches (S1, S2, S3 and S4) that are used to control functionalities supported in the NORA-W40 module. The switch locations and related functions are shown in [Figure 13](#).



INTERFACE SELECT DIP SWITCH



Figure 13: DIP switches on EVK NORA-W40

3.5.1 Module power switch

DIP switch (S1) controls input power to the NORA-W40 module. [Table 5](#) shows the relationship between each switch and the module.

 To connect an onboard power supply, set both sub-switches of Switch (S1) to “ON” position. To connect an external power supply, set both sub-switches position to “OFF. See also [Powering options](#).

NORA-W40 pin name	NORA-W40 function	DIP switch	Comments
A8	VDD	S1.1	Input voltage to NORA module
A7/B7	VCCIO	S1.2	I/O reference voltage to NORA module

Table 5: DIP switch S1 input power control to NORA-W4

3.5.2 GPIO DIP switch

NORA-W1 features several multifunctional pins that are assigned to specific functions or operate as general-purpose I/Os, with their roles determined by the DIP switches. For instance, pin D8 can function as a USB differential data signal connected to a push button (SW4) or as GPIO12 - depending on the DIP switch configuration. See also, the NORA-W40 datasheet, *Pin-out* [1].

 By default, all switch positions are “On” to enable the connections between each module pin and the available interface on the evaluation board. For minimal interference and optimal performance, it is advisable to disable alternate functions and enable only the necessary pins.

[Table 6](#) describes S2 switch positions, their main and alternate functions, and the module pins to which they are connected.

DIP switch	NORA-W40 pin	ESP32-C6 GPIO	Functionality
S2.1	J2	GPIO6	JTAG Test clock, routed also to B4
S2.2	H8	GPIO9	Multipurpose GPIO, routed also to F7
S2.3	G1	GPIO7	JTAG Test Data Out, routed also to A3
S2.4	D3	GPIO22	SPI1 Hold, routed also to F9
S2.5	A2	GPIO21	SPI1 Write Protect, routed also to F8
S2.6	B4	GPIO6	I2C_SDA, routed also to J2
S2.7	A3	GPIO7	I2C_SCL, routed also to G1
S2.8	A5	GPIO14	Multipurpose GPIO, routed also to E9

Table 6: DIP switch (S2) to control the functionality of the GPIOs available on NORA-W4 module.

[Table 7](#) describes S3 switch positions, their main and alternate functions, and the module pins to which they are connected.

DIP switch	NORA-W40 pin	ESP32-C6 GPIO	Functionality
S3.1	D8	GPIO12	Switch button 1, routed also to D9
S3.2	D9	GPIO12	USB differential data signal (N), routed also to D8
S3.3	C9	GPIO13	USB differential data signal (P), routed also to C8
S3.4	C8	GPIO13	Switch button 2, routed also to C9
S3.5	E9	GPIO14	Multipurpose GPIO, routed also to A5
S3.6	F9	GPIO22	UART0 CTS, routed also to D3
S3.7	F8	GPIO21	UART0-RTS, routed also to A2
S3.8	F7	GPIO9	BOOTn, routed also to H8

Table 7: DIP switch (S3) to control the functionality of the GPIOs available on NORA-W4 module

3.5.3 UART DIP switch

In applications where the UART pins are required for other GPIO functionalities, DIP switch (S4) allows you to isolate UART interface from the onboard FTDI chip (U7) on the NORA-W4 module. Each connection between the NORA module and the FTDI chip can be disconnected using the S4 DIP switch positions shown in [Table 6](#). The corresponding signals are accessed through the [Multipurpose GPIO header](#) (J15).

 By default, all switch positions are “ON” to enable connection between the FTDI chip and the NORA module. Turning any switch position “Off” isolates the related module pin to make it available through connector J15.

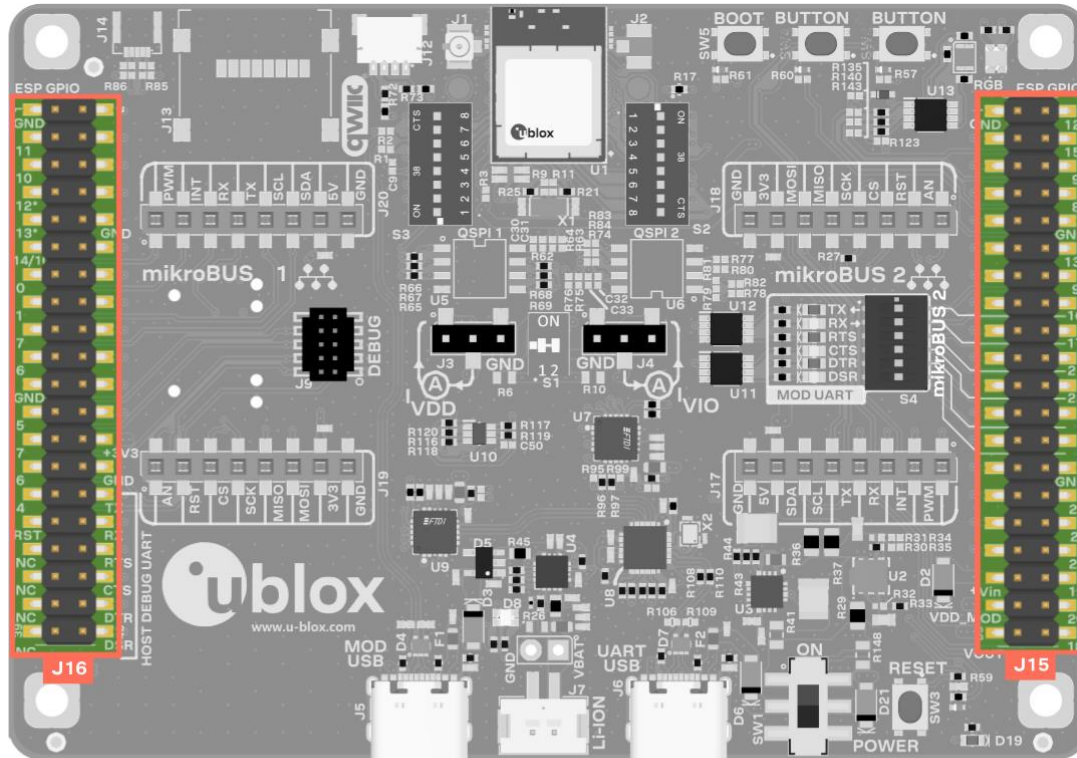
 When a switch position is “On”, the respective GPIOs can’t be accessed through connector J15.

DIP switch	NORA-W40 pin	NORA-W40 function	USB to UART chip signal
S4.1	G8	GPIO16/UART0-TXD	FTDI-RX
S4.2	G9	GPIO17/UART0-RXD	FTDI-TX
S4.3	F8	GPIO21/UART0-RTS	FTDI-CTS
S4.4	F9	GPIO22/UART0-CTS	FTDI-RTS
S4.5	E8	GPIO2/UART0-DTR	FTDI-DSR
S4.6	J9	GPIO3/UART0-DSR	FTDI-DTR

Table 8: DIP switch S4 to isolate onboard FTDI chip from NORA-W4 module

3.6 Multipurpose GPIO header

Figure 14 shows the multi-purpose GPIO headers mounted on NORA-W40 evaluation board.



MultiPurpose GPIOs

J16	J15
1 GND	1 GND
2 NC	2 D8/IO12
3 A6/IO11/D_RX	3 NC
4 A5/IO10/IO14/D_TX	4 NC
5 D9/IO12	5 NC
6 C9/IO13	6 GND
7 E9/IO14/IO10	7 NC
8 C6/IO0	8 NC
9 B6/IO1	9 NC
10 A3/IO7/I2C_SCL	10 NC
11 B4/IO6/I2C_SDA	11 NC
12 GND	12 NC
13 H1/IO5/JT_TDI	13 NC
14 G1/IO7/JT_MTD0	14 +3V3
15 J2/IO6/JT_TCK/SWD_CLK	15 GND
16 H2/IO4/JT_TMS/SWD_IO	16 UART1-TXD
17 J3/RESETn	17 UART1-RXD
18 NC	18 UART1-RTS
19 NC	19 UART1-CTS
20 NC	20 UART1-DTR
21 NC	21 UART1-DSR
22 39	22 39
23 40	23 40

Figure 14: EVK NORA-W4 multipurpose GPIO pin headers

Table 9 describes pin headers J15 and J16, their functionality, and corresponding module pin.

Con. pin	Mod. pin	Description	Schematic net	ESP32-C6 pin	Alternate functions/notes
J15.1	GND	Ground	GND	-	
J15.3	-	Not connected	-	-	
J15.5	-	Not connected	-	-	
J15.7	-	Not connected	-	-	
J15.9	-	Not connected	-	-	
J15.11	-	Not connected	-	-	
J15.13	-	Not connected	-	-	
J15.15	-	Not connected	-	-	
J15.17	-	Not connected	-	-	
J15.19	-	Not connected	-	-	
J15.21	GND	Ground	GND	-	
J15.23	-	Not connected	-	-	
J15.25	-	Not connected	-	-	
J15.27	-	Not connected	-	-	
J15.29	-	Not connected	-	-	
J15.31	-	Not connected	-	-	
J15.33	-	Not connected	-	-	
J15.35	-	Ext. DC supply input, 3.3 – 5 DC	+Vin	-	
J15.37	-	Mod. input voltage, 3.0-3.6 VDC	VDD_MOD	-	
J15.39	-	EVK input voltage, 3.7-5 VDC	VOOUT	-	
J15.2	D8	General Purpose I/O	D8/IO12	IO12	
J15.4	H9	General Purpose I/O	H9/IO15	IO15	
J15.6	H8	General Purpose I/O	H8/IO9	IO9	
J15.8	J8	General Purpose I/O	J8/IO8	IO8	
J15.10	GND	Ground	GND	-	
J15.12	C8	General Purpose I/O	C8/IO13	IO13	
J15.14	F7	General Purpose I/O	F7/IO9	IO9	
J15.16	G8	General Purpose I/O	G8/IO16/URT0_TX	IO16	Module UART TX
J15.18	G9	General Purpose I/O	G9/IO17/URT0_RX	IO17	Module UART RX
J15.20	F8	General Purpose I/O	F8/IO21/URT0_RTS	IO21	Module UART RTS
J15.22	F9	General Purpose I/O	F9/IO22/URT0_CTS	IO22	Module UART CTS
J15.24	E8	General Purpose I/O	E8/IO2/WAKE_HOST	IO2	Module UART DTR LP option (LP_GPIO2 / LP_UART_RTSN)
J15.26	J9	General Purpose I/O	J9/IO3/WAKE_UP	IO3	Module UART DSR LP option (LP_GPIO3 / LP_UART_CTSN)
J15.28	GND	Ground	GND	-	
J15.30	D3	General Purpose I/O	D3/IO22	IO22	
J15.32	A2	General Purpose I/O	A2/IO21	IO21	
J15.34	B3	General Purpose I/O	B3/IO23	IO23	
J15.36	B1		B1/IO19	IO19	
J15.38	C1	General Purpose I/O	C1/IO20	IO20	
J15.40	C2		C2/IO18	IO18	

Con. pin	Mod. pin	Description	Schematic net	ESP32-C6 pin	Alternate functions/notes
J16.1	GND	Ground	GND	-	-
J16.3	A6	General Purpose I/O	A6/IO11/D_RX	IO11	
J16.5	A5	General Purpose I/O	A5/IO10/IO14/D_TX	IO14	
J16.7	D9	General Purpose I/O	D9/IO12	IO12	
J16.9	C9	General Purpose I/O	C9/IO13	IO13	
J16.11	E9	General Purpose I/O	E9/IO14/IO10	IO14	-
J16.13	C6	General Purpose I/O	C6/IO0	IO0	LP option (LP_GPIO0 / LP_UART_DTRN)
J16.15	B6	General Purpose I/O	B6/IO1	IO1	LP option (LP_GPIO1 / LP_UART_DSRN)
J16.17	A3	General Purpose I/O	A3/IO7/I2C_SCL	IO7	LP option (LP_GPIO7 / LP_I2C_SCL)
J16.19	B4	General Purpose I/O	B4/IO6/I2C_SDA	IO6	LP option (LP_GPIO6 / LP_I2C_SDA)
J16.21	GND	Ground	GND	-	-
J16.23	H1	General Purpose I/O	GPIO5/MTDI	IO5	LP option (LP_GPIO5 / LP_UART_TXD)
J16.25	G1	General Purpose I/O	G1/IO7/JT_MTDO	IO7	LP option (LP_GPIO7 / LP_I2C_SCL)
J16.27	J2	General Purpose I/O	J2/IO6/JT_TCK/SWD_CL K	IO6	LP option (LP_GPIO6 / LP_I2C_SDA)
J16.29	H2	General Purpose I/O	H2/IO4/JT_TMS/SWD_IO	IO4	LP option (LP_GPIO4 / LP_UART_RXD)
J16.31	J3	General Purpose I/O	J3/RESETn	CHIP_PU	RESETn
J16.33	-	Not connected	-	-	
J16.35	-	Not connected	-	-	
J16.37	-	Not connected	-	-	
J16.39	-	Not connected	-	-	
J16.2	-	Not connected	-	-	
J16.4	-	Not connected	-	-	
J16.6	-	Not connected	-	-	
J16.8	-	Not connected	-	-	
J16.10	GND	Ground	GND	GND	
J16.12	-	Not connected	-	-	
J16.14	-	Not connected	-	-	
J16.16	-	Not connected	-	-	
J16.18	-	Not connected	-	-	
J16.20	-	Not connected	-	-	
J16.22	-	Not connected	-	-	
J16.24	-	Not connected	-	-	
J16.26	-	3.3V DC regulated supply output	+3V3	-	
J16.28	GND	Ground	GND	-	
J16.30	-	Secondary UART TX	UART1-TXD	-	
J16.32	-	Secondary UART RX	UART1-RXD	-	
J16.34	-	Secondary UART RTS	UART1-RTS	-	

Con. pin	Mod. pin	Description	Schematic net	ESP32-C6 pin	Alternate functions/notes
J16.36	-	Secondary UART CTS	UART1-CTS	-	
J16.38	-	Secondary UART DTR	UART1-DTR	-	
J16.40	-	Secondary UART DSR	UART1-DSR	-	

Table 9: Pinout of the NORA-W4 GPIO headers

 The low power (LP) mode option is used to save power with limited functionality. For more information see NORA-W40 system integration manual [\[2\]](#).

3.7 mikroBUS interfaces

The EVK-NORA-W40 has two mikroBUS connectors, making it easy to host MIKROE Click boards™. With over 1,400 Click boards available, developers can explore countless possibilities by combining u-blox modules with functionalities from various technology suppliers—all using the same kit. Simply plug the desired modules into the mikroBUS connectors to get started.

Each mikroBUS connector exposes:

- 3x GPIOs (RESET, PWM, INT)
- 1x analog input (AN)
- 1x 2-wire UART interface (RX, TX)
- 1x I2C bus (SDA, SCL)
- 1x SPI interface (MISO, MOSI, SCK, CS) with one SPI chip select line for each mikroBUS slot.

For further information about the mikroBUS standard, visit the MIKROE website [\[4\]](#).

 As NORA-W40 I/Os are referenced at 3.3 V, connecting a third-party Click board with I/Os referenced at 5 V can seriously damage the board.

Two mikroBUS sockets are available to incorporate mikroBUS click and other application boards into a project.

A mikroBUS application board can be installed on the following headers as shown in [Figure 15](#). Each application board should face outwards towards the GPIO pin headers.

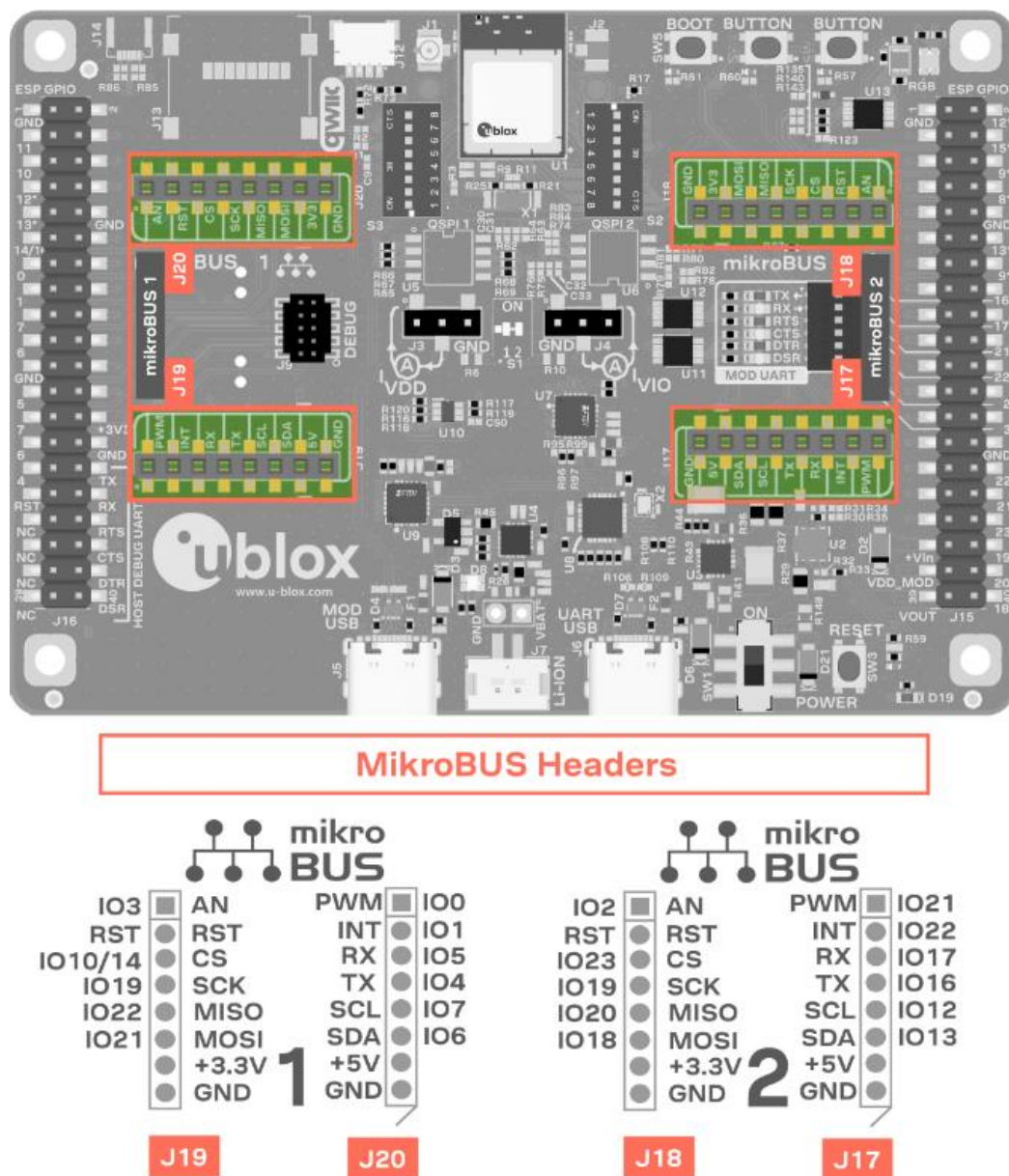


Figure 15: mikroBUS header location (header color may vary)

3.7.1.1 mikroBUS interface 1 (left)

J19 Pin	mikroBUS pin	Schematic net name	Function	Remarks
1	AN	J9/IO3/WAKE_UP	GPIO	Analog input capable GPIO
2	RESET	J3/RESETn	Reset	
3	CS	A5/IO10/IO14/D_TX	GPIO	
4	SCK	B1/IO19	GPIO	FSPI clock
5	MISO	D3/IO22	GPIO	FSPI HD
6	MOSI	A2/IO21	GPIO	FSPI WP
7	+3V3	+3V3	Power	
8	GND	Ground	Ground	

Table 10: mikroBUS interface 1 connector 1

J20 Pin	mikroBUS pin	Schematic net name	Function	Remarks
1	PWM	C6/IO0	GPIO	Analog input capable GPIO
2	INT	B6/IO1	GPIO	Analog input capable GPIO
3	RX	H1/IO5/JT_TDI	GPIO	Analog input capable GPIO/ LP_UART
4	TX	H2/IO4/JT_TMS/SWD_IO	GPIO	Analog input capable GPIO/ LP_UART
5	SCL	A3/IO7/I2C_SCL	GPIO	I2C clock / LP_I2C_SCL
6	SDA	B4/IO6/I2C_SDA	GPIO	I2C data / LP_I2C_SDA
7	+5V	+5V	Power	
8	GND	GND	Ground	

Table 11: mikroBUS interface 1 connector 2

3.7.1.2 mikroBUS interface 2 (right)

J18 Pin	mikroBUS pin	Schematic net name	Function	Remarks
1	AN	E8/IO2/WAKE_HOST	GPIO	Analog input capable GPIO
2	RESET	RESET	Reset	
3	CS	B3/IO23	GPIO	
4	SCK	B1/IO19	GPIO	FSPI clock
5	MISO	C1/IO20	GPIO	FSPI Q
6	MOSI	C2/IO18	GPIO	FSPI D
7	+3V3	+3V3	Power	
8	GND	GND	Ground	

Table 12: mikroBUS interface 2 connector 1

J5 / J6 Pin	mikroBUS pin	Schematic net name	Function	Remarks
1	PWM	F8/IO21/URT0_RTS	GPIO	
2	INT	F9/IO22/URT0_CTS	GPIO	
3	RX	G9/IO17/URT0_RX	GPIO	
4	TX	G8/IO16/URT0_TX	GPIO	
5	SCL	D8/IO12/SW1	GPIO	
6	SDA	8/IO13/SW2	GPIO	
7	+5V	+5V	Power	
8	GND	GND	Ground	

Table 13: mikroBUS interface 2 connector 2

 To adjust the clock signal on both mikroBUS interfaces, reconfigure J18 pin 4 by removing the 0 Ω resistor at position R27 and placing it at R123. This shifts the clock signal from net “B1/IO19” to “H9/IO15/LED_BLUE”.

3.8 Other interfaces

Figure 16 shows several other available interfaces on the evaluation board:

- LF-XTAL 32.768 kHz crystal connected to the NORA-W40 module to source the RTC clock
- JTAG Debug – for debugging, programming, and testing the NORA-W40 module
- QSPI flash – fast SPI interface supporting quad data lines for rapid read/write operations with external flash memory
- I2C/Qwiic – simplified two-wire communication protocol for connecting sensors and devices using a standard Qwiic connector

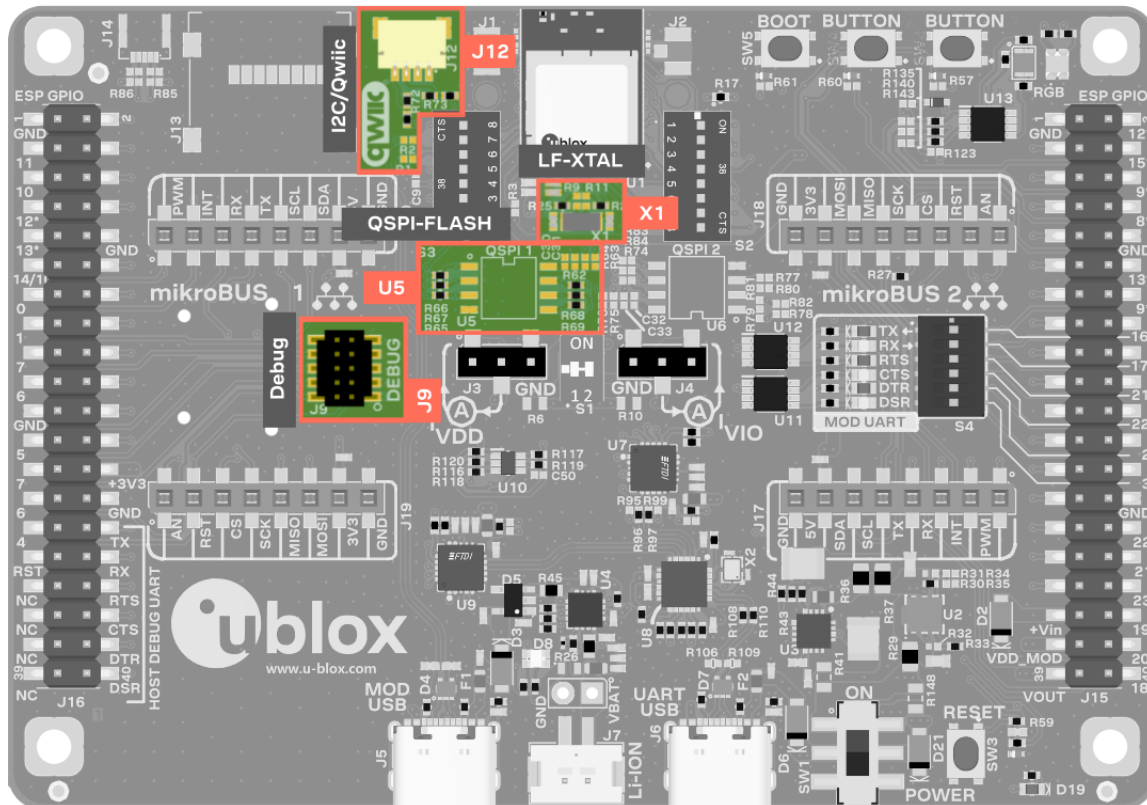


Figure 16: NORA-W40 Debug, I2C, SPI, and LFCLK

3.8.1 Low frequency clock

The evaluation board has a 32.768 kHz crystal, connected to the NORA-W40 module, that can be used to source the RTC clock. Alternatively, the clock can be sourced from the slow internal RC oscillator, or the divided clock of the internal fast RC oscillator.

C6/IO0/X_LP_P and **B6/IO1/X_LP_N** are used to connect low frequency crystal with NORA module. By default, the crystal is not connected to the module, and the crystal GPIOs are connected to the multi-purpose GPIO header. To connect the crystal to the module, swap R25 with R9 and R21 with R11 respectively. The placement of these resistors are positioned adjacent to the X1 crystal, as shown in [Figure 17](#).

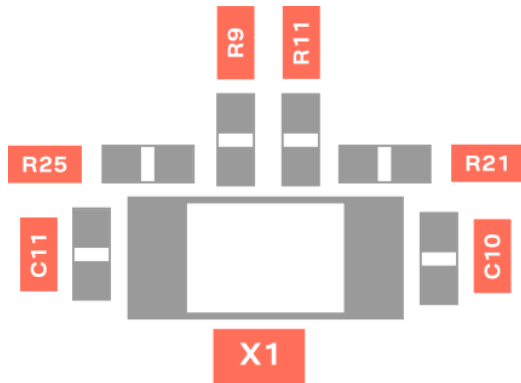


Figure 17: Schematic – 32 kHz crystal

3.8.2 JTAG debug interface

There are two interfaces for debugging NORA-W40 using JTAG:

- An external debug unit can be attached to the J9 header connector for firmware programming and debug. J9 is implemented with a 2x5 header with 1.27 mm pitch. [Figure 18](#) shows the pin layout of the connector.
- A USB serial/JTAG adapter – configured by default to USB serial mode. See also [MOD USB interface](#).

The CPU JTAG signals can either be routed to the USB serial/JTAG controller or the external JTAG adapter GPIO pads using eFuses. The pin layout for this JTAG debug connector is shown in [Figure 18](#).

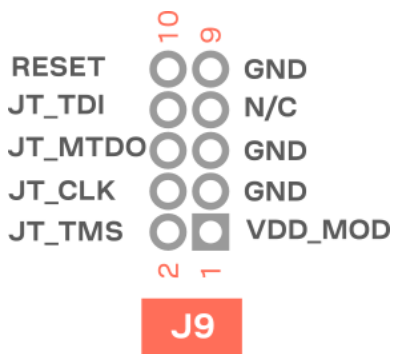


Figure 18: J9 JTAG debug connector pin layout

3.8.3 SPI interface

A Quad SPI external flash can optionally be mounted at position U5 on the EVK board. As an embedded flash memory already resides on the configured module, an external flash memory is in most cases superfluous.

To power the external flash from the **+3V3** supply on the evaluation board, fit a 0 Ω resistor (R64), a 0.47uF capacitor (0402) at C31 and a 0.01uF capacitor (0402) at C30.

Figure 19 shows the schematic of the External SPI flash circuit and its implementation on the EVK board.

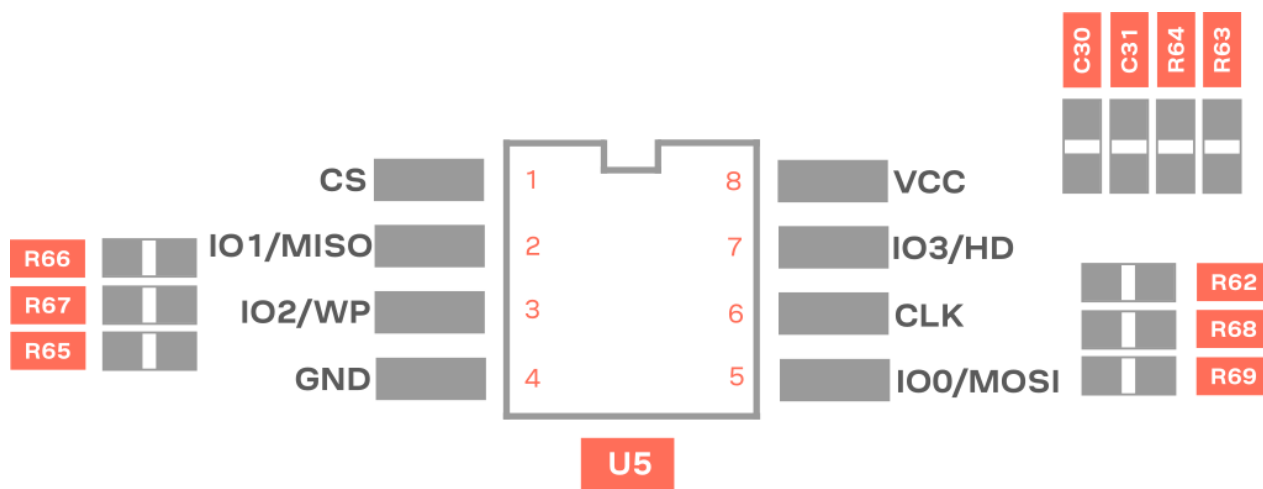


Figure 19: Quad SPI flash on NORA-W40 EVK

Table 14 shows the SPI functions for corresponding ESP32-C6 GPIOs and NORA-W40 pins.

Interface function	ESP32-C6 GPIO	NORA-W40 pin	Interface IC function
QSPI-CS0	23	B3	SPI chip select
QSPI-CLK	19	B1	SPIO clock
QSPI-IO3 HD	22	D3	SPIO Hold
QSPI-IO2 WP	21	A2	SPIO Write Protect
QSPI-IO1 Q	20	C1	SPIO Controller Input Peripheral
QSPI-IO0 D	18	C2	SPIO Controller Output

Table 14: Quad SPI interface signal overview for external flash

3.8.4 I2C / Qwiic

The NORA-W40 module supports a Qwiic connector (J12) that provides a standard I2C interface, which allows the module to function as either a controller or target device in communication with Qwiic-compatible products. Additionally, the I2C bus can be configured for low-power operation for energy-efficient applications.

J12	Qwiic pin	EVK signal	Function	Remarks
1	GND	GND	GND	
2	3.3 VDC	+3V3	Power	
3	SDA	B4/IO6/I2C_SDA	SDA	I2C data
4	SCL	A3/IO7/I2C_SCL	SCL	I2C clock

Table 15: Qwiic connector

The I/O level of I2C interface is referenced at 3.3 V. Deviating from the reference voltage can seriously damage the module.

Appendix

A Schematics

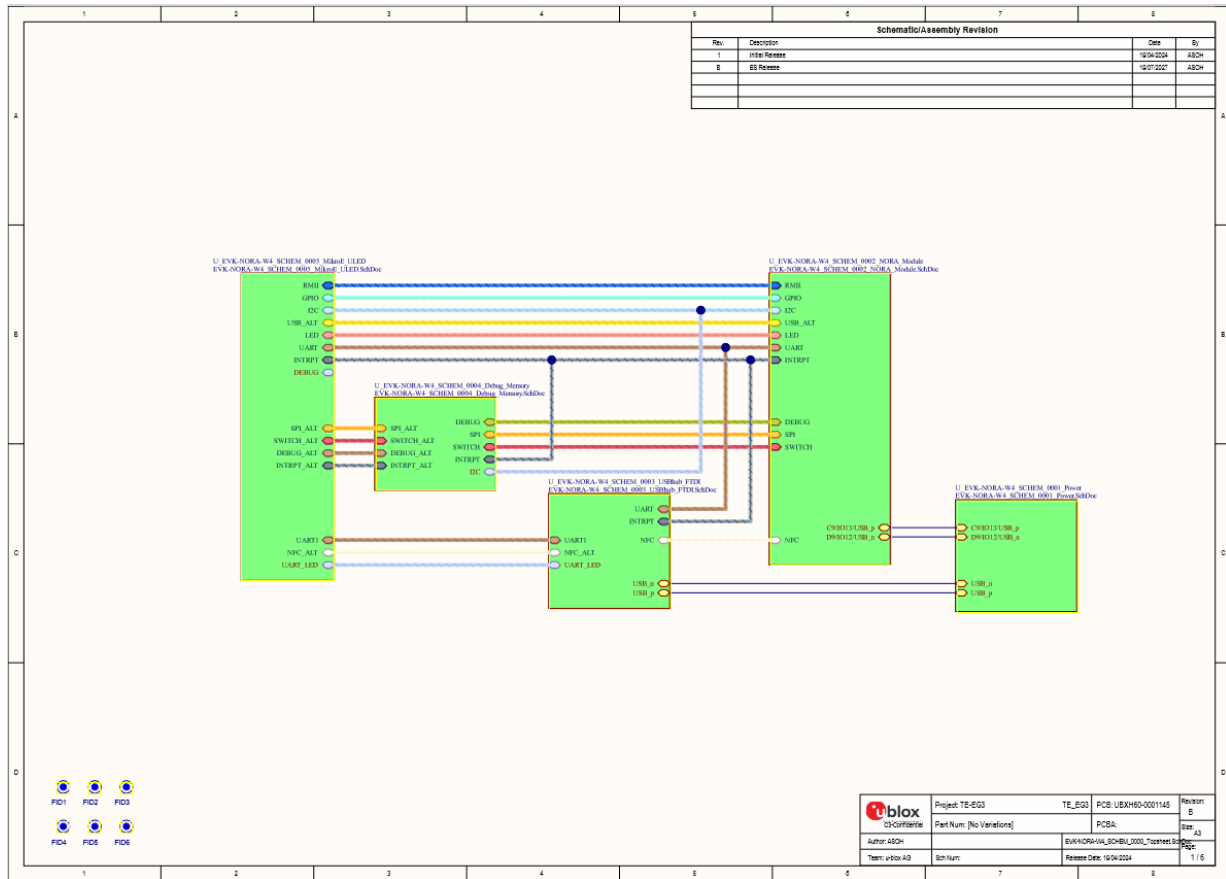


Figure 20: Top page

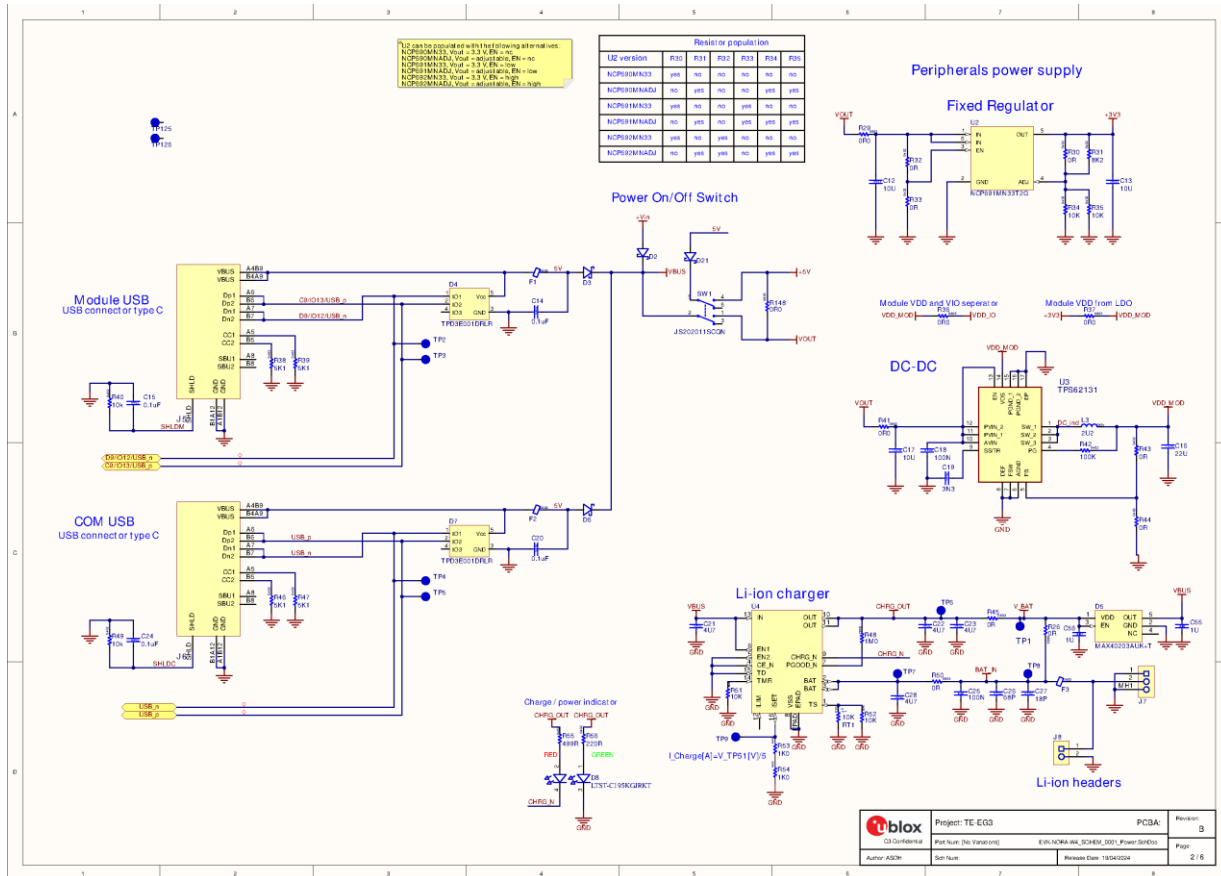


Figure 21: Power

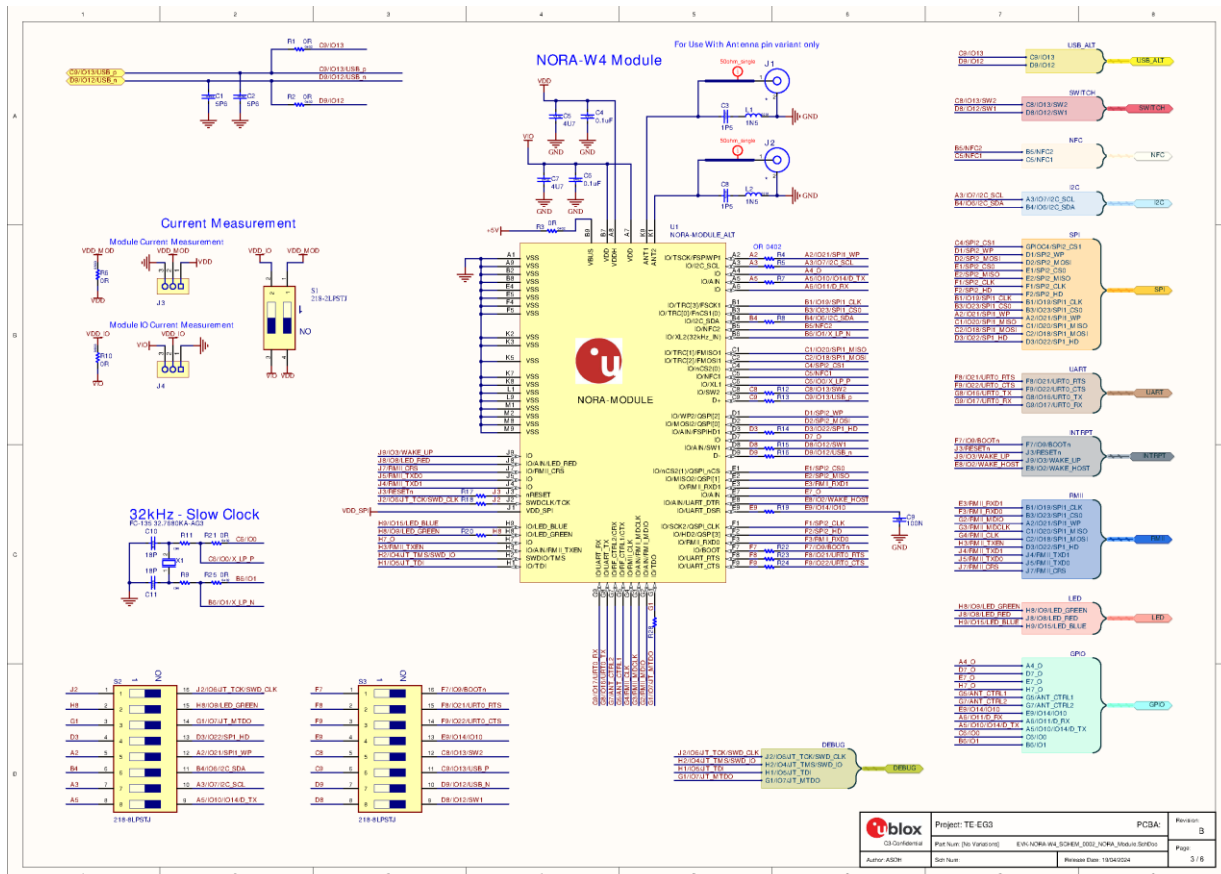


Figure 22: NORA-W4 module

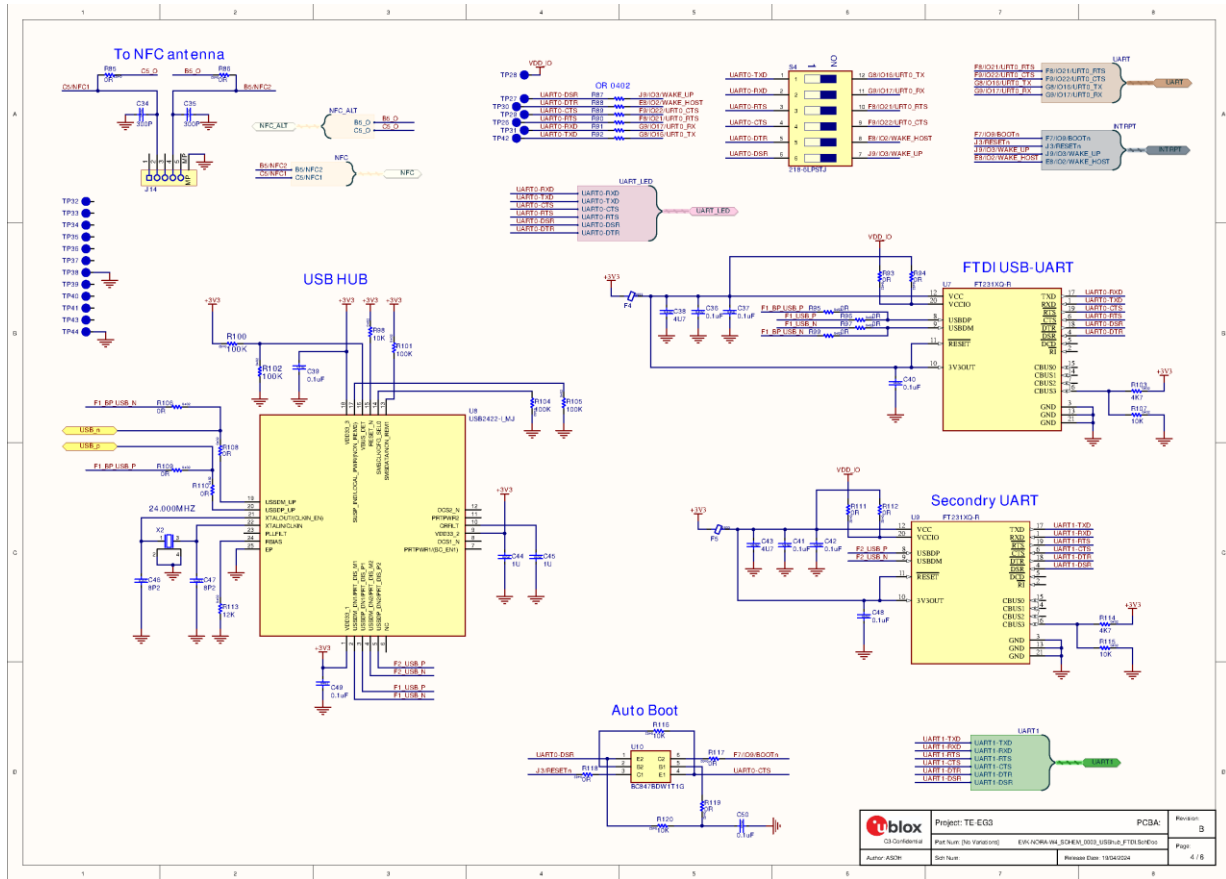


Figure 23: Interface FTDI, USB

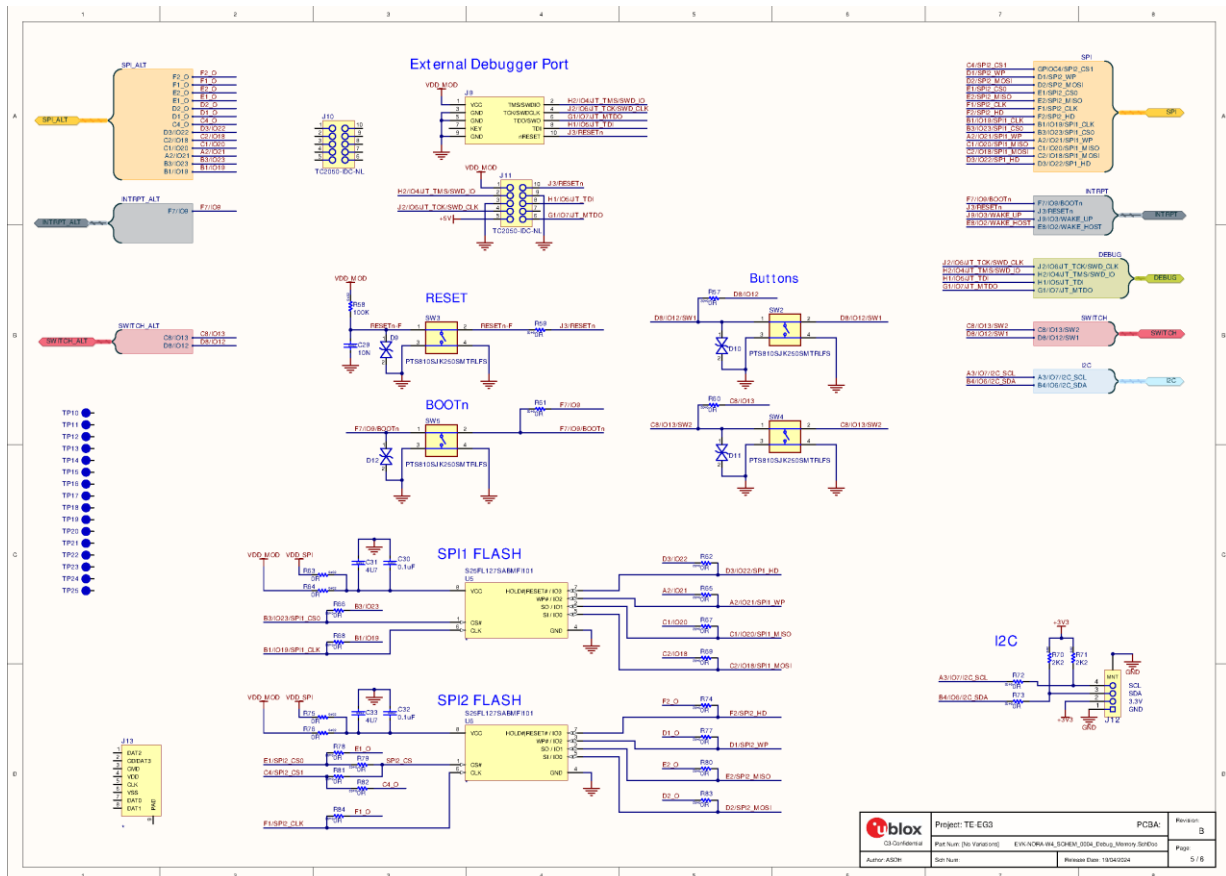


Figure 24: External Debug, Flash and Switch buttons

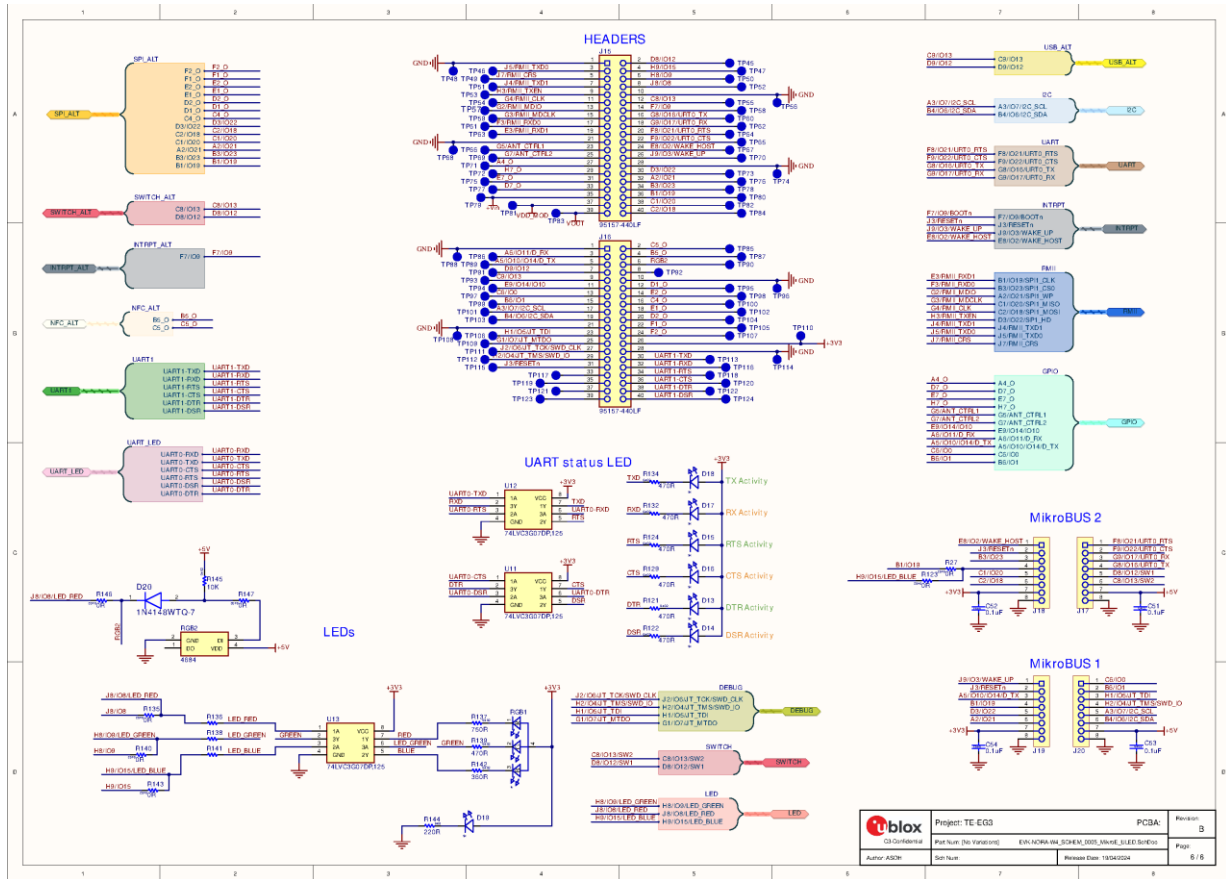


Figure 25: MikroBUS, GPIO headers and LEDs

B Assembly drawing

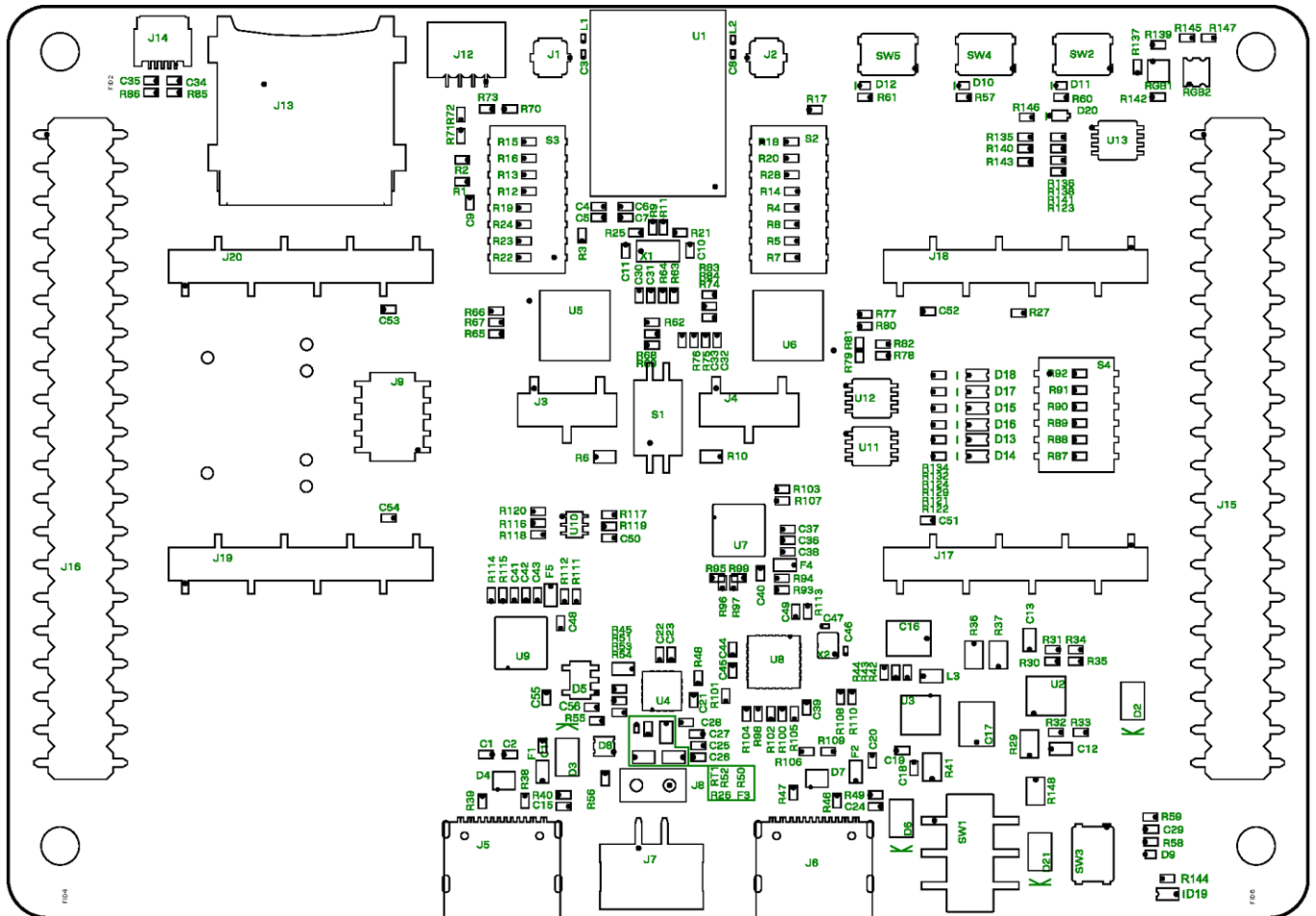


Figure 26: Top layer

C Glossary

Abbreviation	Definition
CPU	Central Processing Unit
CTS	Clear To Send
DC	Direct Current
DC-DC	DC to DC converter
DFU	Device Firmware Update
EVK	Evaluation Kit
FICR	Factory Information Configuration Register
GPIO	General Purpose Input / Output
LDO	Low Drop-Out voltage regulator
LE	Low Energy
LED	Light Emitting Diode
LF	Low Frequency
LiPo	Lithium-Polymer battery
NCS	nRF Connect SDK
NFC	Near-Field Communications
QSPI	Quad Serial Peripheral Interface
RC	Resistor-Capacitor network
RTS	Request To Send
RXD	Receive data signal
SES	SEGGER Embedded Studio
SIG	Special Interest Group
SoC	System on Chip
SPI	Serial Peripheral Interface
TXD	Transmit data signal
UICR	User Information Configuration Register
USB	Universal Serial Bus

Table 16: Explanation of the abbreviations and terms used

Related documentation

- [1] NORA-W40 data sheet, [UBX-21036702](#)
- [2] NORA-W40 system integration manual, [UBX-22005601](#)
- [3] FTDI FT231XQ-R Datasheet, [FT231X \(ftdichip.com\)](#)
- [4] MikroE website, <https://www.mikroe.com/>
- [5] Espressif SoC serial bootloader utility: <https://github.com/espressif/esptool>
- [6] Get Started - ESP32-C6: <https://docs.espressif.com/projects/esp-idf/en/stable/esp32c6/get-started/index.html>
- [7] ESP-IDF [Programming Guide - ESP32](#)

 For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	19-Nov-2024	asoh, hekf	Initial release for EVK-NORA-W40 engineering samples

Contact

u-blox AG

Address: Zürcherstrasse 68
8800 Thalwil
Switzerland

For further support and contact information, visit us at www.u-blox.com/support.