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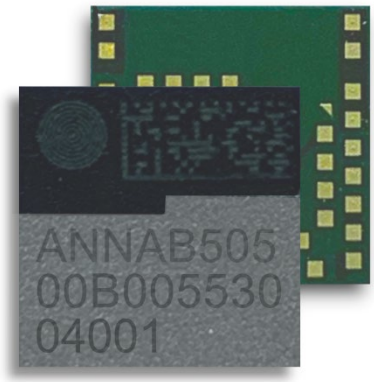
ANNA-B50 series

Stand-alone Bluetooth® 6.0 LE and IEEE 802.15.4 module

Data sheet



Abstract

Targeted towards system integrators and design engineers, this technical data sheet includes the functional description, pin definition, specifications, country approval status, handling instructions, and ordering information for the ultra-compact ANNA-B5 series stand-alone Bluetooth® LE and IEEE 802.15.4 modules. Integrated as a small, System-in-Package design, ANNA-B5 is available with external and internal antenna options, ANNA-B501 and ANNA-B505. ANNA-B50 series provides open CPU architecture with a powerful MCU for customer applications, while ANNA-B56 series is delivered with pre-flashed u-connectXpress software that supports OEMs with the shortest time-to-market. OEMs can embed their own application in conjunction with the Zephyr RTOS (Real -Time Operating System) integrated into the Nordic Semiconductor nRF Connect SDK.

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Document information

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Product status	Corresponding content status	
Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production/ End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Hardware version	PCN reference	Product Status
ANNA-B501	ANNA-B501-00B-00	03	N/A	Engineering sample
ANNA-B505	ANNA-B505-00B-00	03	N/A	Engineering sample

Contents

1 Functional description

1.1 Overview

ANNA-B50 series is a small, stand-alone Bluetooth® LE wireless System-in-Package (SiP) that is particularly suited for harsh professional environments. It is based on the Nordic Semiconductor nRF54L15 Bluetooth® LE System on Chip (SoC) that includes an ultra-low power 2.4 GHz multiprotocol radio and a powerful Arm® Cortex®-M33 processor with comprehensive peripherals and extensive memory. ANNA-B50 modules are qualified against Bluetooth® Core 6.0, including Channel Sounding for secure and accurate distance measurements between devices. Additionally, ANNA-B50 supports Thread, Matter, Zigbee, and Nordic proprietary radio modes. With Nordic proprietary radio modes, ANNA-B50 series modules support high throughput up to 4 Mbps. The module has 1524 KB NVM and 256 KB RAM.

ANNA-B50 modules need only a single supply voltage in the range of 1.7 to 3.6 V and can, as the supply voltage level can also be used as the I/O reference level, be easily integrated into simple, single voltage rail systems. The broad supply voltage range and ultra-low power consumption make ANNA-B50 modules particularly useful in battery powered systems.

ANNA-B50 series offers high-speed communication for multiple connected peripherals over SPI, QSPI, TWI, ADC, and PWM interfaces, and operates at ambient temperature range of -40 °C to 85 °C. The modules offer multiple antenna options, including antenna pin and integrated chip antenna options. For more information about the antennas that are approved for use with the ANNA-B50 series, see also the system integration manual [1].

1.2 Applications

ANNA-B50 series modules provide scalable solutions for a broad range of market segments, including smart cities and buildings, industrial automation, telematics, medical, and healthcare.

Specific application areas include:

- Industrial automation
- Advanced wearables
- Smart buildings and cities
- Low-power sensors
- Wireless-connected and configurable equipment
- Point-of-sale
- Medical and health devices
- Real-time Location, RTLS
- Indoor positioning
- Asset tracking
- Wearables

1.3 Block diagram

Figure 1 shows the integration of the nRF54L15 and other components in ANNA-B50 modules.

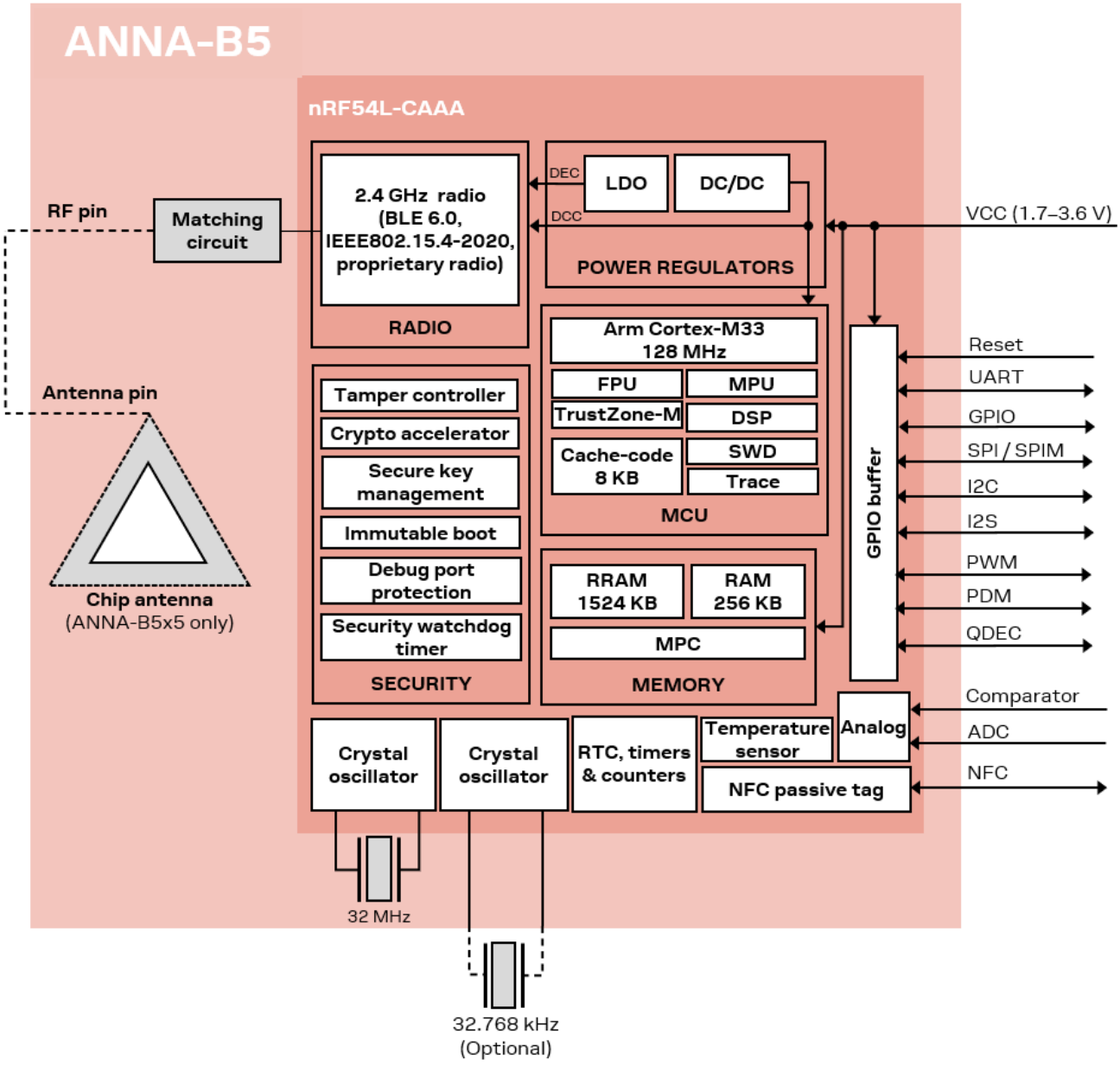


Figure 1: Block diagram of ANNA-B50 series

1.4 Product variants

The ANNA-B50 series modules come with two different antenna options. ANNA-B501 supports an antenna pin for use with external antennas, while ANNA-B505 includes an integrated chip antenna. All product variants are professional grade.

Table 1 describes the main differences between the ANNA-B50 various module variants.

Variants	CPU	Antenna	RAM	Flash	Weight [g]	Dimensions [mm]
ANNA-B501	nRF54L15	Pin	256 kB	1.524 MB	<1	6.5 x 6.5 x 1.2
ANNA-B505	nRF54L15	Chip antenna	256 kB	1.524 MB	<1	6.5 x 6.5 x 1.2

Table 1: ANNA-B50 variants exact characteristics summary

1.5 Product Description

Table 2 describes the common characteristics supported by all ANNA-B50 module variants.

Item	ANNA-B50x-00B
CPU	Nordic Semiconductor nRF54L15
Operating temperature	–40 to +85 °C
Operating voltage	+1.7 to +3.6 VDC
Available GPIO	32 pins
Core	Arm Cortex-M33 with TrustZone® technology
Operating speed	128 MHz or 64 MHz
Floating point unit (FPU)	Single precision with DSP instructions
Debug	Data Watchpoint and Trace (DWT), Embedded Trace Microcells (ETM), Instrumentation Trace Macrocell (ITM), Cross Trigger Interface (CTI), Serial Wire Debug (SWD)
Security	TrustZone®, isolation, tamper detection, and cryptographic engine side-channel leakage protection
Peripherals (not all simultaneous)	SPI: up to 5x main node or sub-node instances with EasyDMA UART: up to 5x instances with RTS/CTS flow control and EasyDMA I2C/TWI (TWI): up to 5x main node or sub-node instances with EasyDMA I2S: 2x instances ADC with up to 8x programmable gain channels PWM: up to 3 instances, 4 channels each. NFC tag: 1x instance QDEC: 2x instances Comparator and low-power comparator with wake-up from System OFF mode Timer/counter: up to 7x instances, 32-bit GRTC, 25 bit
Radio	
Supported 2.4 GHz radio modes	Bluetooth LE tested and verified against Bluetooth Core 6.0 IEEE 802.15.4 and 2.4 GHz proprietary modes
Bluetooth LE specification	
Operating channels and frequencies	40 channels, channel numbers 0–39, 2402–2480 MHz
Bluetooth LE data rates	1 Mbps 2 Mbps 500 kbps (Coded PHY, S=2) 125 kbps (Coded PHY, S=8))
Typical conducted output power	+6.7 dBm
Radiated output power	+6.7 dBm (including maximum antenna gain 0 dBi)
Conducted RX sensitivity, 1 Mbps	-94.9 dBm
Conducted RX sensitivity, 2 Mbps	-92.2 dBm
Conducted RX sensitivity, long range 500 kbps (Coded PHY, S=2)	-98 dBm
Conducted RX sensitivity, long range 125 kbps (Coded PHY, S=8)	-103 dBm
IEEE 802.15.4	
Operating channels and frequencies	16 channels, channel numbers 11-26, 2405–2480 MHz
IEEE 802.15.4 data rate	250 kbps
Conducted RX sensitivity, 250 kbps	-101 dBm
Other	Proprietary 2.4 GHz – 4 Mbps, 2 Mbps, and 1 Mbps

Table 2: ANNA-B50 series common characteristics summary

1.6 Software

The Open CPU architecture of ANNA-B50 series modules allows integrators to develop and run their own applications on the built-in Arm® Cortex®-M33 core. u-blox recommends the Nordic Semiconductor nRF Connect SDK [5] for development.

The nRF Connect SDK integrates the Zephyr Real-Time Operating System (RTOS), MCUboot secure bootloader, and Nordic Semiconductor's nrfxlib device drivers for the nRF54L15 and peripherals.

2 Interfaces

ANNA-B50 series supports a wide range of connectivity options, including a 2.4 GHz radio with an antenna connection, digital and analog I/O, and debug capabilities. The module provides full access to all GPIOs and peripheral interfaces available on the embedded nRF54L15, ensuring seamless integration into customer applications. For more information regarding function and use, see also the nRF54L15 datasheet [4].

2.1 Peripherals power domains

ANNA-B50 series features multiple Power Domains (PD) for low-power operation, including fast MCU and lower speed domains. Figure 2 shows the power domains supplying the integrated ARM Cortex processor, peripherals, and other functional units supported in ANNA-B50 modules, which feature:

- Different power domains support functional blocks that operate at different clock speeds
- Each power domain is mapped to one low-power Advanced Peripheral Bus (APB) that can be powered independently to connect peripherals to the system
- EasyDMA traffic from each domain is aggregated in a local AMBIX interconnect that can access RAMs in the fast MCU power domain.

Three of the power domains have their own GPIO ports. The GPIO pins can be used by peripherals in the same power domain. Selected port 2 pins, **P2.00-P2.10**, can be used for some serial interfaces in the peripheral domain SPIM, SPIS, and UARTE, as described in **Error! Reference source not found.**. For information about each instance's power domain and the related GPIOs, see Figure 2 and Table 6. Refer to nRF54L15 datasheet [4] for more information, and the interconnections between different power domains.

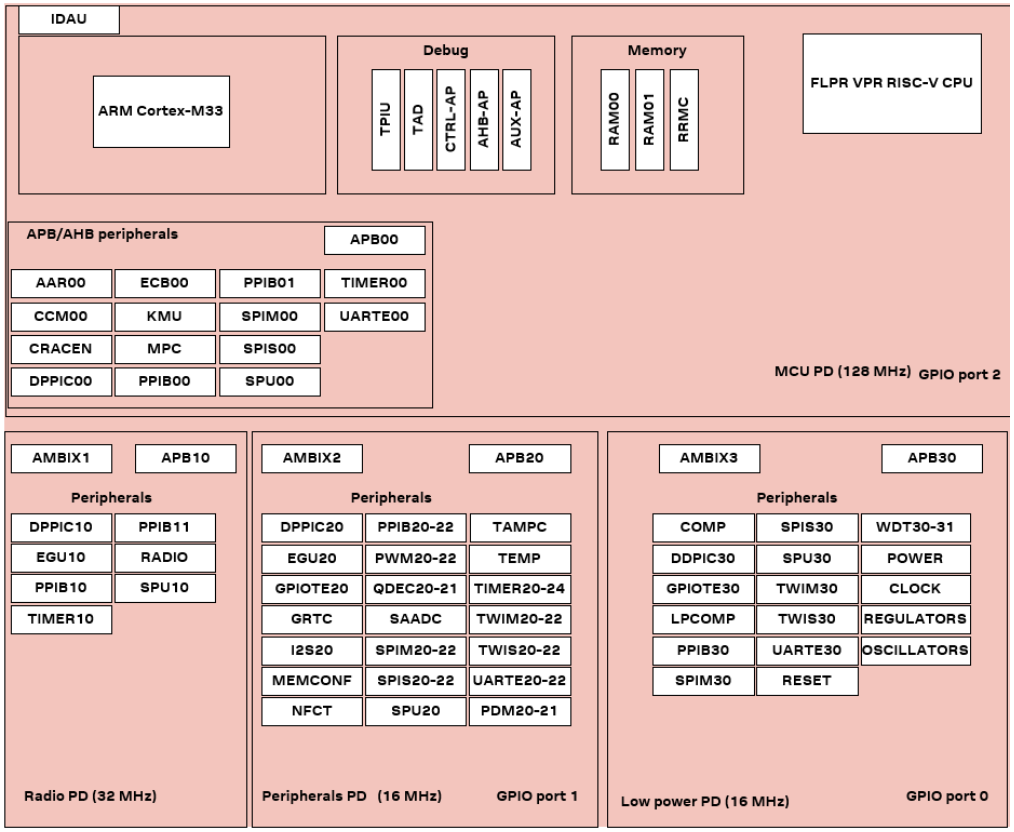


Figure 2: Power domains

2.1.1 Fast MCU domain

The fast MCU domain powers the Arm Cortex-M33 processor and its supporting debug system, which enables debugging and Embedded Trace Macrocell (ETM) tracing. The CPU executes program code from RRAM through an instruction cache. Data is stored in single-cycle RAMs, which are divided into multiple bus subordinates but form a continuous RAM space in the memory map. The fast domain also contains high-speed peripherals.

2.1.2 Lower speed domains

ANNA-B50 series has three lower speed power domains:

Radio domain – contains the short-range radio as well as supporting peripherals used by the radio protocol stack. The domain runs at 32 MHz synchronously with the fast domain.

Peripherals domain – contains most peripherals. The domain runs at 16 MHz synchronously with the Fast MCU domain.

Low Power domain – contains peripherals for ultra-low-power modes. These can be used to wake the rest of the system even when the peripheral domain is powered off. The domain runs at 16 MHz asynchronously to the fast domain.

2.2 Power management

ANNA-B50 series modules utilize integrated LDO and DC/DC regulators that maximize the power efficiency of the system. ANNA-B50 series has a main on-chip voltage regulator VREGMAIN, which converts the voltage supplied on VCC to internal voltage. VCC is also the reference voltage for the I/O signals.

2.3 System clocks

The clock control system sources the system clocks from internal or external high and low frequency oscillators. The system distributes the clocks based on the module requirements.

2.3.1 High-frequency clock HFCLK

ANNA-B50 includes a 32 MHz crystal oscillator that provides a high-quality reference clock for the Bluetooth LE radio system. This crystal also serves as the reference for generating the 64 MHz and 128 MHz system clocks via an internal PLL, supplying the CPU and other digital subsystems. The 32 MHz crystal oscillator relies on integrated tuning capacitors within the nRF54 chip. These capacitors are configured in the board file based on values determined by u-blox.

☞ The capacitor settings are specific to the ANNA-B50 module and must be used according to the reference configuration provided by u-blox.

Alternatively, the CPU clock (64 MHz or 128 MHz) can be derived from the internal high-frequency RC oscillator (HFINT), eliminating the need for an external crystal. However, this mode offers significantly lower frequency accuracy and worse phase noise and is not suitable for RF operation or timing-critical applications.

☞ See the system integration manual [1] for the recommended value of HFXO internal capacitance for ANNA-B50 modules.

2.3.2 Low-frequency LFCLK

A 32.768 kHz low-frequency clock is used by ANNA-B50 modules for various functions, including the timing of radio events, the global real-time counter (GRTC), and the watchdog timer (WDT). The choice of the LFCLK source depends on the accuracy required by the application. One of four sources is required for the low-frequency clock:

- RC oscillator (LFRC) – fully embedded in ANNA-B50 series and does not require external components
- Crystal oscillator (LFXO) – When greater than ± 500 ppm accuracy is required, an external 32.768 kHz crystal and optional loading capacitors must be added. Internal loading capacitors between 4 pF and 18 pF in 0.5 pF steps are also needed. The LFXO accuracy is dependent on the chosen crystal.
- External source – An externally generated 32.768 kHz clock source applied to **XL1**, and **XL2** pins. The accuracy of the clock is dependent on the external source.
- Synthesized clock (LFSYNT) – 32.768 kHz clock generated from the HFCLK, which assumes the accuracy is ±20 ppm. LFSYNT requires HFCLK to run, which results in higher-than-average power consumption.

2.4 RF antenna interfaces

2.4.1 2.4 GHz radio (ANT) and internal antenna (ANT_INT)

The RF pin (**ANT**) of ANNA-B50 series1 module is connected to the single-ended Tx/Rx antenna connection of the 2.4 GHz radio transceiver in nRF54L15 chip. The nRF54L15 chip has an integrated balun but requires an external filter/matching circuitry which is integrated inside of the ANNA-B50 series module. The RF pin (**ANT**) of the module is matched to 50 ohms.

The internal antenna pin (**ANT_INT**) of ANNA-B50 seriesis connected to the feeding point of the internal chip antenna in the module. Matching circuitry for the internal antenna is also integrated in the ANNA-B50 series module.

ANNA-B50 series module offers both internal and external antenna options:

- With the internal chip antenna option, the **ANT** pin shall be connected to the feeding point of the internal antenna through the **ANT_INT** pin of the module.
- When implementing an external antenna option, the external antenna or antenna connector shall be connected to **ANT** pin through a controlled impedance trace.

☞ For more information about the antennas that are approved for use with ANNA-B50 series, see also the system integration manual [1].

2.4.2 Near Field Communication (NFC)

ANNA-B50 series modules include an NFC interface, which is capable of operating as a 13.56 MHz NFC tag at a bit rate of 106 kbps. This interface supports EasyDMA for reading and writing of data packets to and from RAM. As an NFC tag, data can be read from or written to the ANNA-B50 modules using an NFC reader. However, ANNA-B50 modules are not capable of reading other tags or initiating NFC communications. The NFC interface can be used to wake the module from System OFF mode, which means that the module can wake from the deepest power save mode and still react to an NFC field. Two GPIO pins are available for connecting to an external NFC antenna: NFC1 and NFC2 pins.

2.4.3 Channel sounding

ANNA-B50 series supports channel sounding, which is a key feature of Bluetooth LE in the Bluetooth Core 6.0 specification. The feature enables accurate and secure distance measuring with built-in

security features and seamless interoperability. Channel sounding utilizes various ranging techniques and security measures to enable secure and accurate distance measurement between two devices – without increasing product complexity or size. Channel Sounding accuracy meets the requirements for applications such as smart door locks, home appliances, personal item tracking tags, or the presence detection of high-value assets in industrial and professional applications.

For more information, see also Channel Sounding at a glance on the Nordic website [6].

2.5 System functions

2.5.1 Power modes

ANNA-B50 series modules are power efficient devices capable of operating in different power saving modes and configurations. Different sections of the module can be powered off when they are not needed, and complex wake up events can be generated from different external and internal inputs.

The three main power modes are:

- System ON
- System ON IDLE sub-modes
- System OFF – lowest power consumption

Depending on applications, the module should spend most of its time in either System ON IDLE or System OFF mode to minimize current consumption.

2.5.2 System ON

System ON is the default operation after power-on reset. You can switch on or reboot the ANNA-B50 modules in one of the following ways:

- Rising edge on the **VCC** pin to a valid supply voltage
- Issuing a reset of the module. See also Module reset.

An event to wake up from the System OFF mode to the active mode can be triggered by:

- Programmable digital or analog sensor event. For example, a rising voltage level on an analog comparator pin
- Detecting an NFC field
- Debug session
- A pin RESET.

When waking up from System ON IDLE mode to System ON mode, an event can also be triggered by:

- GRTC on-board Global Real Time Counter
- Radio interface
- Detection of an NFC field

2.5.3 System ON idle sub-modes

In System ON operation, when the CPU and all peripherals are idle, the system can reside in one of the following power sub-modes:

- Constant latency – wakeup and task response are constant and kept at a minimum. This is secured by a set of resources that are always enabled.
- Low-power – lowest System ON power consumption.

2.5.4 System OFF

System OFF is the lowest power consumption mode the system can enter. The core functionality of the system is powered down and all ongoing tasks are terminated.

There is no dedicated pin to power off ANNA-B50 modules. Any available GPIO pin can be configured to trigger the application to enter System OFF mode which essentially powers down the module.

An under-voltage (brown-out) shutdown occurs on the ANNA-B50 modules when the **VCC** supply drops below the minimum limit of the operating range. If this occurs, it is not possible to store the current parameter settings in the non-volatile area of the module memory.

2.5.5 Module reset

There are several reset sources:

- **Power-on reset**: The power-on reset generator initializes the system when **VCC** rises above the power-on threshold.
- **Pin reset**: A pin reset is generated when the physical reset pin on the device is asserted.
- Pin reset is available on the reset pin **Pin 12** (**nRESET**).
- **Glitch detector**: The glitch detector (GLITCHDET) puts the system in a reset state if either the **VCC** supply voltage or the device's internal digital voltage drops below safe thresholds.
- **Brownout reset**: The system is placed in reset state if the **VCC** supply drops below the brownout threshold.
- **Wake from System OFF mode reset**: The system is reset when waking from System OFF mode.
- **Soft reset**: A soft reset is generated when the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR) in the Arm CPU is set. It can also be generated using CTRL-AP.
- **CTRL-AP reset**: CTRL-AP can generate the several resets, including Soft reset, Pin reset, and Hard reset – which is used during an erase-all operation and is less intrusive than Pin reset.
- **Watchdog timer (WDT) reset**: A watchdog timer (WDT) reset is generated when the watchdog timer times out.

2.5.6 CPU and memory

The integrated Nordic Semiconductor nRF54L15 chip in ANNA-B50 series modules includes powerful and fully programmable Arm Cortex-M33 processors, which feature a 32-bit instruction set (Thumb®-2 technology) with a superset of 16- and 32-bit instructions. For improved efficiency and power consumption, nRF54L15 also features an integrated **RISC-V** coprocessor that is designed to offload tasks from the primary Cortex-M33 core.

The processor includes an FPU, TrustZone® technology, and a full set of peripherals. It has a flash, and low-leakage RAM. refer to Table 1 for memory information. The CPU supports 128 MHz or 64 MHz speed

2.5.7 Direct Memory Access EasyDMA

Many of the peripherals described in this data sheet utilize Direct Memory Access (DMA), also known as EasyDMA, to provide a direct interface to the RAM – without involving the CPU. This ensures fluent operation of the CPU with minimal need for interruptions. DMA should be used whenever possible to reduce overall power consumption.

2.5.8 Distributed Programmable Peripheral Interconnect (DPPI)

ANNA-B50 series modules include a distributed programmable peripheral interconnect (DPPI). Functioning as a switch matrix, the DPPI connects various control signals between the different interfaces and system functions.

With DPPI, most interfaces can bypass the CPU to trigger a system function. Consequently, an incoming data packet can trigger a counter, falling voltage level on an ADC, or toggle a GPIO – without

having to interrupt the CPU. This facilitates the development of smart, power-efficient applications that wake up the CPU only when it is necessary.

2.5.9 Global Real-Time Counter (GRTC)

A key system feature available on the ANNA-B50 series is the Global Real-Time Counter which can operate in all power modes, including System OFF mode, and implement a shared system timer. This counter can generate multiple interrupts and events to the CPU, radio and internal and external hardware blocks. These events can be precisely timed ranging from microseconds up to 142 years and allow periodic Bluetooth LE advertising events without involving the CPU for example.

GRTC uses the 16 MHz clock when the high-speed clock is active but automatically switches to the low frequency clock in other power modes.

2.6 Serial peripherals

ANNA-B50 modules support the following serial communication interface:

- UART: Up to five instances with RTS/CTS flow control and EasyDMA/One high-speed up to 4 Mbps
- SPI: Up to five main node or sub node instances with EasyDMA/One high-speed SPIM up to 32 MHz
- QSPI: Emulated peripheral
- I2C/TWI (TWI): Up to five main node or sub node instances with EasyDMA up to 400 kHz
- I2S: Two channel Inter-IC sound interface

Most input/output pins on the module are shared between the digital interfaces, analog interfaces, and GPIOs. Unless otherwise stated, all functions can be assigned to any pin that is not already occupied.

2.6.1 Universal Asynchronous Receiver/Transmitter (UART)

The 4-wire UART interface supports hardware flow control with baud rates up to 4 Mbps. Up to five instances can be defined. For information about each instance, power domain and the related GPIOs, see Figure 2 and Table 6.

Other characteristics of the UART interface include:

- Pin configuration:
  - TXD: Transmit Data output pin
  - RXD: Receive Data input pin
  - RTS: Request To Send, flow control output pin (optional)
  - CTS: Clear To Send, flow control input pin (optional)
- Full-duplex operation
- EasyDMA direct transfer to/from RAM
- Individual selection of I/O pins
- Four slow instances with up to 1 Mbps baud rate/ one fast up to 4 Mbps
- Optional even/odd parity bit checking and generation
- One or two stop bits/ Configurable data frame size: 4-bit to 9-bit
- 9-bit support mode with address matching in RX
- Hardware flow control or no flow control is supported.
- Return to IDLE between transactions supported (when using HW flow control)

2.6.2 Serial Peripheral Interface (SPI)

ANNA-B50 modules support up to five Serial Peripheral Interfaces with serial clock frequencies of up to 32 MHz, with EasyDMA, and Individual selection of I/O pins. Other characteristics of the SPI interfaces include:

- Pin configuration in Main node mode:
  - **SCLK**, Serial clock output, up to 32 MHz for SPIM00, and 8 MHz for SPIM2x/30.
  - **MOSI**, Main node output to Sub node input data line
  - **MISO**, Main node Input from Sub node output data line
  - **CS**, Chip select output, active low, selects which peripheral on the bus to talk to. Only one select line is enabled by default but more can be added by customizing a GPIO pin.
  - **DCX**, Data/Command signal. An optional signal used by SPI Sub nodes to distinguish between SPI commands and data
- Pin configuration in Sub mode:
  - **SCLK**, Serial clock input
  - **MOSI**, Main node Output to Sub node Input data line
  - **MISO**, Main node Input from Sub node Output data line
  - **CS**, Chip select input, active low, connects/disconnects the interface from the bus.
- Both Main node and Sub node modes are supported on all interfaces.
- The serial clock supports both normal and inverted clock polarity (CPOL) and data can be captured on rising or falling clock edge (CPHA).

2.6.3 SPIM and SPIS shared resources

The SPI Main (SPIM), SPI Sub (SPIS) interfaces share registers and other resources with other peripherals that have the same ID as the SPIM or SPIS. Therefore, the user must disable all peripherals with the same ID as the SPIM and SPIS before the interfaces can be configured and used.

Disabling a peripheral that has the same ID as the SPIM or SPIS, does not reset any of the registers that are shared with these interfaces. It is therefore important to configure all relevant SPIM and SPIS registers explicitly to ensure that they operate correctly. For more information about the peripherals and their IDs, see the instantiation table included in the nRF54L15 datasheet [4].

2.6.4 Quad Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) can be used to connect an external memory to the ANNA-B50 module.

QSPI always operates in main node mode using the following pin configuration:

- **CLK**, serial clock output
- **CS**, chip select output, active low, selects which peripheral on the bus to talk to
- **D0**, serial output, Main Out Sub In (MOSI) data in single mode, data I/O signal in dual/quad mode
- **D1**, serial input, Main In Sub Out (MISO) data in single mode, data I/O signal in dual/quad mode
- **D2**, data I/O signal in quad mode (optional)
- **D3**, data I/O signal in quad mode (optional)

For information about each power domain and their associated GPIOs, see Figure 2 and Table 6.

2.6.5 Inter-Integrated Circuit interface (I2C/TWI)

The Inter-Integrated Circuit (I2C/TWI) interfaces can be used to transfer and/or receive data on a 2-wire bus network. ANNA-B50 modules can operate as both Controller and Target nodes on the

I2C/TWI bus, using 100 kbps (standard), 400 kbps, and 1000 kbps transmission speeds with EasyDMA, and Individual selection of I/O pins. The interface supports clock stretching, which allows ANNA-B50 modules to temporarily pause any I2C/TWI communication. Up to 127 individually addressable I2C/TWI devices can be connected to the same two signals.

Pin configuration:

- **SCL**, clock output in Controller node, input in Target node
- **SDA**, data input/output pin

To work properly in the main node mode the I2C/TWI requires external pull-up resistors referenced to **VCC**. Pull-up resistors referenced to **VCC** are required in the Target node as well, but these should be placed at the Controller node end of the interface. The I2C/TWI specification allows a line capacitance of 400 pF at most. For information about the value of internal pullup resistor (R_{pu}) for use with ANNA-B50 modules, see Digital pins.

In Controller or Target nodes, the I2C/TWI shares registers and other resources with other peripherals that have the same ID as the I2C/TWI. Therefore, the user must disable all peripherals that have the same ID as the I2C/TWI before the I2C/TWI can be configured and used. Disabling a peripheral that has the same ID as the I2C/TWI will not reset any of the registers that are shared with the I2C/TWI. Therefore, it is important to configure all relevant I2C/TWI registers explicitly to ensure that they operate correctly.

For more information about peripherals and their IDs, see the instantiation table in the nRF54L15 Datasheet [4].

2.6.6 Inter-IC Sound interface (I2S)

The Inter-IC Sound (I2S) interface transfers audio sample streams between ANNA-B50 modules and external audio devices such as codecs, DACs, and microphones. It supports standard I2S, left- or right-aligned interface formats in both Controller and Target nodes, and features EasyDMA for efficient data transfer. The I2S pins can also be individually assigned to different GPIOs.

Pin configuration:

- **MCK**, Main clock
- **LRCK**, Left Right/word/sample clock
- **SCK**, Serial Clock
- **SDIN**, Serial Data In
- **SDOUT**, Serial Data Out

The Controller side of an I2S interface always provides the **LRCK** and **SCK** clock signals, but some Controller node devices can't generate a **MCK** clock signal. For external systems that are unable to generate their own clock signal, ANNA-B50 can supply a **MCK** clock signal in both the Controller and Target. The two data signals, **SDIN** and **SDOUT**, allow simultaneous bi-directional audio streaming. The interface supports 8, 16, 24 and 32-bit sample widths with up to 48 kHz sample rate.

2.7 Digital peripherals

2.7.1 Pulse Width Modulation (PWM)

ANNA-B50 modules provide up to three PWM units – each with four PWM channels and with EasyDMA, that can be used to generate complex waveforms. These waveforms can be used for controlling motors, dimming LEDs, or functioning as audio signals when connected to speakers. Duty-cycle sequences can be stored in RAM and repeated or connected into loops. The duty-cycle values can be updated autonomously and glitch-free directly from memory through EasyDMA – without CPU intervention. Each channel uses a single GPIO pin as output.

2.7.2 Quadrature Decoder (QDEC)

ANNA-B50 modules provide up to two QDEC units that read quadrature encoded data from mechanical and optical sensors in the form of digital waveforms. Quadrature encoded data is often used to indicate the rotation of a mechanical shaft in either a positive or negative direction. The QDEC uses two inputs, **PHASE_A** and **PHASE_B**, and an optional LED output signal. The interface has a selectable sample period ranging from 128 µs to 131 ms.

2.8 Analog interfaces

8 out of the 31 digital GPIOs can be multiplexed to analog functions, including:

- 1x 8-channel ADC[1] with the sampling rates: 14-bit at 31.25 ksps, 12-bit at 250 ksps, and up to 10-bit at 2 Msps.
- 1x Analog comparator
- 1x 8-channel Low-power analog comparator

2.8.1 Successive approximation Analog to Digital Converter (SAADC)

The Analog to Digital Converter (ADC) is used to sample analog voltage on the analog function enabled pins of the ANNA-B50 module. Any of the 8 analog inputs can be used.

Characteristics of the ADC include:

- Three modes, 10-bit at 2 MS/s, 12-bit at 250 KS/s, or 14-bit at 31.25 MS/s
- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Full swing input range of 0 V to **VCC**
- Support for direct sample transfer to RAM using EasyDMA
- Single ended or continuous sampling
- Two operation modes: Single-ended or Differential
    - Single-ended mode, where a single input pin is used
    - Differential mode, where two inputs sample the voltage level difference between them

If the sampled signal level is much lower than the VCC, it is possible for the programmable gain factor of the ADC to better encompass the required signal. This produces a higher effective resolution. Continuous sampling can be configured for specific time intervals or at different internal or external events – without CPU involvement.

2.8.2 SAADC shared resources

The ADC can coexist with COMP and other peripherals using one of AIN0-AIN7, provided these are assigned to different pins.

2.8.3 Comparator (COMP)

The analog comparator compares the analog voltage on one of the analog-enabled pins in ANNA-B50 module with a highly configurable internal or external reference voltage. Events can be generated and distributed to the rest of the system when the voltage levels cross.

Further characteristics of the comparator include:

- Full swing input range of 0 V to VCC.
- Two operation modes: Single-ended or Differential

[1] Each analog pin may only be assigned to one function at any given time, ADC, COMP, or LPCOMP

Single-ended mode

- A single reference level or an upper and lower hysteresis
- Selectable from a 64-level reference ladder with a range from 0 V to VREF, as described in Table 3.

Differential mode

- Two analog pin voltage levels are compared, optionally with configurable hysteresis.
- Two selectable speed/power performance modes: Low power and High speed.

The COMP shares analog resources with other analog peripherals. It also shares registers and other resources with other peripherals with the same ID as the COMP. For further information about the peripherals and their IDs, see also the instantiation table in the nRF54L15 Datasheet [4]. The COMP peripheral must not be disabled (through write operations to the ENABLE register) before the peripheral has stopped. Failing to do so can result in unpredictable module behavior.

2.8.4 Low power comparator (LPCOMP)

In addition to the power save mode available for the comparator, there is also a separate low power comparator (LPCOMP) available on the ANNA-B50 module. The LPCOMP allows for an even lower power operation – with slightly reduced performance and fewer configuration options.

Characteristics of the low power comparator include:

- Full swing input range of 0 to **VCC**
- Two operation modes, Single-ended mode and Differential mode

  Single-ended mode

  - The reference voltage **LP_VIN–** is selected from a 15-level reference ladder

  Differential mode

  - Pin **P1.04/AIN0** or **P1.05/AIN1** is used as reference voltage **LP_VIN–**
  - Can be used to wake the system from System OFF or Sleep mode

Since the run current of the low power comparator is very low, it can be used as an analog trigger to wake up the CPU during the module sleep mode. See also Power modes. For information about power domain and related GPIOs, see Figure 2 and Table 6.

For a summary of the analog pin options, see also Table 3.

LPCOMP shares analog resources with SAADC. While it is possible to use the SAADC at the same time as the LPCOMP, selecting the same analog input pin for both modules is not supported.

Additionally, LPCOMP shares registers and other resources with other peripherals with the same ID as LPCOMP. For more information about the peripherals and their IDs, see the instantiation table in the nRF54L15 Datasheet [4]. The LPCOMP peripheral should not be disabled (through write operation to the ENABLE register) before the peripheral has stopped. Failing to do so may result in unpredictable behavior.

2.8.5 Analog pin options

Table 3 shows the supported connections of the analog functions.

☞ An analog pin must not be simultaneously connected to multiple functions.

Symbol	Analog function	Can be connected to
ADCP	ADC single-ended or differential positive input	AIN0 to AIN7 pin or **VCC**
ADCN	ADC differential negative input	AIN0 to AIN7 pin or **VCC**
VIN+	Comparator input	AIN0 to AIN7 pin

Symbol	Analog function	Can be connected to
VREF	Comparator single-ended mode reference ladder input	AIN0 to AIN7 pin, **VCC**, 1.2 V internal reference
VIN-	Comparator differential mode negative input	AIN0 to AIN7 pin in differential mode, VREF in single ended mode
LP_VIN+	Low-power comparator IN+	AIN0 to AIN7 pin
LP_VIN-	Low-power comparator IN-	**P1.04/AIN0** or **P1.05/AIN1**, 1/16 to 15/16 **VCC** in steps of 1/16 **VCC,** External selected reference.

Table 3: Possible uses of the analog pins

2.9 GPIO

ANNA-B50 series modules have a versatile pin-out. With no dedicated analog or digital interfaces, all module interfaces or functions must then be allocated to a GPIO pin before use.

In an un-configured state, ANNA-B50 modules support a total of 32 GPIO pins. 8 out of the 32 GPIO pins are analog capable, which means that they can have analog functions allocated to them. Table 6 shows the number of digital and analog functions that can be assigned to a GPIO pin.

2.9.1 GPIO ports and capabilities

ANNA-B50 power domains have their own GPIO ports with different capabilities.

Supported GPIO ports in the system, include:

- Port 0: In the low-power domain, this port can wake the system up from System OFF or System ON sleep and can be accessed by all peripherals in the low-power domain.
- Port 1: In the peripheral domain, this port can wake the system up from System OFF or System ON sleep and can be accessed by all peripherals in the peripheral domain.
- Port 2: In the MCU domain, this port has faster pins and can be used for high-speed signals, such as trace or fast serial peripheral communication. GPIO on Port 2 can't wake the system from sleep. Port 2 doesn't have a GPIO SENSE or DETECT mechanism and has no GPIO tasks and events (GPIOTE).

Table 4 describes the port's special functions and characteristics.

Port	Wakeup source	Extra drive strength (E0E1)	Pin sense/Detect	GPIOTE	Speed (MHz)
Port 0	Yes	No	Yes	Yes	8
Port 1	Yes	No	Yes	Yes	8
Port 2	No	Yes	No	No	64

Table 4: Port Capabilities

☞ **P1.00/XL1** and **P1.01/XL2** default to GPIO but can be configured to connect an external 32.768 kHz crystal circuit.

☞ **P1.02/NFC1** and **P1.03/NFC2** default to NFC but can also be configured to operate as GPIO.

⚠ Do not apply NFC field to NFC pins when they are configured as GPIOs. Failure to observe this can cause permanent damage to the module.

⚠ When driving different logic levels on these pins in the GPIO mode, a small current leakage occurs. Make sure these pins are set to the same logic level before entering any of the power saving modes.

☞ **P1.08** default to GPIO but can be configured to external reference for **SAADC**

2.9.2 Drive strength

All GPIO pins are normally configured for low current consumption. Using this standard drive strength, a pin configured as an output can only source or sink a certain amount of current.

If the timing requirements of a digital interface can't be met or if an LED requires more current, an extra drive strength mode is available on port 2 pins. This allows the digital output to draw more current. In addition to drive strength, GPIO pins configured for output can be set for push-pull or open-drain. GPIO pins configured for input can float or enable internal pull-up or pull-down resistors. For more information about the digital GPIO characteristics and extra drive strength values, see Table 16.

Table 5 shows GPIO custom functions configuration.

Function	Description	Configurable GPIOs
General purpose input	Digital input with configurable pull-up, pull-down, edge detection and interrupt generation	Any
General purpose output	Digital output with configurable drive strength, push-pull or open drain output	Any
Pin disabled	Pin is disconnected from the input and output buffers	Any
Timer/ counter	High-precision time measurement between two pulses/ Pulse counting with interrupt/event generation	Any, in the same domain
Interrupt/ Event trigger	Interrupt/event trigger to the software application	Any
HIGH/LOW/Toggle on event	Programmable digital level triggered by internal or external events without CPU involvement	Any
ADC input	8/10/12/14-bit analog to digital converter	Any analog
Analog comparator input	Compares two voltages. Capable of generating wake-up events and interrupts	Any analog
PWM output	Simple output or complex pulse-width modulation waveforms	Any, in the same domain

Table 5: GPIO custom functions configuration

2.10 Debug interface

2.10.1 Serial Wire Debug (SWD)

ANNA-B50 series modules provide ARM Multi-drop SWD technology for flashing and debugging. Through two-pin serial SWD signals, **SWDIO** and **SWDCLK**. Additionally, ANNA-B50 modules can be driven over the same SWD interface to other CPUs that support SWD.

2.10.2 Parallel trace

ANNA-B50 series modules support parallel trace output. This facilitates output from the Embedded Trace Macrocell (ETM) and Instrumentation Trace Macrocell (ITM) embedded in the Arm Cortex-M33 integrated in ANNA-B50 modules. The ETM trace data allows a user to record exactly how the application processes the CPU instructions in real time.

In addition to parallel trace, the ANNA-B50 modules support serial trace through the serial wire output SWO trace protocol. Parallel and serial trace can't be used at the same time. ETM trace is only supported in parallel trace mode. ITM trace is supported in both parallel and serial trace mode.

Trace pins are multiplexed with GPIOs. **SWO** and **TRACEDATA[0]** can use the same GPIO. **SWO** pin can also use a separate GPIO on Port 2.

The parallel trace interface uses one clock signal and four data signals respectively: **TRACE_CLK**, **TRACE_D0**, **TRACE_D1**, **TRACE_D2,** and **TRACE_D3**. For more information about the shared assignments of the GPIO pins, see the Pinout.

3 Pin definition

Following chapters describe the module pin layout and functions.

3.1 ANNA-B50 pin assignment

Figure 3 describes the pin layout and pin number assignments.

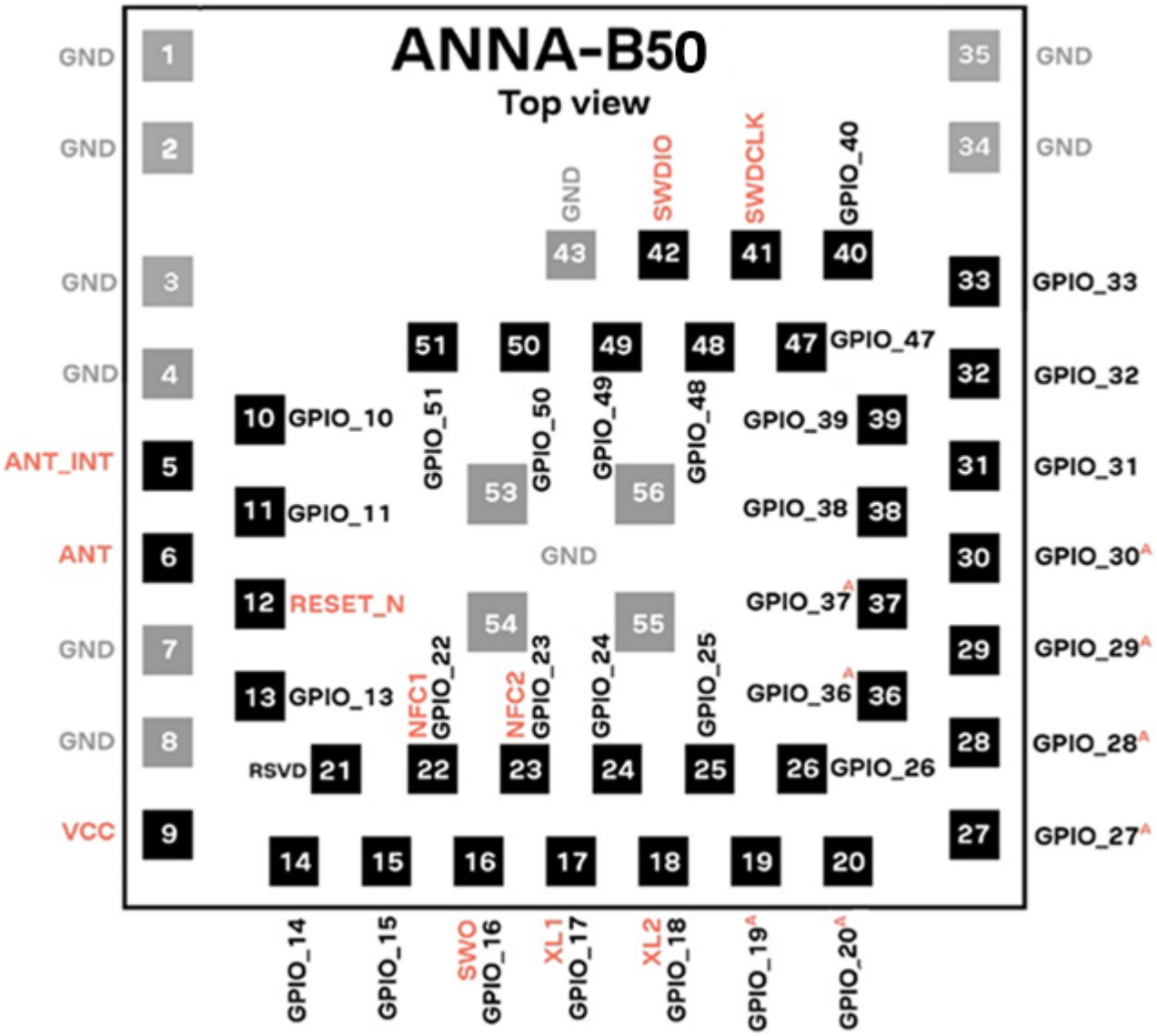


Figure 3: Pin assignment (top view)

GND pins are shown in gray in Figure 3

Signals shown in red are not freely assignable but are fixed to a specific pin.

3.2 Pinout

Table 6 describe the module pinout. GPIO pin routing and configuration are flexible. Some pins are dedicated to specific purposes, and some peripheral signals must use dedicated clock pins. If the same pin number (no.) is repeated on two or more rows it means the pin has mutually exclusive alternative functions.

See nRF54L15 datasheet [4] for further details, including limitations and recommendations, and information about the clock pins, dedicated pins and cross power-domain use.

No.	Name	Function	Description	Dedicated function	Clock pin	Remarks
1	GND (VSS)	Ground	Ground			
2	GND (VSS)	Ground	Ground			
3	GND (VSS)	Ground	Ground			
4	GND (VSS)	Ground	Ground			
5	ANT_INT	Antenna	Feeding to internal antenna of the module			Connect to ANT pin if the internal antenna is used. See also 2.4 GHz radio (ANT) and internal antenna (ANT_INT).
6	ANT	Antenna	Tx/Rx antenna interface			50 Ω nominal characteristic impedance. Connect to ANT_INT pin if the internal antenna is used. See also 2.4 GHz radio (ANT) and internal antenna (ANT_INT).
7	GND (VSS)	Ground	Ground			
8	GND (VSS)	Ground	Ground			
9	VCC (VDD)	Power	Module supply voltage input			
10	P0.00	Digital I/O	General purpose I/O			
11	P0.02	Digital I/O	General purpose I/O			
12	RESET_N (nRESET)	Reset	Pin reset			On-chip pull-up
13	P2.10	Digital I/O	General purpose I/O			
		Digital I/O	FLPR.10	FLPR		
14	P2.09	Digital I/O	General purpose I/O			
		Digital I/O	FLPR.9	FLPR		
15	P2.08	Digital I/O	General purpose I/O			
		Digital I/O	FLPR.8	FLPR		
	TRACEDATA[1]	Digital I/O	Trace data	Trace		
		Digital I/O	SPIM SDO	SPIM00/21		
		Digital I/O	SPIS SDO	SPIS00/21		
		Digital I/O	UARTE TXD	UARTE00/21		
16	P2.07	Digital I/O	General purpose I/O			
		Digital I/O	FLPR.7	FLPR		
	TRACEDATA[0]	Digital I/O	Trace data	Trace		
	SWO	Digital I/O	Serial wire output (SWO)	Trace		
		Digital I/O	SPIM DCX	SPIM00/21		
		Digital I/O	UARTE RXD	UARTE00/21		
17	P1.00	Digital I/O	General purpose I/O			
	XL1	Analog input	Connection for 32.768 kHz crystal			
18	P1.01	Digital I/O	General purpose I/O			
	XL2	Analog input	Connection for 32.768 kHz crystal			

No.	Name	Function	Description	Dedicated function	Clock pin	Remarks
19	P1.04	Digital I/O	General purpose I/O		Yes	
	ASO[0]	Digital I/O	TAMPC active shield 0 output	TAMPC		
	AIN0	Analog input	Analog input			
20	P1.05	Digital I/O	General purpose I/O			
	ASI[0]	Digital I/O	TAMPC active shield 0 input	TAMPC		
	RADIO[6]	Digital I/O	RADIO DFEGPIO	RADIO		
	AIN1	Analog input	Analog input			
21	-	-	No connection			
22	P1.02	Digital I/O	General purpose I/O			See warning in GPIO ports and capabilities
	NFC1	NFC input	NFC antenna connection			
23	P1.03	Digital I/O	General purpose I/O		Yes	See warning in GPIO ports and capabilities
	NFC2	NFC input	NFC antenna connection	NFC		
24	P2.00	Digital I/O	General purpose I/O			
		Digital I/O	SPIM DCX	SPIM00/20		
		Digital I/O	UARTE RXD	UARTE00/20		
		Digital I/O	FLPR.4	FLPR		
		Digital I/O	QSPI D3	FLPR (QSPI)		
25	P2.02	Digital I/O	General purpose I/O			
		Digital I/O	SPIM SDO	SPIM00/20		
		Digital I/O	SPIS SDO	SPIS00/20		
		Digital I/O	UARTE TXD	UARTE00/20		
		Digital I/O	FLPR.1	FLPR		
		Digital I/O	QSPI D0	FLPR (QSPI)		
26	P0.01	Digital I/O	General purpose I/O			
27	P1.14	Digital I/O	General purpose I/O			
	RADIO[5]	Digital I/O	RADIO DFEGPIO	RADIO		
	AIN7	Analog input	Analog input			
28	P1.13	Digital I/O	General purpose I/O			
	RADIO[4]	Digital I/O	RADIO DFEGPIO	RADIO		
	AIN6	Analog input	Analog input			
29	P1.12	Digital I/O	General purpose I/O		Yes	
	ASI[3]	Digital I/O	TAMPC active shield 3 input	TAMPC		
	RADIO[3]	Digital I/O	RADIO DFEGPIO	RADIO		
	AIN5	Analog input	Analog input			
30	P1.11	Digital I/O	General purpose I/O		Yes	
	ASO[3]	Digital I/O	TAMPC active shield 3 output	TAMPC		
	RADIO[2]	Digital I/O	RADIO DFEGPIO	RADIO		
	AIN4	Analog input	Analog input			
31	P1.15	Digital I/O				
32	P0.04	Digital I/O	General purpose I/O		Yes	
		Digital I/O	GRTC CLKOUT32K	GRTC		

No.	Name	Function	Description	Dedicated function	Clock pin	Remarks
33	P1.09	Digital I/O	General purpose I/O			
	ASO[2]	Digital I/O	TAMPC active shield 2 output	TAMPC		
	RADIO[0]	Digital I/O	RADIO DFEGPIO	RADIO		
34	GND (VSS)	Ground	Ground			
35	GND (VSS)	Ground	Ground			
36	P1.06	Digital I/O	General purpose I/O			
	ASO[1]	Digital I/O	TAMPC active shield 1 output	TAMPC		
	AIN2	Analog input	Analog input			
37	P1.07	Digital I/O	General purpose I/O			
	ASI[1]	Digital I/O	TAMPC active shield 1 input	TAMPC		
	AIN3	Analog input	Analog input			
38	P2.05	Digital I/O	General purpose I/O			
		Digital I/O	SPIM CSN	SPIM00/20		
		Digital I/O	SPIS CSN	SPIS00/20		
		Digital I/O	UARTE RTS	UARTE00/20		
		Digital I/O	FLPR.5	FLPR		
		Digital I/O	QSPI CSN	FLPR (QSPI)		
39	P2.01	Digital I/O	General purpose I/O		Yes	
		Digital I/O	SPIM SCK	SPIM00/20		
		Digital I/O	SPIS SCK	SPIS00/20		
		Digital I/O	FLPR.0	FLPR		
		Digital I/O	QSPI SCK	FLPR (QSPI)		
40	P1.10	Digital I/O	General purpose I/O			
	ASI[2]	Digital I/O	TAMPC active shield 2 input	TAMPC		
	RADIO[1]	Digital I/O	RADIO DFEGPIO	RADIO		
41	SWDCLK	Debug	Serial wire clock			Input with on-chip pull-down
42	SWDIO	Debug	Serial wire data			Bidirectional with standard-drive and on-chip pull-up
43	GND (VSS)	Ground	Ground			
47	P0.03	Digital I/O	General purpose I/O		Yes	
		Digital I/O	GRTC PWM	GRTC		
48	P2.06	Digital I/O	General purpose I/O		Yes	
		Digital I/O	FLPR.6	FLPR		
		Digital I/O	SPIM SCK	SPIM00/21		
		Digital I/O	SPIS SCK	SPIS00/21		
	TRACECLK	Digital I/O	Trace clock	Trace		
49	P2.03	Digital I/O	General purpose I/O			
		Digital I/O	FLPR.3	FLPR		
		Digital I/O	QSPI D2	FLPR (QSPI)		

No.	Name	Function	Description	Dedicated function	Clock pin	Remarks
50	P2.04	Digital I/O	General purpose I/O			
		Digital I/O	SPIM SDI	SPIM00/20		
		Digital I/O	SPIS SDI	SPIS00/20		
		Digital I/O	UARTE CTS	UARTE00/20		
		Digital I/O	FLPR.2	FLPR		
		Digital I/O	QSPI D1	FLPR (QSPI)		
51	P1.08	Digital I/O	General purpose I/O		Yes	
		Digital I/O	GRTC CLKOUTFAST			
	EXTREF	Analog input	External reference for SAADC			
	P1.08	Digital I/O	General purpose I/O			
53	GND (VSS)	Ground	Ground			
54	GND (VSS)	Ground	Ground			
55	GND (VSS)	Ground	Ground			
56	GND (VSS)	Ground	Ground			

Table 6: ANNA-B50 pinout

4 Electrical specifications

⚠ Stressing the device above one or more of the absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the recommended operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Signal	Description	Condition	Min	Max	Unit
VCC	Module supply high voltage	Input DC voltage at VCC pin	-0.3	3.9	V
GND				0	V
$V_{I/O}$	Digital pin voltage	VCC ≤ 3.6 V	-0.3	VCC + 0.3	V
$V_{I/O}$	Digital pin voltage	VCC > 3.6 V	-0.3	3.9	V
P_ANT	Maximum power at the receiver	Input RF power at the antenna pin		0	dBm
$I_{NFC1/2}$	NFC Antenna pin current	Input current at NFC pin		130	mA

Table 7: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. Use appropriate protection devices to ensure that voltage spikes exceeding the power supply voltage specifications in Table 7 are kept within the specified limits.

4.1.1 Maximum ESD ratings

Parameter	Min	Typical	Max	Unit	Remarks
ESD sensitivity for all pins except ANT pin			3	kV	Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).
ESD sensitivity for all pins except ANT pin			250	V	Charged device model according to JESD22-C101

Table 8: Maximum ESD ratings

⚠ ANNA-B50 series modules are Electrostatic Sensitive Devices and require special precautions while handling. For ESD handling instructions, refer to also ESD precautions.

4.1.2 NVM memory endurance

Parameter	Value	Unit
Endurance	10 000	Write/rewrite cycles
Retention	10	Years at [85] °C

Table 9: NVM memory endurance

4.2 Recommended operating conditions

☞ Unless otherwise specified, all given specifications have been measured at an ambient temperature of 25 °C with a supply voltage of 3.3 V.

⚠ Operation beyond the specified operating conditions is not recommended and extended exposure beyond them may affect device reliability.

4.2.1 Operating and storage temperature range

Parameter	Min	Typ	Max	Unit
Storage temperature	–40		+105	°C
Operating temperature	–40	+25	+85	°C

Table 10: Temperature range

4.2.2 Supply/power pin

Symbol	Parameter	Min	Typ	Max	Unit
VCC	ANNA-B50 module supply voltage	1.7	-	3.6	V
VCCPOR	VCC supply voltage during power-on reset	1.75			V

Table 11: Input characteristics of voltage supply pins

4.2.3 Current consumption

Table 12 shows the typical current consumption of an ANNA-B50 module at 3.0 V supply, independent of the software used.

Condition	Min	Typ	Max	Unit
Radio RX only @ 1 Mbps Bluetooth LE mode		3.4		mA
Radio RX only @ 2 Mbps Bluetooth LE mode		3.4		mA
Bluetooth LE TX 1 Mbps at 0 dBm		4.8		mA
Bluetooth LE TX 1 Mbps at +4 dBm		6.6		mA
Bluetooth LE TX 1 Mbps at +6.7 dBm (maximum power setting)		9.8		mA

Table 12: ANNA-B50 VCC current consumption

4.2.4 RF performance

Parameter	Test condition	Min	Typ	Max	Unit
	Bluetooth LE mode				
Receiver input sensitivity*	Conducted at 25 °C, 1 Mbit/s Bluetooth LE mode		-94.9		dBm
	Conducted at 25 °C, 2 Mbit/s Bluetooth LE mode		-92.2		dBm
	Conducted at 25 °C, 500 kbit/s Bluetooth LE mode		-98		dBm
	Conducted at 25 °C, 125 kbit/s Bluetooth LE mode		-103		dBm
Maximum output power**	Conducted at 25 °C		+6.7		dBm
	IEEE 802.15.4 mode				
Receiver input sensitivity*	Conducted at 25 °C, 250 kbit/s		-101		dBm
Maximum output power**	Conducted at 25 °C, 250 kbit/		+6.7		dBm
	Antenna				
ANNA-B505 antenna gain	Integral to EVK-ANNA-B505		0		dBi

*Conducted test on EVK-ANNA-B505 evaluation board configured with external antenna connector, with 3.0 V supply voltage at 25 °C.

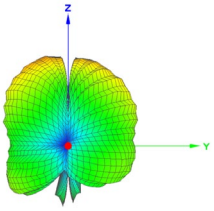
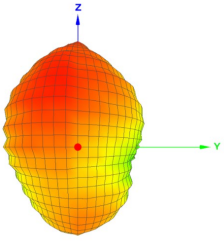
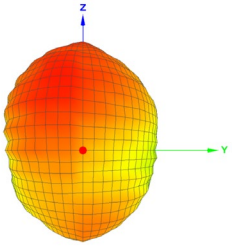
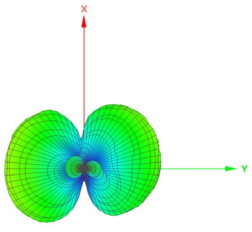
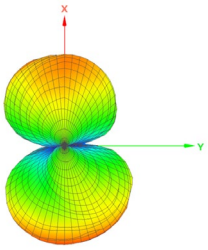
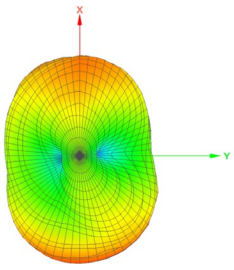
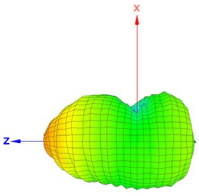
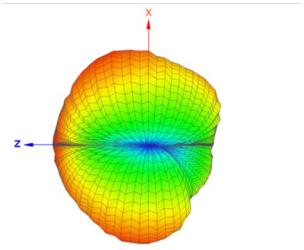
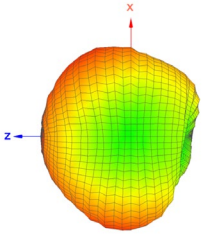
Table 13: ANNA-B50 RF performance

4.2.5 Antenna radiation patterns

Figure 4 provides an overview of the measurement procedure and describes how the ANNA-B505 module is aligned to the XYZ-coordinate system. A measurement is taken at every dotted position above the module image (shown left). Each measurement is represented as a grid point in the radiation pattern (shown right).

Figure 4: Spherical test points

Table 14 describes the radiation patterns for ANNA-B505. The antenna radiation test setup utilizes the reference design that comprises an evaluation board with ANNA-B505 situated in the middle of the EVK-ANNA-B505 board.

View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
	Antenna Gain (dBi) -25 -18 -12 -6 0		
Top view, YZ plane positivw X direction 			
Side view, XY plane negative Z direction 			
Side view, XZ plane negative Y direction 			

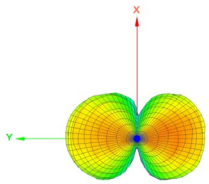
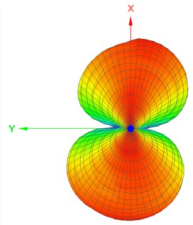
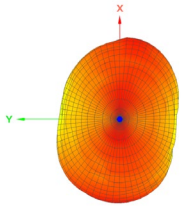
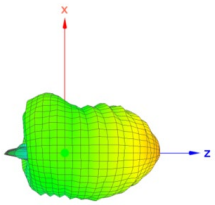
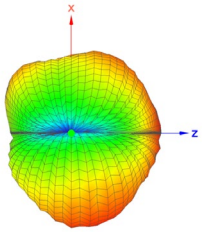
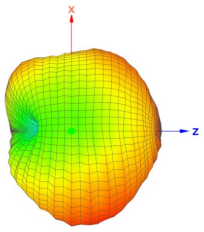
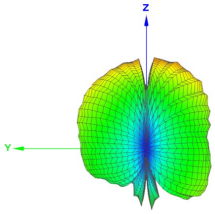
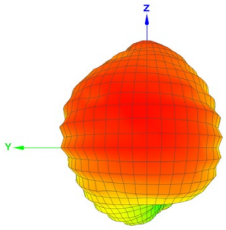
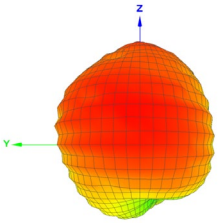
View	Vertical polarization	Horizontal polarization	Total (Vertical + Horizontal)
	Antenna Gain (dBi) -25 -18 -12 -6 0		
Side view, XY plane positive Z direction			
Side view, XZ plane positive Y direction			
Bottom view, YZ plane negative X direction			

Table 14: ANNA-B505 antenna radiation patterns

4.2.6 RESET_N pin

Pin name	Parameter	Min	Typ	Max	Unit
RESET_N	Time measured as time in power-on reset after supply reaches minimum operating voltage, with VCC rise time from 1 µs to 100ms		0.2	2	ms

Table 15: RESET_N pin characteristics

4.2.7 Digital pins

Condition	Min	Typ	Max	Unit
Input high voltage	0.7 x VCC		VCC	V
Input low voltage	GND		0.3 x VCC	V
Output high voltage, standard drive, 0.5 mA, VCC ≥1.7	VCC-0.4		VCC	V
Output high voltage, high drive, 5 mA, VCC >= 2.7 V	VCC-0.4		VCC	V
Output high voltage, high drive, 3 mA, VCC >= 1.7 V	VCC-0.4		VCC	V

Condition	Min	Typ	Max	Unit
Output low voltage, standard drive, 0.5 mA, VCC ≥1.7	GND		GND+0.4	V
Current at GND+0.4 V, output set low, standard drive, VCC ≥1.7	1	3	4	mA
Current at GND+0.4 V, output set low, high drive, VCC >= 1.7 V	3			mA
Current at GND+0.4 V, output set low, extra drive, VCC >= 1.7 V	16			mA
Current at VCC-0.4 V, output set high, standard drive, VCC ≥1.7	1	3	4	mA
Current at VCC-0.4 V, output set high, high drive, VCC >= 1.7 V	4			mA
Current at VCC-0.4 V, output set high, extra drive, VCC >= 1.7 V	14			mA
Recommended maximum sustained current drawn by all GPIOs			15	mA
Rise/Fall time, high drive mode, 20-80%, 12 pF load		4		ns
Rise/Fall time, extra drive mode, 20-80%, 12 pF load		0.9		ns
Pull-up resistance	12	14	16	kΩ
Pull-down resistance	12	14	18	kΩ

Table 16: Digital pin characteristics

5 Mechanical specifications

5.1 ANNA-B50 footprint dimensions

Figure 5 shows a side view of the mechanical outline and the critical dimensions of the ANNA-B50 module package.

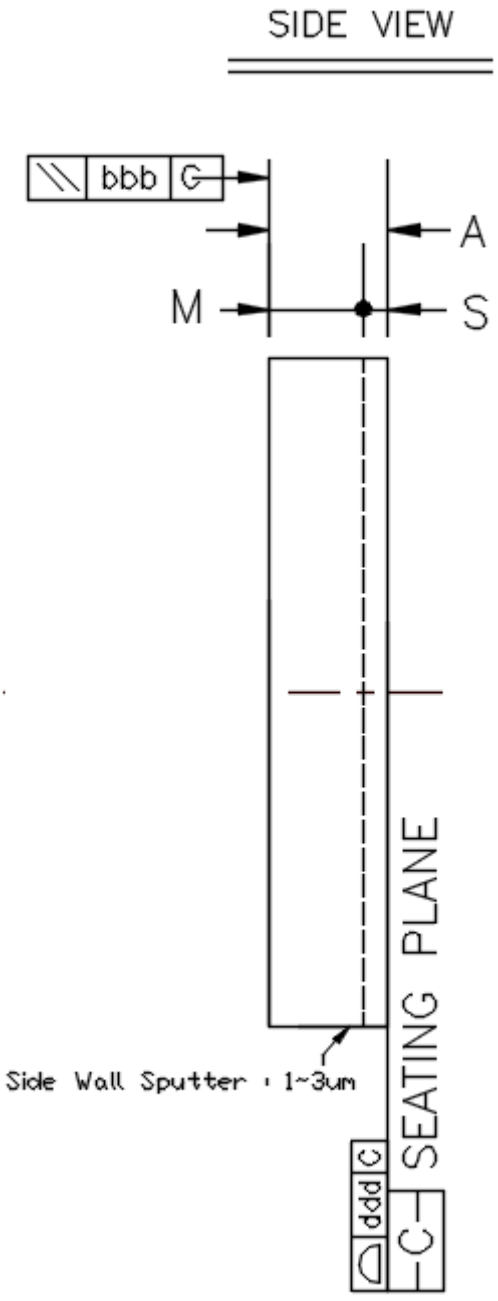


Figure 5: ANNA-B50 physical package – side view

Figure 6 shows a bottom view of the mechanical outline and the critical dimensions of the ANNA-B50 package.

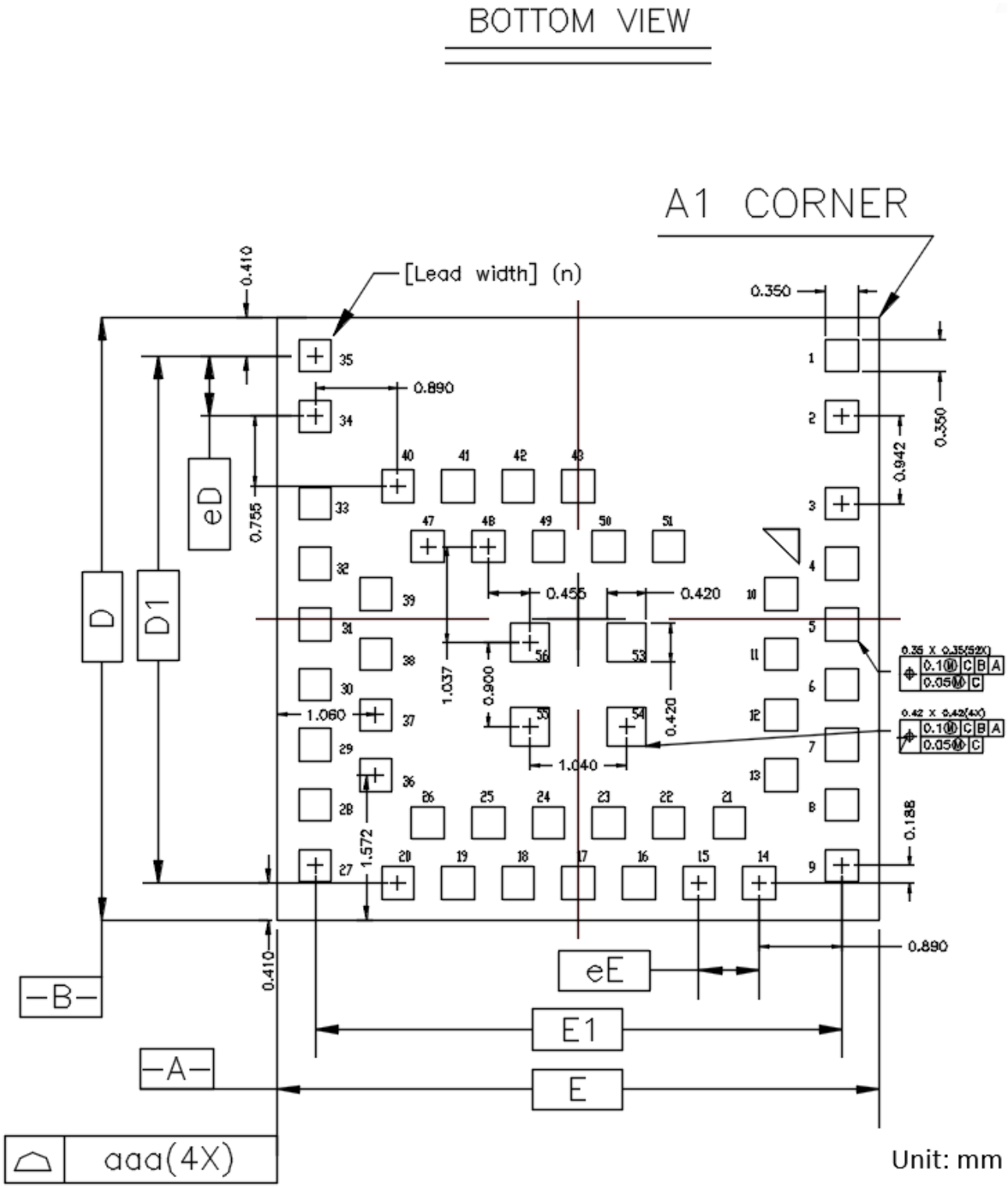


Figure 6: ANNA-B50 physical package outline – bottom view

Figure 7 describes the minimum, nominal, and maximum dimensions together with the symbols for the physical package outline of the ANNA-B50 module.

Description		Symbol	Dimensions(mm)		
			MIN	NOM	MAX
Package :			PIM		
Body Size:	X	E	6.400	6.500	6.600
	Y	D	6.400	6.500	6.600
Lead Pitch :	X	eE		0.650	
	Y	eD		0.650	
Total Thickness :		A		1.150 +/- 0.100	
Mold Thickness :		M		0.910	
Substrate Thickness :		S		0.240	
Lead width:				0.350x0.350 / 0.420x0.420	
Package Edge Tolerance :		aaa		0.100	
Mold Flatness :		bbb		0.100	
Coplanarity:		ddd		0.100	
Lead Count :		n		52	
Edge Lead Center to Center :	X	E1		5.680	
	Y	D1		5.680	

Figure 7: ANNA-B50 physical package - parameters, symbols, and dimensions

6 Qualifications and approvals

⚠ All approvals are currently pending for all ANNA-B50 module variants.

⚠ The development status of ANNA-B50 series modules is described in the document information. Consequently, the information given in this chapter only becomes valid after each module variant has been fully tested and approved during the Initial Production stage.

6.1 Country approvals

ANNA-B50 modules are certified for use in the following countries/regions:

Country/region	ANNA-B501	ANNA-B505
Europe	Pending	Pending
Great Britain (UKCA)	Pending	Pending
USA	Pending	Pending
Canada	Pending	Pending
Japan	Pending	Pending
South Korea	Pending	Pending
Australia	Pending	Pending
New Zealand	Pending	Pending
Taiwan	Pending	Pending

Table 17: Country approvals

☞ For detailed information about the regulatory requirements that must be met for all end-product applications based on ANNA-B50 modules, refer to the system integration manual [1].

6.2 Bluetooth qualification

All products that use Bluetooth technology must be qualified with the Bluetooth Special Interest Group (SIG). This is also applicable for products that are using an already Bluetooth-qualified module.

Product declarations are submitted through the SIG Bluetooth SIG Qualification Workspace

The ANNA-B50 series modules will be qualified as a Core-Controller Configuration against Bluetooth Core 6.0.

To list your product that integrates ANNA-B50 with no additional testing required, combine the DN (Device Number) for the Bluetooth stack implemented in the Core-Host Configuration with the DN of the Core-Controller Configuration shown in Table 18.

Product name	Product type	DN	Product qualification date
ANNA-B501, ANNA-B505	Core-Controller Configuration	TBD	TBD

Table 18: ANNA-B50 series Bluetooth Design Number

7 Product handling

7.1 Packaging

ANNA-B50 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, refer to also the Packaging information reference guide [1].

7.1.1 Reels

Information about the reel types for ANNA-B50 series modules are provided in Table 19. See also the Packaging information reference guide [1].

Model	Reel type	Reel part number	Qty
ANNA-B501	F	MYR-131-BB	500 pcs/reel
ANNA-B505	F	MYR-131-BB	500 pcs/reel

Table 19: Reel types for different models of the ANNA-B50 series

7.1.2 Tapes

Figure 8 shows the position and orientation of the ANNA-B50 series modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 9.

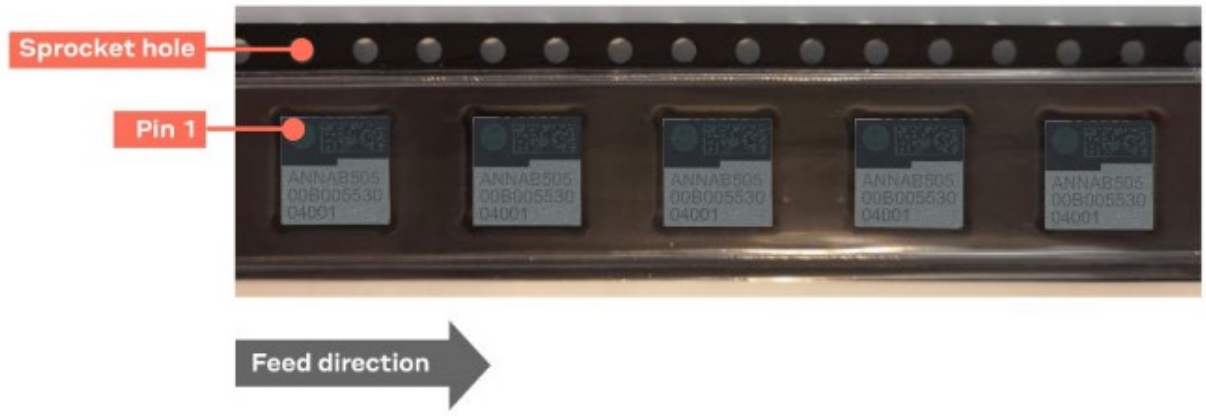
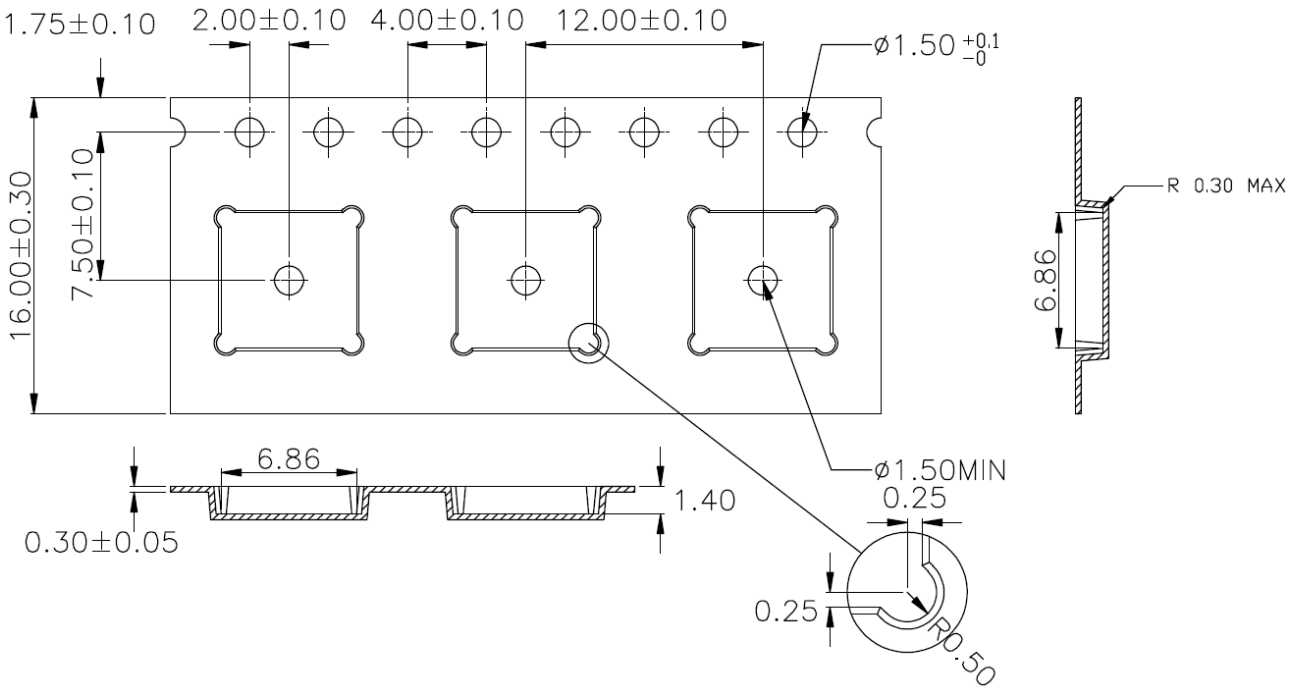


Figure 8: Orientation of ANNA-B50 module on tape



Sprocket hole pitch cumulative tolerance ±0.20.
Carrier camber is within 1mm in 250mm.
Material: Black Conductive Polyester Allow (ABS+PS).
All dimensions meet EIA-481-D requirements.
Thickness: 0.30±0.05 mm.
Surface resistivity: 105~109 Ω/sq.

Figure 9: Orientation of ANNA-B50 module on the tape

7.2 Moisture sensitivity levels

ANNA-B50 series modules are classified as Moisture Sensitive Devices (MSD) in accordance with the IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the required packaging and handling precautions.

⚠ ANNA-B50 series modules are rated at **MSL level 3** in accordance with the IPC/JEDEC J-STD-020 standard. For detailed information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 168 hours in factory conditions of maximum 30 °C/60%RH or must be stored at less than 10%RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033B standard.

For more information regarding moisture sensitivity levels, labeling and storage, see the Packaging information reference guide [1].

☞ For MSL standards, see also IPC/JEDEC J-STD-020 and IPC/JEDED J-STD-033B. The standards can be downloaded from the JEDEC website [7].

7.3 Reflow soldering

Reflow profiles are selected according to u-blox recommendations. See the ANNA-B50 series system integration manual [1] for more information.

⚠ Failure to follow these recommendations can result in severe damage to the device.

7.4 ESD precautions

⚠ ANNA-B50 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the ANNA-B50 series modules without proper ESD protection may destroy or damage them permanently.

ANNA-B50 series modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to the ESD sensitive components. See also Maximum ESD ratings.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the ANNA-B50 series module. Failure to observe these recommendations can result in severe damage to the device.

See also, “Handling and Soldering” in the ANNA-B50 system integration manual [1].

8 Labeling and ordering information

The laser markings on ANNA-B50 series modules include important product information.

8.1 Module marking

Figure 13 shows the laser marking applied to ANNA-B50 series modules. Each of the given laser markings is described in Table 20.

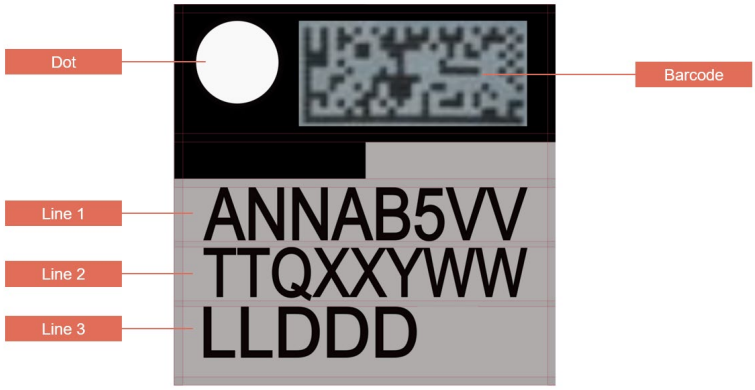


Figure 13: Product marking layout

Item	Description	Example
Dot	Pin 1 corner indication for assembly orientation	-
Line 1	**Product name**	
Pos 1–8	Product name	ANNAB505
Line 2	**Major version, product grade, minor version and production date**	
Pos 1–2	Major product version	00
Pos 3	Product grade	B
Pos 4-5	Minor product version	00
Pos 6	Last digit of production year	5
Pos 7-8	Week number of production date	52
Line 3	**Assembly lot information**	
Pos 1–2	Assembly mother lot, last digits	E1
Pos 3–5	Assembly sub lot number	001

2D barcode		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		Year	Assembly mother lot#						Sub lot#			Strip#		X axis		Y axis	
	Example	8	3	6	U	B	E	1	0	0	1	0	1	0	1	0	1

Table 20: ANNA-B50 laser marking data

8.2 Product identifiers

Table 21 describes the three product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products.	PPPPTGVV (Line1, position 1–8)
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade.	PPPPTGVVTTQ (Line1, position 1-8) (Line 2 position 1–3)
Type number	Comprises the model name and ordering code – with additional identifiers to describe minor product versions.	PPPP -TGVV-TTQ-XX (Line1, position 1–8) (Line 2, position 1–5)

Table 21: Product code formats

8.3 Identification codes

Table 22 explains the parts of the product code.

Code	Meaning	Example
PPPP	Form factor	ANNA

TG	Platform (Technology and Generation)
	• T – Dominant technology, For example,
	  ○ W: Wi-Fi,
	  ○ B: Bluetooth
	G – Generation
		B5: Bluetooth Generation 5

VV	Variant based on the same platform; range [00…99]	05: default mounting, with internal antenna
TT	Major Product Version	00: first revision
Q	Quality grade • A: Automotive • B: Professional • C: Standard	B: professional grade
XX	Minor product version (not relevant for certification)	Default value is 00

Table 22: Part identification code

8.4 Ordering information

Ordering Code	Product
ANNA-B501-00B	ANNA-B5 module with antenna pin, based on nRF54L15, open CPU for custom applications
ANNA-B505-00B	ANNA-B5 module with internal chip antenna, based on nRF54L15, open CPU for custom applications

Table 23: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
AoA	Angle of Arrival
AoD	Angle of Departure
BPF	Band Pass Filter
CBC-MAC	cipher block chaining - message authentication code
CCM	Counter with cipher block chaining - message authentication code
CMAC	Cipher-based Message Authentication Code
CPU	Central Processing Unit
CTI	Cross Trigger Interface
CTR	AES CCM combines counter
CTS	Clear To Send
DC	Direct Current
DMA	Direct Memory Access
DPPI	Distributed Programmable Peripheral Interconnect
DWT	Data Watchpoint and Trace
ECB	Electronic CodeBook
EDM	Extended Data Mode
ESD	ElectroStatic Discharge
ETM	Embedded Trace Macrocell
FCC	Federal Communications Commission (United States)
FEM	Front End Module
FLPR	Fast Lightweight Peripheral Processor
FPU	Floating Point Unit
GATT	Generic ATTribute profile
GCM	Galois/Counter Mode
GPIO	General Purpose Input/Output
I2C/TWI	Inter-Integrated Circuit
ISED	Innovation, Science and Economic Development (Canada)
IEEE	Institute of Electrical and Electronics Engineers
IPC	Inter-Processor Communication
ITM	Instrumentation Trace Macrocell
LE	Low Energy
LNA	Low Noise Amplifier
MUTEX	Mutually Exclusive Peripheral
NC	Not Connected
NFC	Near Field Communication
OEM	Original Equipment Manufacturer
OTP	One-Time Programmable
OUI	Organizationally Unique Identifier
PA	Power Amplifier
PDM	Pulse Density Modulation

Abbreviation	Definition
PWM	Pulse Width Modulation
QDEC	Quadrature DECoder
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RNG	Random Number Generator
GRTC	Global Real-Time Counter
RTLS	Real-Time Location Service
RTS	Request To Send
SDK	Software Development Kit
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
TWI	Two-Wire Interface (See I2C/TWI)
UART	Universal Asynchronous Receiver/Transmitter
UICR	User Information Control Registers
WDT	WatchDog Timer
XIP	eXecute In Place

Table 24: Explanation of the abbreviations and terms used

Related documents

[1] ANNA-B50 system integration manual, UBXDOC-465451970-3933
[2] Packaging information reference guide, UBX-14001652
[3] u-blox openCPU GitHub repository
[4] Nordic Semiconductor nRF54L15_nRF54L10_nRF54L05 Datasheet
[5] Nordic Semiconductor nRF Connect SDK
[6] Channel Sounding at a glance
[7] JEDEC website
[8] RC oscillator configuration for nRF5 open CPU modules Application Note, UBX-20009242

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	15-Sep-2025	yach, habd	Initial release
R02	1-Apr-2026	mape, habd	Updated module status in Document information. Updated product description Table 2. Added VCCPOR to power pins Table 11. Updated current consumption Table 12, RF performance Table 13, and Antenna radiation patterns. Minor updates and documentation improvements throughout the document.

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