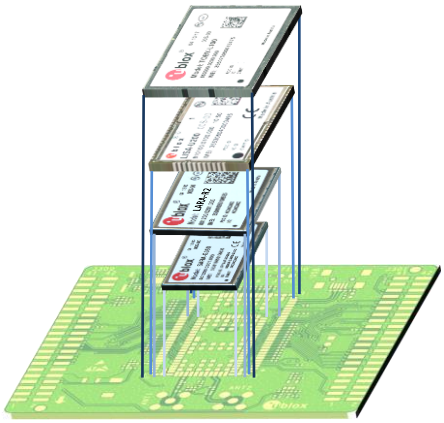
Nested design

Reference design for TOBY / LISA / SARA / LARA modules

Application note



Abstract

This document describes the nested design for the TOBY, LISA, SARA, and LARA cellular modules, in which modules of these different form factors may alternatively be mounted on the same PCB. This reference design is intended to be used as a template to assist in making application-specific products. Reference designs, including example schematics, bill of materials, layout and routing suggestions, are available to u-blox customers.

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This document applies to the following products:

Product name
TOBY-L1 series
TOBY-L2 series
TOBY-R2 series
LISA-U2 series
SARA-G3 series
SARA-G4 series
SARA-U2 series
SARA-N3 series
SARA-R4 series
SARA-R5 series
LARA-R2 series
LARA-R6 series

Contents

1 Introduction

u-blox uses the term “nested design” to describe application boards on which modules of different form factors can be mounted in the same space. This document provides HW guidelines for mounting TOBY, LISA, SARA, or LARA form factor modules on the same space of a “nested” application board and describes the u-blox reference design as a “nested” printed circuit board design for the TOBY, LISA, SARA, and LARA cellular modules.

Detailed firmware topics are not covered in this document, but TOBY, LISA, SARA, and LARA modules share most of the AT commands (for all the complete description details and differences, see the AT commands manual for the LARA-R2, LISA-U2, SARA-G3, SARA-G4, SARA-U2, TOBY-L2, and TOBY-R2 series modules [26], for TOBY-L1 series modules [24], for SARA-R41 and SARA-R42 series modules [25], for SARA-N2 and SARA-N3 series modules [27], for SARA-R5 series modules [28] or for LARA-R6 series modules [29]).

In this document, unless otherwise noted:

- TOBY refers to TOBY-L1 series, TOBY-L2 series, and TOBY-R2 series cellular modules
- LISA refers to LISA-U2 series cellular modules
- SARA refers to SARA-G3 series, SARA-G4 series, SARA-U2 series, SARA-N3 series, SARA-R41 series, SARA-R42 series, and SARA-R5 series cellular modules
- LARA refers to LARA-R2 and LARA-R6 series cellular modules

This application note explains the points to consider when developing a nested application board for TOBY, LISA, SARA, or LARA modules, focusing particularly on the following series of modules:

- TOBY-L1, TOBY-L2, and TOBY-R2 series modules,
- LISA-U2 series modules,
- SARA-U2, SARA-G3, and SARA-R41 series modules,
- LARA-R2 and LARA-R6 series modules.

Further guidelines to migrate between all the different SARA modules product versions, including the SARA-G3, SARA-G4, SARA-U2, SARA-N2, SARA-N3, SARA-R41, SARA-R42, and SARA-R5 series modules, are available in the SARA modules migration guidelines application note [30].

Further guidelines to migrate between all the different LARA modules product versions are available in the LARA modules migration guidelines application note [31].

For further details regarding the characteristics, usage, or settings of each product version of TOBY, LISA, SARA, and LARA modules, see:

- The specific data sheet of the related series of u-blox cellular modules: TOBY-L1 [1], TOBY-L2 [2], TOBY-R2 [3], LISA-U2 [4], SARA-G3 [5], SARA-G4 [6], SARA-U2 [7], SARA-N3 [8], LARA-R2 [9], LARA-R6 [10], SARA-R4 [11], SARA-R5 [12]
- The specific system integration manual for related series of u-blox cellular modules: TOBY-L1 [13], TOBY-L2 [14], TOBY-R2 [15], LISA-U2 [16], SARA-N2 / SARA-N3 [17], SARA-G4 [18], SARA-G3 / SARA-U2 [19], LARA-R2 [20], LARA-R6 [21], SARA-R41 / SARA-R42 [21], SARA-R5 [23]
- The specific AT commands manual for the related series of u-blox cellular modules: TOBY-L1 [24], TOBY-L2 / TOBY-R2 / LISA-U2 / SARA-G3 / SARA-G4 / SARA-U2 / LARA-R2 [26], SARA-R41 / SARA-R42 [25], SARA-N2 / SARA-N3 [27], SARA-R5 [28], LARA-R6 [29]
- the modules’ pins comparisons in Table 2

2 Nested design description

2.1 Nested design concept

Migrating between TOBY, LISA, SARA, and LARA module designs is a straightforward procedure that allows customers to take maximum advantage of their hardware and software investments.

u-blox adheres to a core “nested design” philosophy. Although the TOBY modules (35.6 x 24.8 mm, 152-pin LGA), the LISA modules (33.2 x 22.4 mm, 76-pin LCC), the SARA modules (26.0 x 16.0 mm, 96-pin LGA), and the LARA modules (26.0 x 24.0 mm, 100-pin LGA) each have different form factors, the footprints for the TOBY, LISA, SARA, and LARA modules have been developed to ensure layout compatibility. This is preferred to pin compatibility, which requires every module to share the largest, most expensive package.

With the “nested design” solution, any TOBY, LISA, SARA, or LARA module can be alternatively mounted on the same nested PCB as shown in Figure 1.

In particular, the eleven pins of the modules along the side where the RF pins for cellular antenna(s) are located (the white pins on the lower edges in Figure 1) share the same eleven pads on the PCB. These pins have the same pitch and nearly the same functions due to layout compatibility.

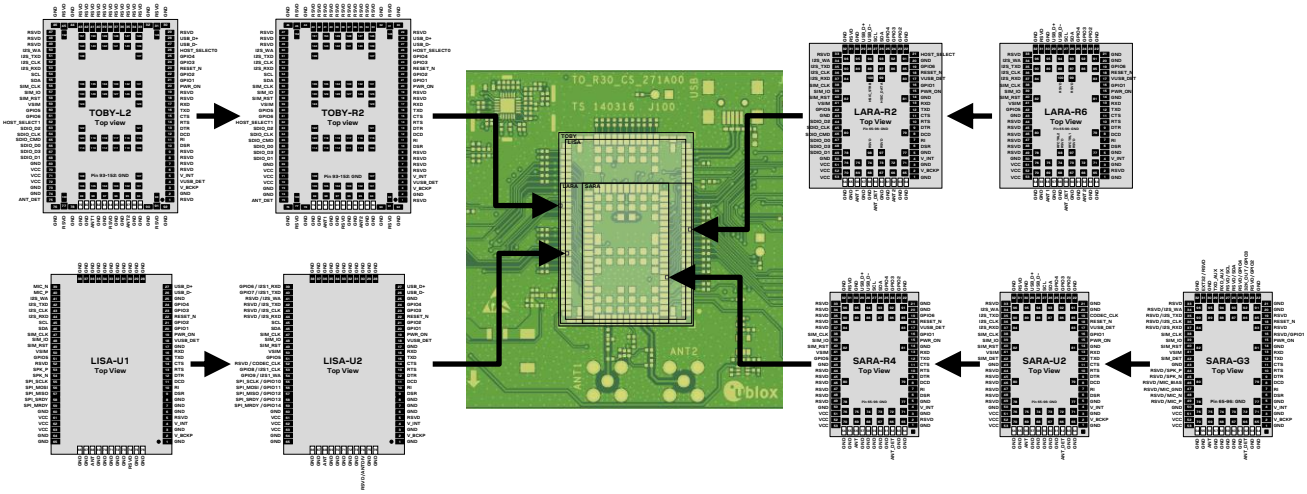

Figure 1: TOBY, LISA, SARA, LARA modules’ layout compatibility: all modules can be mounted on the same nested footprint

Four different soldering paste masks are implemented in the nested design, one each for the four different form factors according to the selected mounting option (TOBY, LISA, SARA, or LARA), as shown in Figure 2.

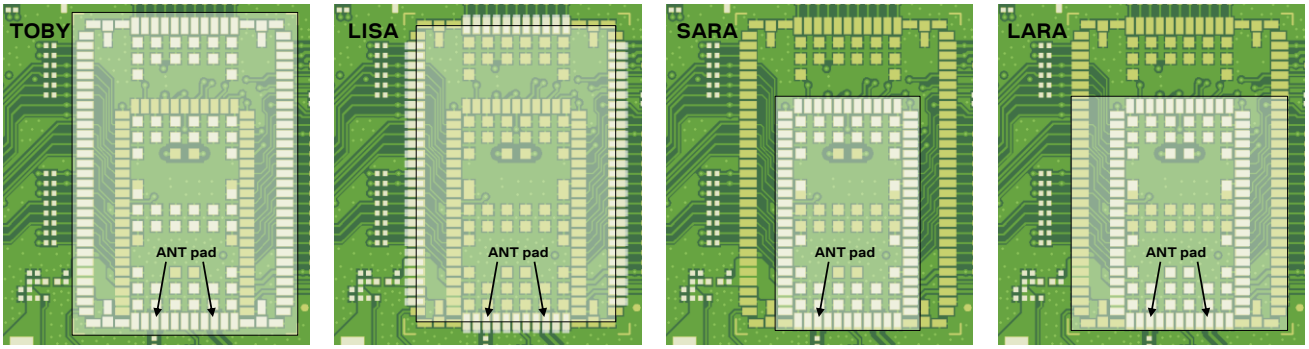

Figure 2: Nested design concept description: TOBY, SARA, and LARA modules alternatively mounted on the same PCB

As illustrated in Figure 1 and Figure 2, the LISA and TOBY modules have a very similar footprint, and the SARA and LARA modules have almost the same footprint.

In details, the LISA modules (33.2 x 22.4 mm, 76-pin LCC) are designed to share the same 76 pads on the host nested application PCB that are available to accommodate 76 “lateral” pads of the TOBY modules (35.6 x 24.8 mm, 152-pin LGA): these 76 pads on the host PCB are along the edge of the LISA LCC modules, and they are below the TOBY LGA modules, so that LISA modules can perfectly fit on the footprint designed for TOBY modules. Additional “central” GND pads are available on the TOBY LGA modules, differently from LISA LCC modules, but this does not prevent at all the possibility to mount LISA modules on the footprint designed for TOBY modules.

Following a roughly similar concept, the SARA modules (26.0 x 16.0 mm, 96-pin LGA) are designed to share the same 96 pads on the host nested application PCB that are available to accommodate the “lateral” and most of the “central” pads of the larger LARA modules (26.0 x 24.0 mm, 100-pin LGA). Four more “central” pads are available on LARA modules as compared with SARA modules, and these pads can be left open if their function is not intended to be used in the end-device application, as for example the additional antenna dynamic tuner function available with LARA-R6401 / LARA-R6401D modules that can be optionally implemented in the end-device application but not necessarily.

While the RF pin(s) of all the TOBY, LISA, SARA, and LARA modules share the same pads on the top layer of the nested application board, as well as all the eleven pins of the modules along the side where the RF pins are located (the white pins on the lower edges in Figure 1), roughly the same concept is applicable also to all the main interfaces due to the layout compatibility between TOBY / LISA and SARA / LARA, for example:

- The three **VCC** pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the three **VCC** pins of SARA and LARA modules to facilitate routing (see section 3.1.1, Figure 4)
- SIM pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the SIM pins of SARA and LARA (see section 3.4, Figure 17)
- UART pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the UART pins of SARA and LARA (see section 3.5.1, Figure 18)
- USB pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the USB pins of SARA and LARA (see section 3.5.3, Figure 21)
- I2S pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the I2S pins of SARA and LARA (see section 3.6.2.1, Figure 23)

This concept can be extended to all the interfaces shared between the modules, as described in section 3, allowing fast and easy development of the application circuit for all the modules.

2.2 Nested design bill of materials variants

The printed circuit board of the nested reference design for mounting TOBY, LISA, SARA, or LARA modules is identified by the "TO_R30_CS_271A00" code (shown on the top side of the board).

Table 1 lists the different bill of materials (BOM) variants, also referred to as hardware release (HR) variants, available as mounting options on the same nested PCB[1], so that any TOBY-L1, TOBY-L2, TOBY-R2, LISA-U2, SARA-G3, SARA-U2, SARA-R41, LARA-R2 or LARA-R6 module can be alternatively mounted on the same nested board with all the suitable components provided in the mounting options.

Table 1 also lists the four top-side paste masks implemented in the nested design for the four form factors (TOBY, LISA, SARA, and LARA) described in Figure 2.

Further guidelines to migrate between any of the u-blox SARA modules product versions are available in the specific SARA modules migration guidelines application note [30]. Among the SARA modules, the SARA-G4, SARA-N2, SARA-N3, SARA-R42, and SARA-R5 series modules can be alternatively mounted on a the same nested footprint implemented on the host PCB; the SARA-G3, SARA-U2, and SARA-R41 series modules listed in Table 1 are specifically considered in this application note with related design files package.

Further guidelines to migrate between any of the u-blox LARA modules product versions are available in the LARA modules migration guidelines application note [31].

☞ Only one schematic (the TO_R30_HS_271A00.pdf file) is provided, including all the necessary comments explaining the different BoM mounting options for the different hardware release variants of the nested design.

Variant ID	HW release ID	BoM file	Top-side paste mask file	Schematic file	Modules
A	HR_271A**A**0	TO_R30_BM_271A**A**0	07_PASTE_TOP_**LARA**	TO_R30_HS_271A00	**LARA-R2 series**
B	HR_271A**B**0	TO_R30_BM_271A**B**0	07_PASTE_TOP_**TOBY**	TO_R30_HS_271A00	**TOBY-L2 series**
C	HR_271A**C**0	TO_R30_BM_271A**C**0	07_PASTE_TOP_**TOBY**	TO_R30_HS_271A00	**TOBY-R2 series**
D	HR_271A**D**0	TO_R30_BM_271A**D**0	07_PASTE_TOP_**TOBY**	TO_R30_HS_271A00	**TOBY-L1 series**
E	HR_271A**E**0	TO_R30_BM_271A**E**0	07_PASTE_TOP_**SARA**	TO_R30_HS_271A00	**SARA-U2 series**
F	HR_271A**F**0	TO_R30_BM_271A**F**0	07_PASTE_TOP_**SARA**	TO_R30_HS_271A00	**SARA-G3 series**
G	HR_271A**G**0	TO_R30_BM_271A**G**0	07_PASTE_TOP_**LISA**	TO_R30_HS_271A00	**LISA-U2 series**
H	HR_271A**H**0	TO_R30_BM_271A**H**0	07_PASTE_TOP_**SARA**	TO_R30_HS_271A00	**SARA-R41 series**
J	HR_271A**J**0	TO_R30_BM_271A**J**0	07_PASTE_TOP_**LARA**	TO_R30_HS_271A00	**LARA-R6 series**

Table 1: Nested design hardware releases (HR) / bill of materials (BoM) variants description

[1] The Nested Design Reference Design can be mounted on the EVB-WL1 or the EVB-WL3 Evaluation Boards as Adapter for cellular modules. The voltage rail of the modules' generic digital interfaces can be set to 1.8 V or 2.85 V on the EVB-WL1 board. The TOBY/LISA/SARA/LARA Nested Design sets this voltage to 1.8 V by tying to GND pin 41 of J301 and pin 42 of J303 as described in the schematic diagram TO_R30_CS_271A00, because the V_INT voltage level of the generic digital interfaces of all TOBY, LISA, SARA, and LARA modules is 1.8 V.

2.3 Module pin-out comparison

Table 2 summarizes the electrical differences of pins on TOBY, LISA, SARA, and LARA cellular modules.

Pin name	N	TOBY-L2	N	TOBY-R2	N	LISA-U2	N	SARA-G3 [2]	N	SARA-U2	N	SARA-R41	N	LARA-R2	N	LARA-R6
Power																
VCC	70 71 72	Normal operat. Range: 3.4 V … 4.35 V Extended operat. Range: 3.2 V … 4.35 V TOBY-L200/L210/L280: Large pulse current in 2G GSM TDMA call mode	70 71 72	Normal operat. Range: 3.3 V … 4.4 V Extended operat. Range: 3.0 V … 4.5 V TOBY-R200: Large pulse current in 2G GSM TDMA call mode	61 62 63	Normal operat. Range: 3.3 V … 4.4 V Extended operat. Range: 3.1 V … 4.5 V Large pulse current in 2G GSM TDMA call mode	51 52 53	Normal operat. Range: 3.35 V … 4.5 V Extended operat. Range: 3.00 V … 4.5 V Large pulse current in 2G GSM TDMA call mode	51 52 53	Normal operat. Range: 3.3 V … 4.4 V Extended operat. Range: 3.1 V … 4.5 V SARA-U201/260/270: Large pulse current in 2G GSM TDMA call mode	51 52 53	Normal operat. Range: 3.2 V … 4.2V Extended operat. Range: 3.0 V … 4.3 V SARA-R412M: Large pulse current in 2G GSM TDMA call mode	51 52 53	Normal operat. Range: 3.3 V … 4.4 V Extended operat. Range: 3.0 V … 4.5 V LARA-R211: Large pulse current in 2G GSM TDMA call mode	51 52 53	Normal operat. Range: 3.3 V … 4.5 V Extended operat. Range: 3.1 V … 4.5 V LARA-R6001/R6801: Large pulse current in 2G GSM TDMA call mode
V_BCKP	3	Output characteristics: 3.0 V typ, 3 mA max Input operating range: 1.4 V … 4.2 V	3	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V	2	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V	2	Output characteristics: 1.8 V typ, 2 mA max Input operating range: 1.0 V … 2.4 V	2	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V		Not Available	2	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V	2	Not available
V_INT	5	Output characteristics: 1.8 V typ, 70 mA max	5	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max
Antenna																
ANT1 / ANT	81	RF input/output for Tx/Rx antenna	81	RF input/output for Tx/Rx antenna	68	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna
ANT2 / ANT_DIV	87	RF input for LTE Rx MIMO 2x2 3G Rx diversity	87	RF input for LTE Rx diversity 3G Rx diversity	74	LISA-U230 only: RF input for 3G Rx diversity		Not Available		Not Available		Not Available	62	RF input for LTE Rx diversity 3G Rx diversity	62	RF input for LTE Rx diversity 3G Rx diversity
ANT_DET	75	Input for antennas detection circuit[3]	75	Input for antennas detection circuit		Not available: Internal antenna detection circuit	62	SARA-G340 / G350: Input for antenna detection circuit	62	Input for antenna detection circuit	62	Input for antenna detection circuit	59	Input for antenna detection circuit	59	Input for antenna detection circuit
System																
PWR_ON	20	Internal pull-up: 50kΩ to VCC Low: 0.0 … 0.3 x VCC Low pulse to switch-on: 5 ms min Low pulse to switch-off: Not supported	20	Internal pull-up: 10kΩ to V_BCKP Low: –0.30 V … 0.54 V Low pulse to switch-on: 50 µs min Low pulse to switch-off: 1 s min	19	Internal pull-up: Not present Low: –0.30 V … 0.65 V Low pulse to switch-on: 50 µs min / 80 µs max Low pulse to switch-off: 1 s min	15	Internal pull-up: Not present Low: –0.10 V … 0.65 V Low pulse to switch-on: 5 ms min Low pulse to switch-off: Not supported	15	Internal pull-up: Not present Low: –0.30 V … 0.65 V Low pulse to switch-on: 50 µs min / 80 µs max Low pulse to switch-off: 1 s min	15	Internal pull-up: 200kΩ to 1.8V Low: –0.30 V … 0.35 V Low pulse to switch-on: 0.15 s min / 3.2 s max Low pulse to switch-off: 1.50 s min	15	Internal pull-up: 10kΩ to V_BCKP Low: –0.30 V … 0.54 V Low pulse for switch-on: 50 µs min Low pulse to switch-off: 1 s min	15	Internal pull-up: 200kΩ to 1.8V Low: –0.30 V … 0.35 V Low pulse to switch-on: 0.15 s min / 3.2 s max Low pulse to switch-off: 1.5 s min

[2] Antenna detection (ANT_DET), I2C, analog audio (MIC, SPK), digital audio (I2S) and GPIOs are not supported by SARA-G300 / SARA-G310: the related pins are reserved for future use (RSVD).
[3] Not supported by “00”, “01”, “60” product versions

Pin name	N	TOBY-L2	N	TOBY-R2	N	LISA-U2	N	SARA-G3 [2]	N	SARA-U2	N	SARA-R41	N	LARA-R2	N	LARA-R6
RESET_N	23	Internal pull-up: 50kΩ to VCC Low: 0.0 … 0.3 x VCC Low pulse to switch-on: 18 ms min / 0.8 s max Low pulse to reset: 2.1 s min / 15 s max Low pulse to switch-off: 16 s min	23	Internal pull-up: 10kΩ to V_BCKP Low: –0.30 V … 0.54 V Low pulse to switch-on: 50 ms min Low pulse to reset: 50 ms min Low pulse to switch-off: Not supported	22	Internal pull-up: 10kΩ to V_BCKP Low: –0.30 V … 0.51 V Low pulse to switch-on: 50 ms min Low pulse to reset: 50 ms min Low pulse to switch-off: Not supported	18	Internal pull-up: diode & 10kΩ to V_INT Low: –0.30 V … 0.30 V Low pulse to switch-on: Not supported Low pulse to reset: 50 ms min Low pulse to switch-off: Not supported	18	Internal pull-up: 10kΩ to V_BCKP Low: –0.30 V … 0.51 V Low pulse to switch-on: 50 ms min Low pulse to reset: 50 ms min Low pulse to switch-off: Not supported	18	Internal pull-up: 37kΩ to 1.8V Low: –0.30 V … 0.63 V Low pulse to switch-on: Not supported Low pulse to reset: Not supported Low pulse to switch-off: 10 s min	18	Internal pull-up: 10kΩ to V_BCKP Low: –0.30 V … 0.54 V Low pulse to switch-on: 50 ms min Low pulse to reset: 50 ms min Low pulse to switch-off: Not supported	18	Internal pull-up: 10kΩ to 1.8V Low: –0.30 V … 0.63 V Low pulse to switch-on: Not supported Low pulse to reset: 50 ms min / 6 s max Low pulse to switch-off: 10 s min
EXT32K		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode	31	SARA-G300 / G310: 32 kHz input for RTC & low power idle mode SARA-G340 / G350: Not available due to internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power mode		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode
32K_OUT		Not Available		Not Available		Not Available	24	SARA-G300 / G310: 32 kHz output, only to feed the EXT32K input SARA-G340 / G350: Not Available		Not Available		Not Available		Not Available		Not Available
HOST_SELECT0	26	1.8 V input to select module setting by host[4]	26	1.8 V input to select module setting by host[4]		Not Available		Not Available Pin 21 is connected to GND internally, it may be left open externally		Not Available Pin 21 is connected to GND internally, it may be left open externally		Not Available Pin 21 is connected to GND internally, it may be left open externally	21	1.8 V input to select module setting by host[4]		Not available Pin 21 is connected to GND internally, it may be left open externally
HOST_SELECT1	62	1.8 V input to select module setting by host[4]	62	1.8 V input to select module setting by host[4]		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available
SIM																
SIM_CLK	56	1.8 V / 3.0 V SIM clock	56	1.8 V / 3.0 V SIM clock	47	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock
SIM_IO	57	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	57	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	48	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up
SIM_RST	58	1.8 V / 3.0 V SIM reset	58	1.8 V / 3.0 V SIM reset	49	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset
VSIM	59	1.8 V / 3.0 V SIM supply	59	1.8 V / 3.0 V SIM supply	50	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply
SIM_DET	60	Provided by GPIO5[5]: 1.8 V, SIM detect input	60	Provided by GPIO5: 1.8 V, SIM detect input	51	Provided by GPIO5: 1.8 V, SIM detect input	42	1.8 V, SIM detect input	42	1.8 V, SIM detect input	42	Provided by GPIO5: 1.8 V, SIM detect input	42	Provided by GPIO5: 1.8 V, SIM detect input	42	Provided by GPIO5: 1.8 V, SIM detect input

[4] Not supported
[5] Not supported by “00”, “01”, “60” product versions

Pin name	N	TOBY-L2	N	TOBY-R2	N	LISA-U2	N	SARA-G3 [2]	N	SARA-U2	N	SARA-R41	N	LARA-R2	N	LARA-R6
UART																
DSR	10	1.8 V, DSR out[6] / GPIO[7] Driver strength: 2 mA	10	1.8 V, DSR output Driver strength: 6 mA	9	1.8 V, DSR output Driver strength: 1 mA	6	1.8 V, DSR output Driver strength: 6 mA	6	1.8 V, DSR output Driver strength: 1 mA	6	1.8 V, DSR output Driver strength: 2 mA	6	1.8 V, DSR output Driver strength: 6 mA	6	1.8 V, DSR output Driver strength: 6 mA
RI	11	1.8 V, RI output[6] / GPIO[7] Driver strength: 2 mA	11	1.8 V, RI output Driver strength: 6 mA	10	1.8 V, RI output Driver strength: 2 mA	7	1.8 V, RI output Driver strength: 6 mA	7	1.8 V, RI output Driver strength: 2 mA	7	1.8 V, RI output Driver strength: 2 mA A	7	1.8 V, RI output Driver strength: 6 mA	7	1.8 V, RI output Driver strength: 6 mA
DCD	12	1.8 V, DCD out[6] / GPIO[7] Driver strength: 2 mA	12	1.8 V, DCD output Driver strength: 6 mA	11	1.8 V, DCD output Driver strength: 2 mA	8	1.8 V, DCD output Driver strength: 6 mA	8	1.8 V, DCD output Driver strength: 2 mA	8	1.8 V, DCD output Driver strength: 2 mA	8	1.8 V, DCD output Driver strength: 6 mA	8	1.8 V, DCD output Driver strength: 6 mA
DTR	13	1.8 V, DTR in[6] / GPIO[7] Internal pull-up: ~80 kΩ	13	1.8 V, DTR input Internal pull-up: ~7.5 kΩ	12	1.8 V, DTR input Internal pull-up: ~14 kΩ	9	1.8 V, DTR input Internal pull-up: ~33 kΩ	9	1.8 V, DTR input Internal pull-up: ~14 kΩ	9	1.8 V, DTR input Internal pull-up: ~100kΩ	9	1.8 V, DTR input Internal pull-up: ~7.5 kΩ	9	1.8 V, DTR input Internal pull-up: ~100kΩ
RTS	14	1.8 V, Flow ctrl input[6] Internal pull-up: ~80 kΩ	14	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ	13	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ	10	1.8 V, Flow control input Internal pull-up: ~58 kΩ	10	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ	10	1.8 V, Flow control input Internal pull-up: ~100kΩ	10	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ	10	1.8 V, Flow control input Internal pull-up: ~100kΩ
CTS	15	1.8 V, Flow ctrl output[6] Driver strength: 2 mA	15	1.8 V, Flow ctrl output Driver strength: 6 mA	14	1.8 V, Flow ctrl output Driver strength: 6 mA	11	1.8 V, Flow ctrl output Driver strength: 6 mA	11	1.8 V, Flow ctrl output Driver strength: 6 mA	11	1.8 V, Flow ctrl output Driver strength: 2 mA	11	1.8 V, Flow ctrl output Driver strength: 6 mA	11	1.8 V, Flow ctrl output Driver strength: 6 mA
TXD	16	1.8 V, Data input[6] Internal pull-up: ~80 kΩ	16	1.8 V, Data input Internal pull-up: ~7.5 kΩ	15	1.8 V, Data input Internal pull-up: ~7.5 kΩ	12	1.8 V, Data input Internal pull-up: ~18 kΩ	12	1.8 V, Data input Internal pull-up: ~7.5 kΩ	12	1.8 V, Data input Internal pull-up: ~100kΩ	12	1.8 V, Data input Internal pull-up: ~7.5 kΩ	12	1.8 V, Data input Internal pull-up: ~100kΩ
RXD	17	1.8 V, Data output[6] Driver strength: 2 mA	17	1.8 V, Data output Driver strength: 6 mA	16	1.8 V, Data output Driver strength: 6 mA	13	1.8 V, Data output Driver strength: 5 mA	13	1.8 V, Data output Driver strength: 6 mA	13	1.8 V, Data output Driver strength: 2 mA	13	1.8 V, Data output Driver strength: 6 mA	13	1.8 V, Data output Driver strength: 6 mA
UART AUX																
TXD_AUX		Not Available		Not Available		Not Available	29	1.8 V, Data input Internal pull-up: ~18 kΩ	26	SARA-U201-04: AUX UART data input configurable on SDA pin Internal pull-up: ~7.5 kΩ		Not Available	26	LARA-R211 and '03B': AUX UART data input configurable on SDA pin Internal pull-up: ~7.5 kΩ	9	AUX UART data input configurable on DTR pin Internal pull-up: ~100kΩ
RXD_AUX		Not Available		Not Available		Not Available	28	1.8 V, Data output Driver strength: 5 mA	27	SARA-U201-04: AUX UART data output configurable on SCL pin Driver strength: 0.1 mA		Not Available	27	LARA-R211 and '03B': AUX UART data output configurable on SCL pin Driver strength: 6 mA	8	AUX UART data output configurable on DCD pin Driver strength: 6 mA
RTS_AUX		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available	6	AUX UART flow ctrl input configurable on DSR pin Internal pull-up: ~100 kΩ
CTS_AUX		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available	7	AUX UART flow ctrl output configurable on RI pin Driver strength: 6 mA
USB																
VUSB_DET	4	Leave unconnected Functionality of the pin is not supported by FW	4	Input for VBUS USB supply detection 1.5 V … 5.25 V	18	Input for VBUS USB supply detection 4.4 V … 5.25 V		Not Available	17	Input for VBUS USB supply detection 4.4 V … 5.25 V	17	Input for VBUS USB supply detection 4.4 V … 5.25 V at boot	17	Input for VBUS USB supply detection 1.5 V … 5.25 V	17	Input for VBUS USB supply detection 1.5 V … 5.25 V at boot
USB_D-	27	High-Speed USB 2.0	27	High-Speed USB 2.0	26	High-Speed USB 2.0		Not Available	28	High-Speed USB 2.0	28	High-Speed USB 2.0	28	High-Speed USB 2.0	28	High-Speed USB 2.0
USB_D+	28	High-Speed USB 2.0	28	High-Speed USB 2.0	27	High-Speed USB 2.0		Not Available	29	High-Speed USB 2.0	29	High-Speed USB 2.0	29	High-Speed USB 2.0	29	High-Speed USB 2.0

[6] Not supported by “00” product versions
[7] Not supported by “00”, “01”, “60” product versions

Pin name	N	TOBY-L2	N	TOBY-R2	N	LISA-U2	N	SARA-G3 [2]	N	SARA-U2	N	SARA-R41	N	LARA-R2	N	LARA-R6
HSIC																
HSIC_DATA		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available	99	1.2V, HSIC USB data[8]		Not available (pin 99 is RSVD)
HSIC_STRB		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available	100	1.2V, HSIC USB strobe[8]		Not available (pin 100 is RSVD)
I2C																
SCL	54	1.8 V, open drain[9] No internal pull-up Driver strength: 1 mA	54	1.8 V, open drain No internal pull-up Driver strength: 1 mA	45	1.8 V, open drain No internal pull-up Driver strength: 1 mA	27	1.8 V, open drain No internal pull-up Driver strength: 3 mA	27	1.8 V, open drain No internal pull-up Driver strength: 1 mA	27	1.8 V, open drain[10] Internal pull-up: 2.2kΩ Driver strength: 2 mA	27	1.8 V, open drain No internal pull-up Driver strength: 1 mA	27	1.8 V, open drain Internal pull-up: 2.2kΩ Driver strength: 2 mA
SDA	55	1.8 V, open drain[9] No internal pull-up Driver strength: 1 mA	55	1.8 V, open drain No internal pull-up Driver strength: 1 mA	46	1.8 V, open drain No internal pull-up Driver strength: 1 mA	26	1.8 V, open drain No internal pull-up Driver strength: 3 mA	26	1.8 V, open drain No internal pull-up Driver strength: 1 mA	26	1.8 V, open drain[10] Internal pull-up: 2.2kΩ Driver strength: 2 mA	26	1.8 V, open drain No internal pull-up Driver strength: 1 mA	26	1.8 V, open drain Internal pull-up: 2.2kΩ Driver strength: 2 mA
SPI																
SPI_SCLK		Not Available (Pin 64 is for SDIO)		Not Available (Pin 64 is for SDIO/RSVD)	55	1.8 V, SPI clock in / GPIO		Not Available		Not Available	36	Not supported		Not Available		Not Available
SPI_MOSI		Not Available (Pin 65 is for SDIO)		Not Available (Pin 65 is for SDIO/RSVD)	56	1.8 V, SPI data in / GPIO		Not Available		Not Available	34	Not supported		Not Available		Not Available
SPI_MISO		Not Available (Pin 66 is for SDIO)		Not Available (Pin 66 is for SDIO/RSVD)	57	1.8 V, SPI data out/GPIO		Not Available		Not Available	37	Not supported		Not Available		Not Available
SPI_SRDY		Not Available (Pin 67 is for SDIO)		Not Available (Pin 67 is for SDIO/RSVD)	58	1.8 V, SPI ctrl out / GPIO		Not Available		Not Available		Not Available		Not Available		Not Available
SPI_MRDY		Not Available (Pin 68 is for SDIO)		Not Available (Pin 68 is for SDIO/RSVD)	59	1.8 V, SPI ctrl in / GPIO		Not Available		Not Available		Not Available		Not Available		Not Available
SDIO																
SDIO_D2	63	1.8 V, SDIO data [2][11] Driver strength: 2 mA	63	1.8 V, SDIO data [2][8] Driver strength: 6 mA		Not Available (Pin 54 is for I2S1/GPIO)		Not Available (Pin 44 is for analog audio)		Not Available (Pin 44 is RSVD)	44	Reserved for future use	44	1.8 V, SDIO data [2][8] Driver strength: 6 mA	44	Reserved for future use
SDIO_CLK	64	1.8 V, SDIO clock out[11] Driver strength: 2 mA	64	1.8 V, SDIO clock out[8] Driver strength: 6 mA		Not Available (Pin 55 is for SPI/GPIO)		Not Available (Pin 45 is for analog audio)		Not Available (Pin 45 is RSVD)	45	Reserved for future use	45	1.8 V, SDIO clock out[8] Driver strength: 6 mA	45	Reserved for future use
SDIO_CMD	65	1.8 V, SDIO command[11] Driver strength: 2 mA	65	1.8 V, SDIO command[8] Driver strength: 6 mA		Not Available (Pin 56 is for SPI/GPIO)		Not Available (Pin 46 is for analog audio)		Not Available (Pin 46 is RSVD)	46	Reserved for future use	46	1.8 V, SDIO command[8] Driver strength: 6 mA	46	Reserved for future use
SDIO_D0	66	1.8 V, SDIO data [0][11] Driver strength: 2 mA	66	1.8 V, SDIO data [0][8] Driver strength: 6 mA		Not Available (Pin 57 is for SPI/GPIO)		Not Available (Pin 47 is for analog audio)		Not Available (Pin 47 is RSVD)	47	Reserved for future use	47	1.8 V, SDIO data [0][8] Driver strength: 6 mA	47	Reserved for future use
SDIO_D3	67	1.8 V, SDIO data [3][11] Driver strength: 2 mA	67	1.8 V, SDIO data [3][8] Driver strength: 6 mA		Not Available (Pin 58 is for SPI/GPIO)		Not Available (Pin 48 is for analog audio)		Not Available (Pin 48 is RSVD)	48	Reserved for future use	48	1.8 V, SDIO data [3][8] Driver strength: 6 mA	48	Reserved for future use
SDIO_D1	68	1.8 V, SDIO data [1][11] Driver strength: 2 mA	68	1.8 V, SDIO data [1][8] Driver strength: 6 mA		Not Available (Pin 59 is for SPI/GPIO)		Not Available (Pin 49 is for analog audio)		Not Available (Pin 49 is RSVD)	49	Reserved for future use	49	1.8 V, SDIO data [1][8] Driver strength: 6 mA	49	Reserved for future use

[8] Not supported
[9] Not supported by “00”, “01”, “60” and TOBY-L201-02S product versions
[10] Not supported by “00”, “01” product versions
[11] Not supported by “00”, “01”, “60” product versions

Pin name	N	TOBY-L2	N	TOBY-R2	N	LISA-U2	N	SARA-G3 [2]	N	SARA-U2	N	SARA-R41	N	LARA-R2	N	LARA-R6
Audio																
Analog audio																
MIC_BIAS		Not Available		Not Available		Not Available	46	2.2 V supply out for mic.		Not Available (Pin 46 is RSVD)		Not Available (Pin 46 is SDIO/RSVD)		Not Available (Pin 46 is SDIO/RSVD)		Not Available (Pin 46 is RSVD)
MIC_GND		Not Available		Not Available		Not Available	47	Local sense for mic.		Not Available (Pin 47 is RSVD)		Not Available (Pin 47 is SDIO/RSVD)		Not Available (Pin 47 is SDIO/RSVD)		Not Available (Pin 47 is RSVD)
MIC_P		Not Available		Not Available		Not Available	49	Differential signal in (+)		Not Available (Pin 49 is RSVD)		Not Available (Pin 49 is SDIO/RSVD)		Not Available (Pin 49 is SDIO/RSVD)		Not Available (Pin 49 is RSVD)
MIC_N		Not Available		Not Available		Not Available	48	Differential signal in (-)		Not Available (Pin 48 is RSVD)		Not Available (Pin 48 is SDIO/RSVD)		Not Available (Pin 48 is SDIO/RSVD)		Not Available (Pin 48 is RSVD)
SPK_P		Not Available		Not Available		Not Available	44	Diff. signal out (+)		Not Available (Pin 44 is RSVD)		Not Available (Pin 44 is SDIO/RSVD)		Not Available (Pin 44 is SDIO/RSVD)		Not Available (Pin 44 is RSVD)
SPK_N		Not Available		Not Available		Not Available	45	Diff. signal out (-)		Not Available (Pin 45 is RSVD)		Not Available (Pin 45 is SDIO/RSVD)		Not Available (Pin 45 is SDIO/RSVD)		Not Available (Pin 45 is RSVD)
Digital audio																
I2S_TXD	51	1.8 V, I2S out[12] / GPIO[7] Driver strength: 2 mA	51	1.8 V, I2S out / GPIO Driver strength: 6 mA	42	1.8 V, I2S data output Driver strength: 2 mA	35	1.8 V, I2S data output Driver strength: 5 mA	35	1.8 V, I2S out / GPIO Driver strength: 2 mA	35	Reserved for future use	35	1.8 V, I2S out / GPIO Driver strength: 6 mA	35	1.8 V, I2S out[13] / GPIO Driver strength: 6 mA
I2S_RXD	53	1.8 V, I2S in[12] / GPIO[7] Driver strength: 2 mA	53	1.8 V, I2S in / GPIO Driver strength: 6 mA	44	1.8 V, I2S data in input	37	1.8 V, I2S data input	37	1.8 V, I2S in / GPIO Driver strength: 2 mA	37	Reserved for future use	37	1.8 V, I2S in / GPIO Driver strength: 6 mA	37	1.8 V, I2S in[13] / GPIO Driver strength: 6 mA
I2S_WA	50	1.8 V, I2S sync[12] / GPIO[7] Driver strength: 2 mA	50	1.8 V, I2S sync / GPIO Driver strength: 6 mA	41	1.8 V, I2S sync Driver strength: 2 mA	34	1.8 V, I2S sync Driver strength: 6 mA	34	1.8 V, I2S sync / GPIO Driver strength: 2 mA	34	Reserved for future use	34	1.8 V, I2S sync / GPIO Driver strength: 6 mA	34	1.8 V, I2S sync[13] / GPIO Driver strength: 6 mA
I2S_CLK	52	1.8 V, I2S clock[12] / GPIO[7] Driver strength: 2 mA	52	1.8 V, I2S clock / GPIO Driver strength: 6 mA	43	1.8 V, I2S clock Driver strength: 2 mA	36	1.8 V, I2S clock Driver strength: 5 mA	36	1.8 V, I2S clock / GPIO Driver strength: 2 mA	36	Reserved for future use	36	1.8 V, I2S clock / GPIO Driver strength: 6 mA	36	1.8 V, I2S clock[13] / GPIO Driver strength: 6 mA
I2S1_TXD		Not Available (pin 49 is RSVD)		Not Available (pin 49 is RSVD)	40	1.8 V, I2S1 input / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available		Not Available		Not Available
I2S1_CLK		Not Available (pin 62 is host select)		Not Available (pin 62 is host select)	53	1.8 V, I2S1 sync / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available		Not Available		Not Available
I2S1_WA		Not Available (pin 63 is SDIO)		Not Available (pin 63 is SDIO)	54	1.8 V, I2S1 output / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available		Not Available		Not Available
I2S1_RXD		Not Available (pin 48 is RSVD)		Not Available (pin 48 is RSVD)	39	1.8 V, I2S1 clock / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available		Not Available		Not Available
Other																
CODEC_CLK	61	Provided by GPIO6[14]: 1.8 V, clock output Driver strength: 2 mA	61	Provided by GPIO6: 1.8 V, clock output Driver strength: 6 mA	52	1.8 V, clock output Driver strength: 4 mA		Not Available (pin 19 is RSVD)	19	1.8 V, clock output Driver strength: 4 mA		Not Available (pin 19 is GPIO6)	19	Provided by GPIO6: 1.8 V, clock output Driver strength: 6 mA	19	Provided by GPIO6: 1.8 V, clock output Driver strength: 2 mA

[12] Not supported by “00”, “01”, “60”, TOBY-L201-02S and TOBY-L220-62S product versions
[13] I2S is not supported by LARA-R6001D and LARA-R6401D data-only versions: I2S pins are by default set as pin disabled
[14] Not supported by “00”, “01”, “60” product versions

Pin name	N	TOBY-L2	N	TOBY-R2	N	LISA-U2	N	SARA-G3 [2]	N	SARA-U2	N	SARA-R41	N	LARA-R2	N	LARA-R6
GPIO																
GPIO1	21	1.8 V, GPIO Default: Wi-Fi enable Driver strength: 2 mA WWAN status signal on '00', '01', '60' versions	21	1.8 V, GPIO Default: Pin disabled Driver strength: 6 mA	20	1.8 V, GPIO Default: Pin disabled Driver strength: 6 mA	16	1.8 V, GPIO Default: Pin disabled Driver strength: 6 mA	16	1.8 V, GPIO Default: pin disabled Driver strength: 6 mA	16	1.8 V, GPIO Default: Pin disabled Driver strength: 2 mA	16	1.8 V, GPIO Default: Pin disabled Driver strength: 6 mA	16	1.8 V GPIO Default: Pin disabled Driver strength: 6 mA
GPIO2	22	1.8 V, GPIO[14] Default: Pin disabled Driver strength: 2 mA	22	1.8 V, GPIO Default: GNSS control Driver strength: 6 mA	21	1.8 V, GPIO Default: GNSS control Driver strength: 1 mA	23	1.8 V, GPIO Default: GNSS control Driver strength: 6 mA	23	1.8 V, GPIO Default: GNSS control Driver strength: 1 mA	23	1.8 V, GPIO Default: Pin disabled Driver strength: 2 mA	23	1.8 V, GPIO Default: GNSS control Driver strength: 6 mA	23	1.8 V, GPIO Default: GNSS control Driver strength: 6 mA
GPIO3	24	1.8 V, GPIO[14] Default: Pin disabled Driver strength: 2 mA	24	1.8 V, GPIO Default: GNSS Tx ready Driver strength: 6 mA	23	1.8 V, GPIO Default: GNSS Tx ready Driver strength: 6 mA	24	1.8 V, GPIO Default: GNSS Tx ready Driver strength: 5 mA	24	1.8 V, GPIO Default: GNSS Tx ready Driver strength: 6 mA	24	1.8 V, GPIO Default: Pin disabled Driver strength: 2 mA	24	1.8 V, GPIO Default: GNSS Tx ready Driver strength: 6 mA	24	1.8 V, GPIO Default: GNSS Tx ready Driver strength: 6 mA
GPIO4	25	1.8 V, GPIO[14] Default: Output / Low Driver strength: 2 mA	25	1.8 V, GPIO Default: Output/Low Driver strength: 6 mA	24	1.8 V, GPIO Default: GNSS RTC shar Driver strength: 6 mA	25	1.8 V, GPIO Default: GNSS RTC shar Driver strength: 6 mA	25	1.8 V, GPIO Default: GNSS RTC shar Driver strength: 6 mA	25	1.8 V, GPIO Default: Output/Low Driver strength: 2 mA	25	1.8 V, GPIO Default: Output/Low Driver strength: 6 mA	25	1.8 V, GPIO Default: Output/Low Driver strength: 6 mA
GPIO5	60	1.8 V, GPIO[14] Default: SIM detection Driver strength: 2 mA	60	1.8 V, GPIO Default: SIM detection Driver strength: 6 mA	51	1.8 V, GPIO Default: SIM detection Driver strength: 6 mA		GPIO not available. 1.8 V SIM detection provided on pin 42 SIM_DET		GPIO not available. 1.8 V SIM detection provided on pin 42 SIM_DET	42	1.8 V, GPIO Default: SIM detection Driver strength: 2 mA	42	1.8 V, GPIO Default: SIM detection Driver strength: 6 mA	42	1.8 V, GPIO Default: SIM detection Driver strength: 6 mA
GPIO6	61	1.8 V, GPIO[14] Default: clock output Driver strength: 2 mA		GPIO not available. 1.8 V clock out provided on pin 61, named GPIO6	39	1.8 V, I2S1_RXD / GPIO Default: I2S1_RXD Driver strength: 1 mA 1.8 V clock out provided on pin 52 CODEC_CLK		Not Available		GPIO not available. 1.8 V clock out provided on pin 19 CODEC_CLK	19	1.8 V, GPIO Default: Pin disabled Driver strength: 2 mA	19	GPIO not configurable: 1.8 V clock out set on pin 19, named GPIO6	19	GPIO not configurable: 1.8 V clock out set on pin 19, named GPIO6[15]
Antenna tuner																
RFCTRL1		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available (pin 97 is RSVD)	97	LARA-R6401/R6401D: 1.8 V, RF tuner output
RFCTRL2		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available (pin 97 is RSVD)	98	LARA-R6401/R6401D: 1.8 V, RF tuner output
Reserved																
RSVD		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 6 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 6 that must be externally tied to GND.		All the pins reserved for future use (RSVD) must be left floating except for the pin n° 5 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 33 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 33 that must be externally tied to GND.		All the pins reserved for future use (RSVD) can be left floating except for the pin n° 33 that can be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 33 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 33 that is intended to be externally accessible via a test point

Table 2: Summary of pin differences and compatibility level among modules

☞ For further guidelines to migrate between any of the u-blox SARA modules product versions, including SARA-G4, SARA-N2, SARA-N3, SARA-R42 and SARA-R5 series modules, as well as the SARA-G3, SARA-U2 and SARA-R41 series modules listed in Table 1, see

- the SARA modules migration guidelines application note [30]

[15] LARA-R6001D and LARA-R6401D data-only product versions do not support GPIO6 clock output.

☞ For further guidelines to migrate between any of the u-blox LARA modules product versions, see

- the LARA modules migration guidelines application note [31]

☞ For further details regarding characteristics, capabilities, usage or settings applicable for each interface of the modules, see

- the specific data sheet of related modules' series: TOBY-L1 [1], TOBY-L2 [2], TOBY-R2 [3], LISA-U2 [4], SARA-G3 [5], SARA-G4 [6], SARA-U2 [7], SARA-N3 [8], SARA-R41 / SARA-R42 [11], SARA-R5 [12], LARA-R2 [9], LARA-R6 [10]
- the specific system integration manual for the related modules' series: TOBY-L1 [13], TOBY-L2 [14], TOBY-R2 [15], LISA-U2 [16], SARA-G3 / SARA-U2 [19], SARA-G4 [18], SARA-N2 / SARA-N3 [17], SARA-R41 / SARA-R42 [21], SARA-R5 [23], LARA-R2 [20], LARA-R6 [21]
- the specific AT commands manual for related modules' series: TOBY-L1 [24], TOBY-L2 / TOBY-R2 / LISA-U2 / SARA-G3 / SARA-G4 / SARA-U2 / LARA-R2 [26], SARA-N2 / SARA-N3 [27], SARA-R41 / SARA-R42 [25], SARA-R5 [28], LARA-R6 [29]

3 Interfaces

3.1 Power management

3.1.1 Module supply (VCC)

The same compatible external circuit can be implemented for all TOBY, LISA, SARA, and LARA modules, for example the one described in Figure 3, even if there are minor differences in the **VCC** input voltage ranges and some differences in the current consumption figures.

The nominal voltage provided at the supply input must be within the normal operating range limits to allow module switch-on and optimized performance, and then the voltage must be held within the extended operating range limits to avoid module switch-off and reduced performances. For the detailed **VCC** input voltage range values, see Table 2 or the module's data sheet.

The maximum average current consumption of the modules may vary depending on the radio access technology and capabilities available with the module. For example, the maximum average current consumption of modules supporting the LPWA technologies LTE Cat M1 and/or NB-IoT, or the one of modules supporting only the 2G radio access technology, is in general lower than that of modules supporting higher LTE categories and/or UMTS/HSPA, due to differences in the technologies and related architecture.

Cellular modules that support any radio access technology with RF signal transmission not enabled in continuous mode, as the 2G TDMA radio technology, or the LTE TDD, or also the LTE FDD half-duplex (in LTE Cat M1 and/or NB-IoT), have a pulsed current profile in connected mode, when a call is enabled, with maximum peak of current consumption much higher in particular with the 2G radio technology considering the maximum RF power transmitted in the 2G low frequency bands may be up to ~2 W instead of the ~0.25 W maximum RF power transmitted in LTE, NB-IoT or UMTS/HSPA.

Cellular modules that support only LTE FDD full-duplex and/or UMTS/HSPA radio access technology, with RF signal transmission enabled in continuous mode, do not show a pulsed current profile typical of the 2G TDMA, the LTE TDD, or the LTE FDD half-duplex radio access technology.

For the detailed current consumption values, see the module's data sheet.

For a safe design margin, it is recommended to use a **VCC** supply source that can deliver double the typical **VCC** current consumption at maximum Tx power, normal ambient temperature and normal voltage condition shown in the module's data sheet.

The module's system integration manual illustrates examples of current consumption profiles for various basic operating conditions, and it includes detailed supply circuit design-in guidelines.

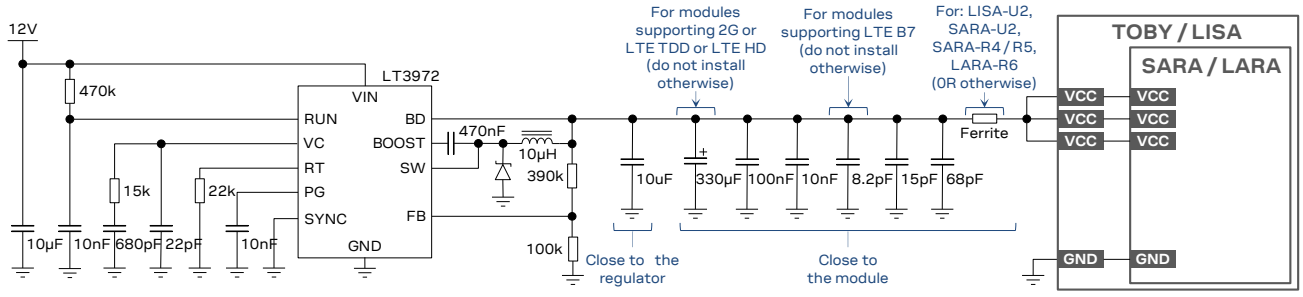

Figure 3: Example of compatible VCC supply application circuit using a high reliability step-down regulator

The three **VCC** pins of TOBY and LISA share the same pads on the top layer of the nested application board, which are positioned very close to the three **VCC** pads shared by SARA, and LARA modules to facilitate routing, as shown in the nested design top layer description shown in Figure 4.

Bypass capacitors with Self-Resonant Frequency in the supported radio frequency bands are placed very close to the **VCC** pins, at the narrowing of the **VCC** line implemented in the design, to filter EMI in the supported bands. Note that the bypass capacitors values change according to the operating bands of the module that is mounted. See the module's system integration manual for more details about proper design of the **VCC** supply line.

In the nested design variants for LISA-U2, SARA-U2, SARA-R4, SARA-R5, and LARA-R6 series modules, an additional series ferrite bead specifically designed for noise suppression in the GHz band (such as Murata BLM18EG221SN1) is placed close to the **VCC** pins of the modules to filter EMI, as recommended in the respective module's system integration manual.

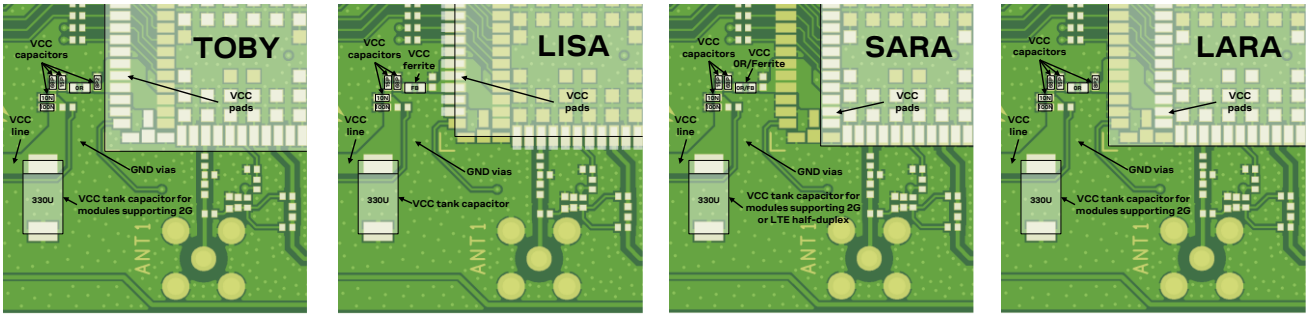

Figure 4: TOBY / LISA / SARA / LARA VCC line routing and components placement

3.1.2 RTC supply (V_BCKP)

All the modules, except SARA-R4, SARA-R5, and LARA-R6 series, have the **V_BCKP** pin providing the output of an internal low power voltage regulator that is always enabled when the module **VCC** supply voltage is within its valid operating range.

The same compatible external circuit can be implemented using the **V_BCKP** supply output to bias the pull-up for the **PWR_ON** input pin for TOBY-L1, LISA-U2, SARA-G3, and SARA-U2 modules, even if there are minor differences in the **V_BCKP** typical output voltage, as shown in Table 2 or in the module's data sheet.

The **V_BCKP** supply output must not be used to bias an external pull-up for the **PWR_ON** input of any of the other modules covered in the present application note, with the exception of the modules above, because the **PWR_ON** input is equipped with an internal pull-up to **VCC, V_BCKP** or an internal power supply depending on the module family. Consult the module's data sheet for more details.

The **V_BCKP** pin of all the modules except TOBY-L1 series can be used as input to supply the RTC when the **VCC** voltage is not present, providing RTC back-up functionality, which is not supported by TOBY-L1 modules.

The **V_BCKP** pin of TOBY and LISA share the same pad on the top layer of the nested application PCB, which is positioned very close to the **V_BCKP** pad shared by SARA and LARA to facilitate the routing.

3.1.3 Generic Digital Interfaces supply output (V_INT)

The same compatible external circuit can be implemented for TOBY, LISA, SARA, and LARA: all the modules provide a 1.8 V supply output at the **V_INT** pin, enabled when the modules are switched on and outside deep-sleep PSM / eDRX mode, as shown in Table 2 or in the module's data sheet.

The **V_INT** pin of TOBY and LISA share the same pad on the top layer of the nested application board, which is positioned very close to the **V_INT** pad shared by SARA and LARA to facilitate routing.

It is in general recommended to monitor the status of the **V_INT** pin by the external host application processor, to check whether the module is switched on, outside deep-sleep PSM / eDRX mode.

3.2 System functions

3.2.1 Module power-on

Table 3 summarizes the allowed power-on events of TOBY, LISA, SARA, and LARA modules. For more details, see the module's data sheet and system integration manual.

	TOBY-L2	TOBY-R2	LISA-U2	SARA-G3	SARA-U2	SARA-R41	LARA-R2	LARA-R6
From No-Power Mode	Applying **VCC**	Applying **VCC**, with ramp from 2.3 V to 2.8 V within 4 ms	Applying **VCC**, with ramp from 2.5 V to 3.2 V within 1 ms	Applying **VCC**, with ramp from 2.5 V to 3.2 V within 4 ms	Applying **VCC**, with ramp from 2.5 V to 3.2 V within 1 ms		Applying **VCC**, with ramp from 2.3 V to 2.8 V within 4 ms	
From Power-off Mode	Low level on **PWR_ON** for 5 ms min	Low pulse on **PWR_ON** for 50 µs min	Low pulse on **PWR_ON** for 50 µs ÷ 80 µs	Low level on **PWR_ON** for 5 ms min	Low pulse on **PWR_ON** for 50 µs ÷ 80 µs	Low pulse on **PWR_ON** for 0.15 s ÷ 3.2 s	Low pulse on **PWR_ON** for 50 µs min	Low pulse on **PWR_ON** for 0.15 s ÷ 3.2 s
	RTC alarm	RTC alarm	RTC alarm	RTC alarm (G340/G350)	RTC alarm		RTC alarm	
	Low pulse on **RESET_N** for 18 ms ÷ 0.8 s	Low pulse on **RESET_N** for 50 ms min	Low pulse on **RESET_N** for 50 ms min		Low pulse on **RESET_N** for 50 ms min		Low pulse on **RESET_N** for 50 ms min	

Table 3: Summary of power on events among modules

The same compatible external **PWR_ON** circuit can be implemented for TOBY, LISA, SARA, and LARA modules, as the one shown in Figure 5, even if there are minor differences in the **PWR_ON** input voltage levels ranges and in the low level time or low pulse time to switch-on the module (see Table 2 or the module's data sheet).

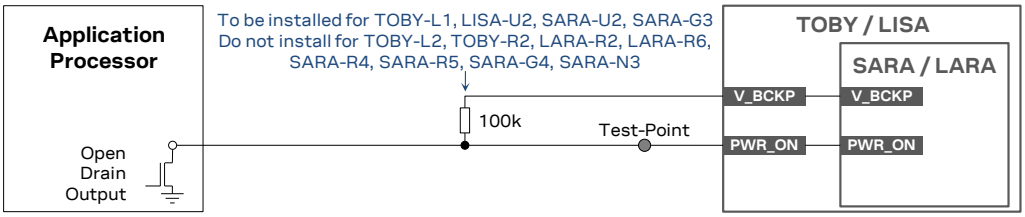

Figure 5: Example of compatible PWR_ON application circuits using an open drain output of an application processor

The line should be driven by open drain, open collector or contact switch, providing an external pull-up for the TOBY-L1, LISA-U2, SARA-U2 and SARA-G3 modules. An external pull-up is not needed for TOBY-L2 modules, which have internal pull-up to **VCC**, or TOBY-R2 and LARA-R2 modules, which have internal pull-up to **V_BCKP**, and not for any other module not mentioned above, which have internal pull-up. Consult the module's data sheet for more details.

The **PWR_ON** pin of TOBY and LISA share the same pad on the top layer of the nested application PCB, positioned very close to the **PWR_ON** pad shared by SARA and LARA to facilitate the routing.

Depending on the product, different ways to power on the module are supported:

- Auto power-on: the start-up event is triggered when a low to high transition is detected on the VCC pins of the module.
- Power-on by toggling the **PWR_ON** / **PWR_CTRL** line: the start-up event is triggered when a control pin is asserted for a valid time period and then released.

The following conditions apply regardless of the supported power-on mod:

- All the generic digital pins are tri-stated (not powered) before the switch-on of their supply source (**V_INT**). Therefore, any external signal connected to the generic digital pins must be tri-stated or set low at least before the activation of the **V_INT** supply output to avoid latch-up of circuits and allow a proper boot of the module.

- The **V_INT** generic digital interfaces supply output is enabled by the internal power management unit during the internal switch-on routine executed by the module.
- If supported, the **V_BCKP** output is enabled by the module as soon as **VCC** reaches valid value
- The duration of the boot phase and of pins' configuration phase varies between different modules' platforms, and it varies between generic digital interfaces and the USB interface due to specific host / device enumeration timings. The host application processor should not send any AT command until the end of this interface's configuration phase. The greeting text can be activated by the +CSGT AT command, to notify the external application that the module is ready to reply to AT commands. On UART ports, make sure to disable autobauding functionality and set **DTR** line low to see the greeting text after startup.

See the module's system integration manual for more details regarding the requirements and proper timings for the power-on sequence. Figure 6 and Figure 7 summarize the switch-on sequence from not-powered mode for auto-power-on modules and for modules that require toggling a control pin.

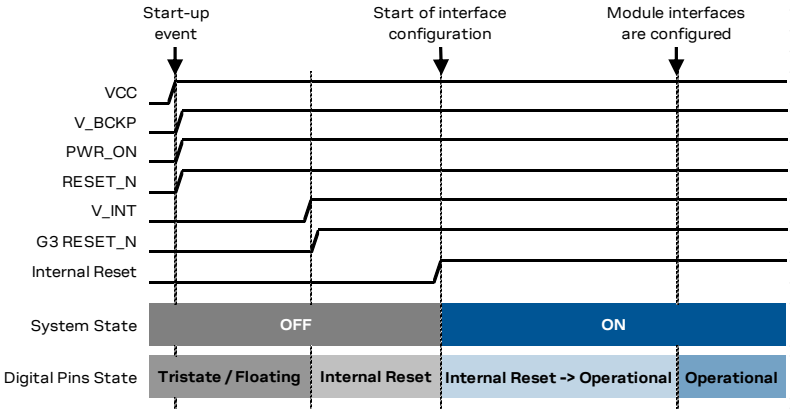

Figure 6: Switch-on sequence from not-powered mode for modules having the auto power on functionality

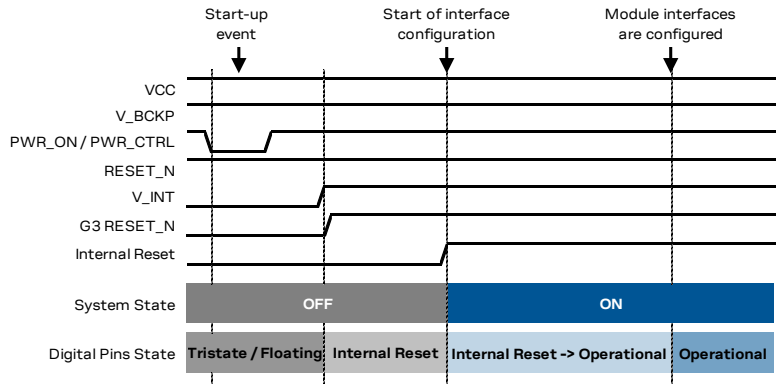

Figure 7: Switch-on sequence from power-off mode for modules requiring toggling of a control pin

3.2.2 Module power-off

All TOBY, LISA, SARA, and LARA modules can be properly switched off in this way:

- AT+CPWROFF command, for more details see the module's AT commands manual. The current parameters are saved in module's non-volatile-memory and a clean network detach is performed.

TOBY-R2, LISA-U2, SARA-U2, LARA-R2, LARA-R6, SARA-N3, SARA-R41, and SARA-R42 modules can also be properly switched off in this way:

- Low pulse on **PWR_ON** / **PWR_CTRL** pin, as shown in Table 2 or in the module's data sheet.

An abrupt emergency hardware shutdown of TOBY-L1, TOBY-L2, LARA-R6, and SARA-R41 modules is triggered when:

- a low level is applied to **RESET_N** input for a valid time period (see the Table 2 or the module's data sheet). In this case, the current parameters are not saved in module's non-volatile-memory and a proper network detach is not performed.

An abrupt emergency hardware shutdown of SARA-R5 modules is triggered when:

- a low level is first applied to **PWR_ON** input and then to the **RESET_N** input, for valid periods of time (see the module's data sheet [12]). In this case, the current parameters are not saved in module's non-volatile-memory and a proper network detach is not performed.

An abrupt emergency hardware shutdown occurs on SARA-G450 modules when:

- a low level is applied to **PWR_OFF** input. In this case, the current parameter settings are not saved in the module's non-volatile memory and a clean network detach is not performed.

☞ It is highly recommended to avoid an abrupt emergency hardware shutdown of the modules during modules normal operation: the abrupt emergency hardware shutdown should be executed only if reset or shutdown via AT commands fails or if the module does not reply to a specific AT command for a time period longer than the response time defined in module's AT commands manual

Figure 8 summarizes the recommended graceful switch-off sequence for all TOBY, LISA, SARA, and LARA modules, triggered by AT+CPWROFF command. For more details about the specific power-off sequence, consult the module's system integration manual.

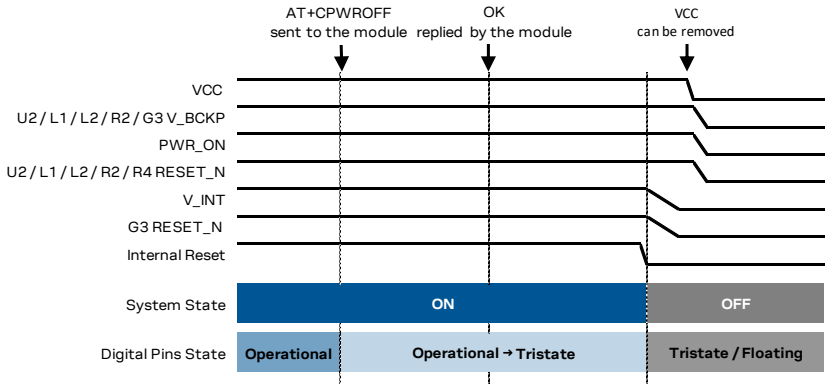

Figure 8: Description of TOBY, LISA, SARA, and LARA modules switch-off sequence by AT+CPWROFF command

1. When the AT+CPWROFF command is sent, the module starts the switch-off routine.
2. The module replies OK on the AT interface: the switch-off routine is in progress.
3. At the end of the switch-off routine, the internal reset signal is set low by the PMU
   The generic digital interfaces supply output (**V_INT**) is turned off by the module
   All the digital pins are tri-stated (not powered) because their supply is turned off
   The application can monitor **V_INT** to sense the end of the switch-off routine.
4. After the end of the switch-off routine, the module is in power-off mode as long as a valid supply is held. **V_BCKP** output (if available) is still turned on during this phase.
5. The module supply can be removed. The module enters not-powered mode.

☞ For the switch-off procedure above, a proper VCC supply must be held at least until the end of the modules' internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

3.2.3 Module reset

All TOBY, LISA, SARA, and LARA modules can be properly reset (re-booted) in this “software” way:

- AT+CFUN=16 / AT+CFUN=15 command, see the module’s AT commands manual. The current parameter settings are saved in module’s non-volatile memory and a clean network detach is done.

An abrupt hardware reset (re-boot) is performed on TOBY-L1 and SARA-R41 series modules in this “hardware” way:

- Low level on the **RESET_N** pin, normally high due to internal pull-up, for a valid time and then force the low level on the **PWR_ON** pin, normally high, for a valid time period. The current parameter settings are not saved in module’s non-volatile memory and a clean network detach is not done. For values of the valid time period, see Table 2 or the module’s data sheet.

An abrupt hardware reset (re-boot) is performed on SARA-R42 series modules in this way:

- Low level on the **PWR_CTRL** pin, normally high due to internal pull-up, for a valid time period. The current parameter settings are not saved in module’s non-volatile memory and a clean network detach is not performed. For values of the valid time period, see module’s data sheet [11].

An abrupt hardware reset (re-boot) is performed on SARA-G4 in this way:

- low level is applied on the **PWR_OFF** input pin and then a low level is applied on the **PWR_ON** input pin for valid time periods. The current parameter settings are not saved in module’s non-volatile memory and a clean network detach is not performed. For values of the valid time period, see the module’s data sheet [6]

An abrupt hardware reset (re-boot) is performed on any other TOBY, LISA, SARA, and LARA module not outlined above in this way:

- Low level on the **RESET_N** pin, normally high by internal pull-up, for a valid time. The current parameter settings are not saved in module’s non-volatile memory and a clean network detach is not performed. For values of the valid time period, see Table 2 or the module’s data sheet.

The same compatible external reset circuit can be implemented for TOBY, LISA, SARA, and LARA modules as illustrated in Figure 9, even if there are minor differences in the **RESET_N** input voltage level ranges and in the low level time, as shown in Table 2 or in the module’s data sheet. The line should be driven by open drain, open collector or contact switch, because all the modules are equipped with an internal pull-up.

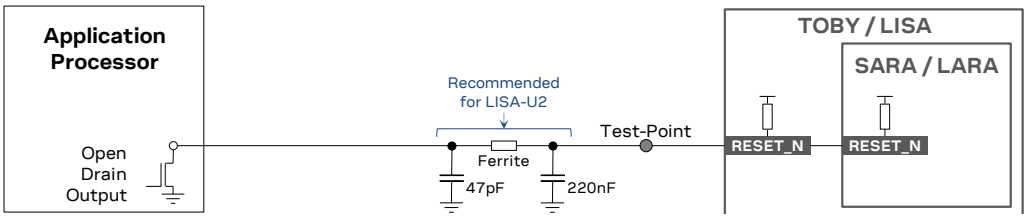

Figure 9: Example of compatible RESET_N application circuits using an open drain output of an application processor

The **RESET_N** pin of TOBY / LISA share the same pad on the top layer of the nested application board, which is positioned very close to the **RESET_N** pad shared by SARA and LARA to facilitate routing.

On the **RESET_N** line of the nested application board, there are spaces to mount proper bypass capacitors and a series ferrite bead / EMI suppression filter as additional circuit precautions for LISA-U2 series modules to satisfy ESD immunity test requirements, as suggested in LISA-U series system integration manual [18]. These additional components are not required for the other modules.

3.2.4 External 32 kHz input (EXT32K)

SARA-G300 and SARA-G310 modules provide the **EXT32K** input pin, which must be fed by a proper 32 kHz signal (e.g. the one provided by the **32K_OUT** output of the same modules), to provide the reference clock for the RTC, allowing low power idle-mode and RTC functions support (see Table 2 or SARA-G3 data sheet [5]).

TOBY, LISA, LARA, and the other SARA modules do not provide the **EXT32K** input pin.

SARA-G300 / SARA-G310 **EXT32K** pin shares a pad on the top layer of the nested PCB with the **RSVD** (reserved) pin of the other SARA modules, while the same pad is not used for any TOBY or LISA pins.

A 0 Ω series resistor can be mounted to connect the **EXT32K** pin with the **32K_OUT** pin. Otherwise, a 32 kHz signal can be provided by mounting an external oscillator circuit.

3.2.5 Internal 32 kHz output (32K_OUT)

SARA-G300 and SARA-G310 modules provide the **32K_OUT** output pin, which provides a 32 kHz reference signal suitable only to feed the **EXT32K** input pin of the same modules.

TOBY, LISA, LARA, and the other SARA modules do not provide the **32K_OUT** output.

The **32K_OUT** pad for SARA-G300 / SARA-G310 is shared on the top layer of the nested PCB with the **GPIO3** pad for the other SARA / LARA modules, while the same pad is not shared with any pad for TOBY and LISA.

3.2.6 Module / host configuration selection

LARA-R2 modules include one pin (**HOST_SELECT**) for the selection of module / host processor configuration, but the functionality is not supported by the FW. Therefore, the pin can be left unconnected or grounded.

TOBY-L2 and TOBY-R2 modules include two **HOST_SELECTx** pins, but the functionality is not supported by the FW. Therefore, the pin can be left not connected or it can also be grounded.

TOBY-L1, LISA, and SARA modules do not provide host select input pins.

Host select pins of TOBY-L2 and TOBY-R2 share the pads on the top layer of the nested PCB with **RSVD** pins of TOBY-L1 and LISA, while the host select pin of LARA-R2 shares the pad with a **GND** pin of LARA-R6 and SARA-G, SARA-U2, SARA-R4, SARA-N3.

3.3 RF connection

3.3.1 RF interface for Tx/Rx main antenna

The same compatible external circuit can be implemented for all the TOBY, LISA, SARA, and LARA modules on the RF input/output for the main Tx/Rx antenna (**ANT1** pin of TOBY and LARA, **ANT** pin of LISA and SARA), even if there are some differences in the operating bands frequency ranges, as summarized in Figure 10.

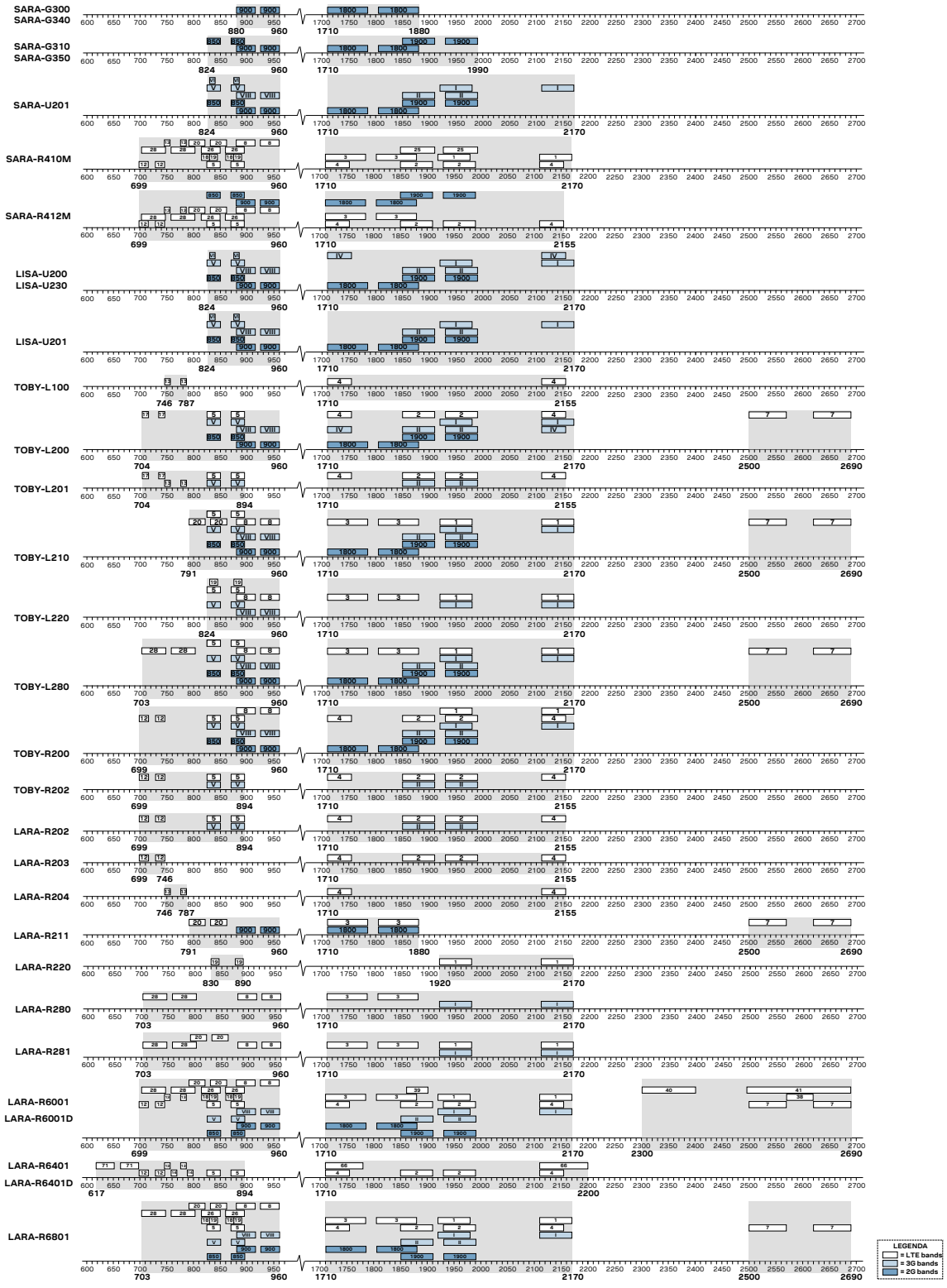

Figure 10: Summary of operating bands frequency ranges among TOBY, LISA, SARA, and LARA modules

The **ANT1** / **ANT** pin of TOBY, LISA, SARA, and LARA share the same pad on the top layer of the nested application board, so that a unique 50 Ω transmission line can be implemented on the application board for the main RF input/output. This is shown in the nested design top layer description in Figure 11 to Figure 15.

On the main RF line of the nested application board, there is space to mount a high-pass filter (series capacitor and shunt inductor) as additional circuit precaution for LISA-U2 and SARA-U2 modules to satisfy ESD immunity test requirements, as suggested in the module's system integration manual. These additional components are not required for TOBY and SARA-G3 modules, which provide ESD immunity up to ±4 / ±8 kV for Contact / Air Discharge according to IEC 61000-4 2.

On the main RF line of the nested application board there are spaces to mount a high-pass filter (series capacitor) as part of the main antenna detection circuit connected to the **ANT_DET** pin of TOBY-L2, TOBY-R2, LARA-R2, SARA-R4, SARA-U2, SARA-G340, and SARA-G350 modules, as suggested in the module's system integration manual. These additional parts are not required for LISA-U2 modules, which are equipped with internal circuit for antenna detection support, and for the TOBY-L1 and SARA-G300 / SARA-G310 modules, which do not support antenna detection.

3.3.2 RF interface for Rx MIMO / diversity antenna

The same compatible external circuit can be implemented for TOBY, LARA, and LISA-U230 on the RF input for the Rx MIMO antenna or for the Rx diversity antenna (**ANT2** pin of TOBY or LARA, **ANT_DIV** pin of LISA-U230), even if there are some differences in the operating bands frequency ranges, as summarized in Figure 10.

The **ANT2** / **ANT_DIV** pin of TOBY, LARA, and LISA-U230 share the same pad on the top layer of the nested application board, a 50 Ω transmission line can be implemented on the application board, as in the nested design top layer described from Figure 11 to Figure 15.

The SARA modules and the other LISA-U2 series modules do not support Rx diversity nor MIMO.

On the secondary RF line of the nested application board there is space to mount a high-pass filter (series capacitor) as part of the secondary antenna detection circuit connected to the **ANT_DET** pin of TOBY-L2, TOBY-R2, and LARA modules, as suggested in the module's system integration manual.

ANT2 / **ANT_DIV** pin of TOBY, LARA, and LISA-U230 shares a pad on the top layer of the nested application board with the antenna detection input (**ANT_DET** pin) of SARA-G340 / SARA-G350 and SARA-U2 modules, and with a **RSVD** (reserved) pin of the other LISA-U2 modules and SARA-G300 / SARA-G310 modules.

3.3.3 Antenna detection interface (ANT_DET)

An external application circuit can be implemented to provide antenna detection functionality as described in Figure 11 to Figure 14. Figure 15 shows the stack-up of the example nested design board and view of the different layers close to RF and VCC circuits.

The **ANT_DET** pin of SARA modules shares a pad on the top layer of the nested application board with the **ANT2** / **ANT_DIV** / **RSVD** pin of TOBY, LARA, and LISA modules.

The **ANT_DET** pin of TOBY modules does not share a pad on the top layer of the nested application board with the other LISA, SARA, and LARA modules.

The **ANT_DET** pin of LARA modules shares a pad on the top layer of the nested application board with a **RSVD** pin of TOBY and with a **GND** pin of SARA and LISA modules.

LISA-U2 modules has an internal circuit for antenna detection support. Thus, external antenna detection components are not mounted for these modules. In the LISA-U2 nested design hardware release variant (HR_271AG0), a high-pass filter (series capacitor and shunt inductor) is provided on the main RF line as additional circuit precaution to satisfy ESD immunity test requirements, as suggested in LISA-U series system integration manual [18]. These additional components prevent support of antenna detection functionality by LISA-U2 modules on the HR_271AG0 nested design hardware release variant.

TOBY-L1 and SARA-G300 / SARA-G310 modules do not support the antenna detection. Thus, external antenna detection components are not mounted for these modules.

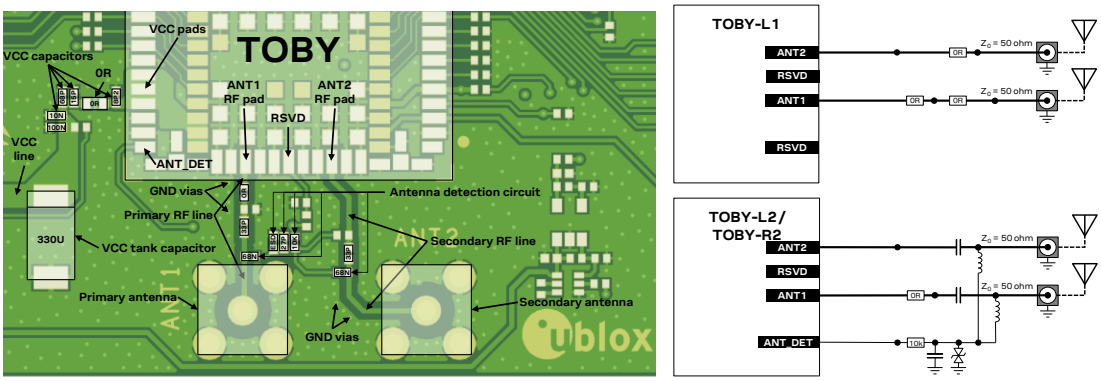

Figure 11: TOBY RF and VCC lines routing and components placement

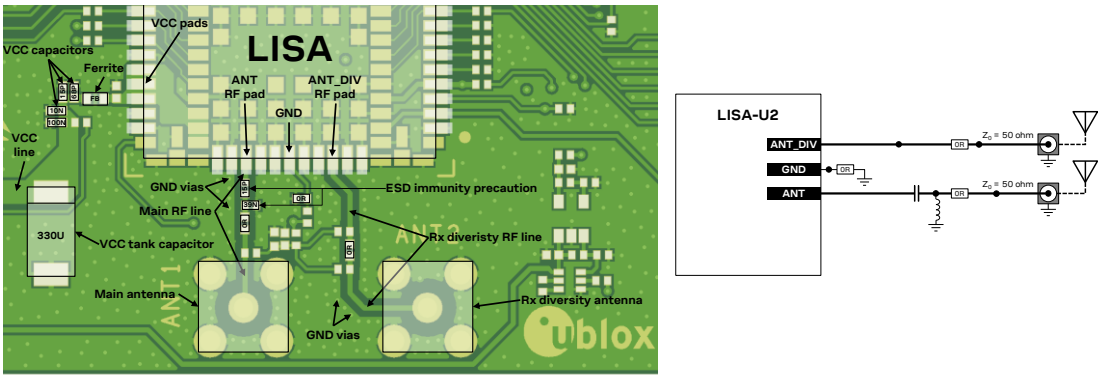

Figure 12: LISA RF and VCC lines routing and components placement

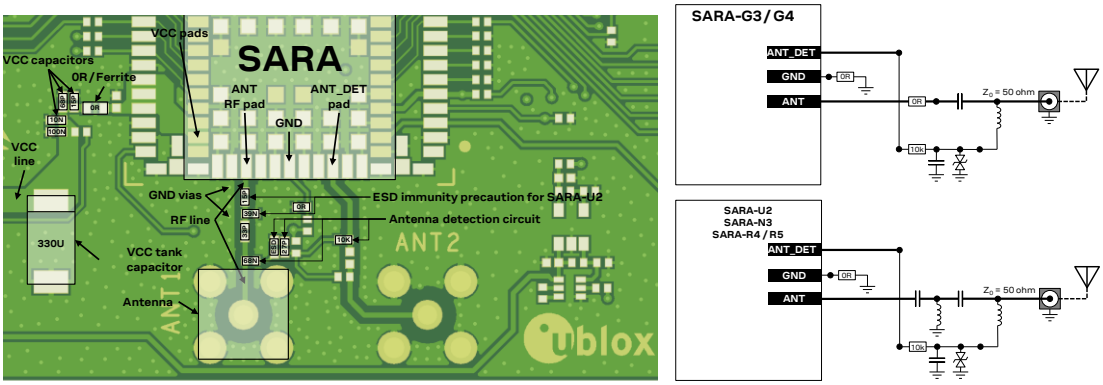

Figure 13: SARA RF and VCC lines routing and components placement

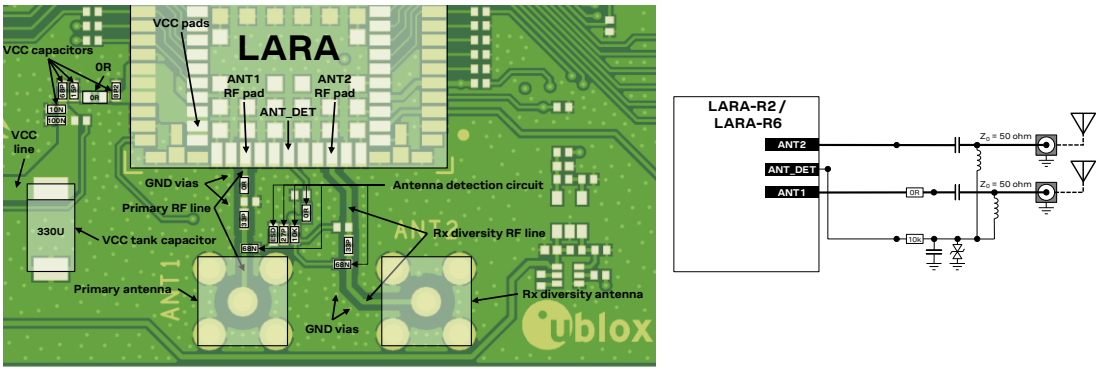

Figure 14: LARA RF and VCC lines routing and components placement

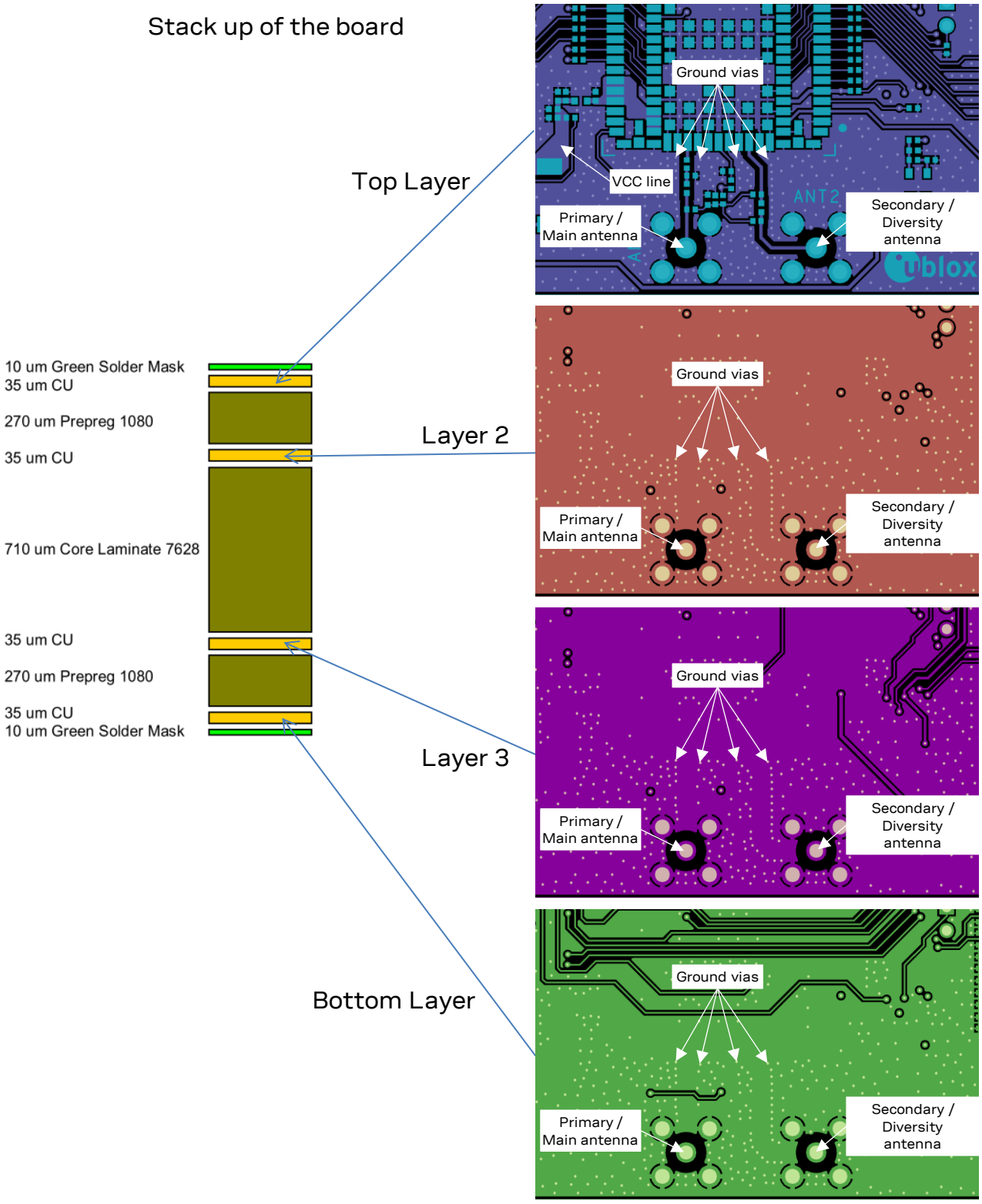

Figure 15: Stack-up of the nested design board and view of the different layers close to RF and VCC circuits

3.4 SIM interface

The same compatible external circuit can be implemented for TOBY, LISA, SARA, and LARA modules: 1.8 V and 3.0 V SIM card / IC are supported over the available SIM interface.

SIM card detection function is available on the **GPIO5** pin of TOBY-L2, TOBY-R2, and LISA-U2 modules, and the pin shares the same pad on the top layer of the nested application board. The pad is positioned very close to the pad shared by SARA / LARA modules for the SIM card detection pin (**SIM_DET** pin or **GPIO5** pin).

TOBY-L1 and SARA-N3 modules do not support the SIM card detection function, while SIM card hot insertion/removal function is additionally configurable on the same pin of TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, SARA-G3, SARA-U2, SARA-R5, LARA-R2, and LARA-R6 modules.

Figure 16 shows an example of compatible application circuit for the connection of a removable SIM card placed in a SIM card connector equipped with a normally open mechanical switch for the optional implementation of the SIM card detection function.

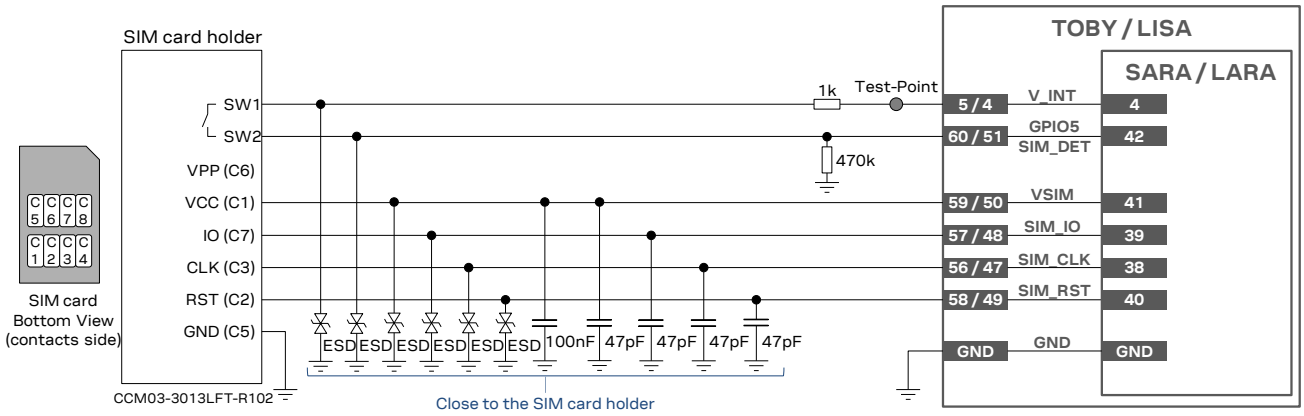

Figure 16: Example of compatible application circuit connecting a removable SIM card, with SIM card detection implemented

SIM interface pins of TOBY / LISA, including the pin providing the SIM card detection function, share the same pads on the top layer of the nested application board. These pads are positioned very close to the SIM pads shared by SARA / LARA modules to facilitate routing; see Figure 17.

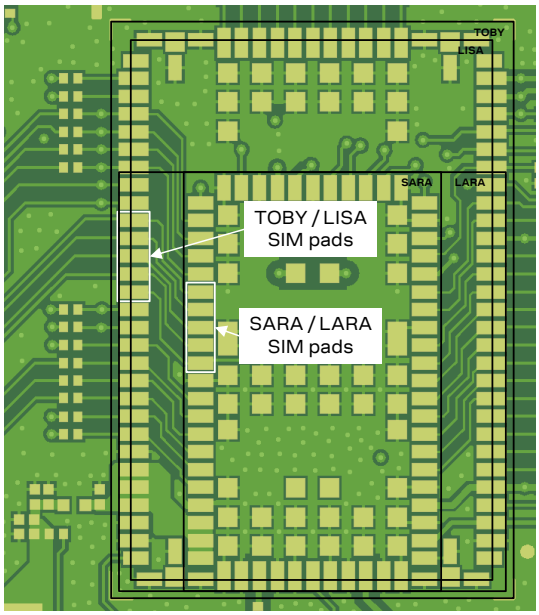

Figure 17: SIM interface pads for TOBY / LISA and SARA / LARA modules' SIM pins are positioned to facilitate routing

3.5 Serial interfaces

3.5.1 UART interface

The same compatible external circuit for a 1.8 V UART interface can be implemented for TOBY, LISA, SARA, and LARA modules, as shown in Figure 18. The communication with a 3.0 V Application Processor (DTE) is implemented by appropriate unidirectional voltage translators. This provides a partial power down feature so that either the DTE 3.0 V supply or the **V_INT** 1.8 V supply of the module can be ramped up first.

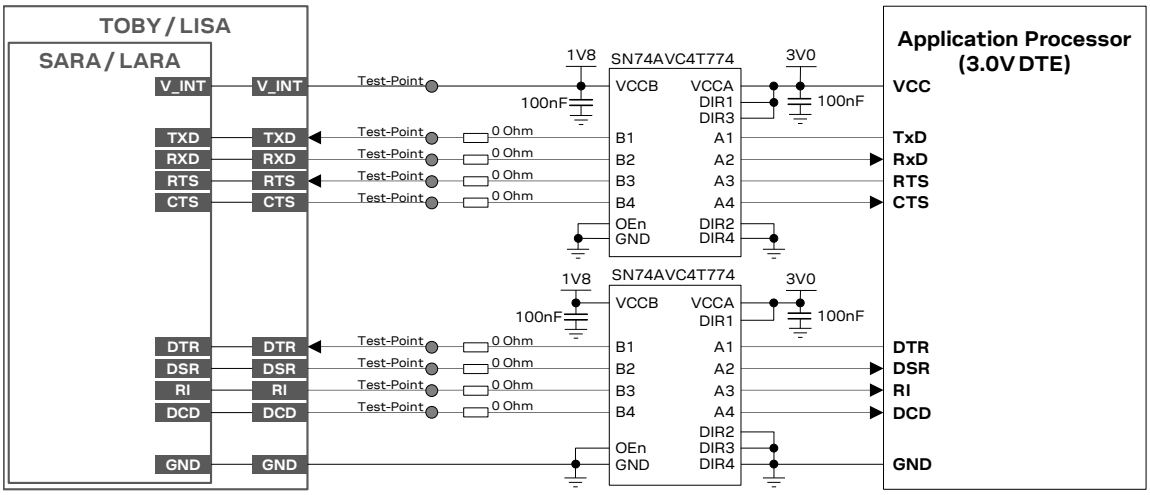

Figure 18: Compatible UART interface application circuit with complete V.24 serial communication with 3.0 V DTE

All the modules support a UART interface, except TOBY-L1 and the product version “00” of TOBY-L2 modules.

Table 2 and the module’s data sheet report minor differences for internal pull-ups and drivers strengths.

UART interface pins of TOBY / LISA share the same pads on the top layer of the nested application board, while SARA / LARA pins do not share the same pads, but they are positioned very close to each other facilitating routing, as shown in Figure 19.

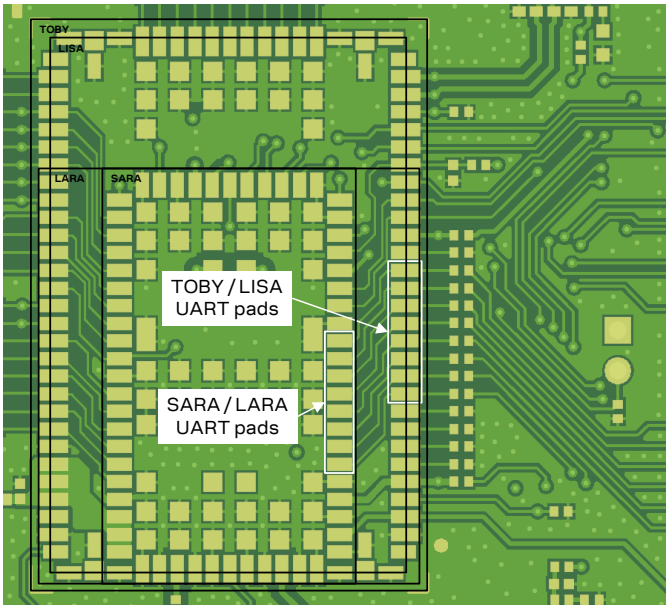

Figure 19: UART interface pins for TOBY / LISA and SARA / LARA modules are positioned to facilitate routing

3.5.2 UART AUX interface

SARA-G3 modules provide an auxiliary UART interface on the **RXD_AUX** / **TXD_AUX** pins #28 and #29 that share the same pads on the top layer of the nested application board with the USB data interface pins (**USB_D-** / **USB_D+**) of SARA-U2, SARA-R4, SARA-R5, and LARA modules: 0 Ω series resistors are provided to detach the auxiliary UART signals and avoid stubs on the impedance-controlled USB lines (see Figure 20 and Figure 21).

The pads for SARA-G3 auxiliary UART on the nested application board are not shared with any TOBY and LISA pins.

Latest SARA-G4 modules support an auxiliary UART interface on the **RXD_AUX** / **TXD_AUX** pins #19 and #17. Latest SARA-U2 and LARA-R2 modules support an auxiliary UART interface as alternative function of the I2C interface pins **SDA** and **SCL**. The SARA-R42, SARA-R5, and LARA-R6 modules support an auxiliary UART interface as alternative function of the pins **DCD** (as data output), **DTR** (as data input), **RI** (as flow control output), **DSR** (as flow control input).

3.5.3 USB interface

All the modules except SARA-G3, SARA-G4 and SARA-N3 provide a High-Speed USB 2.0 interface.

USB_D- / **USB_D+** pins of TOBY and LISA share the same pads on the top layer of the nested application board: the impedance-controlled USB data lines (differential characteristic impedance Z_0 = 90 Ω and common mode characteristic impedance Z_{CM} = 30 Ω as per USB 2.0 specifications) are routed on the top layer of the nested application board providing direct connection between TOBY / LISA pins and the USB connector.

USB_D- / **USB_D+** pins of SARA-U2, SARA-R4, SARA-R5, and LARA modules do not share the same pads with the **USB_D-** / **USB_D+** pins of TOBY and LISA: 0 Ω series resistors are provided on the bottom layer, close to TOBY / LISA pads, to detach the signals when TOBY / LISA modules are mounted, avoiding stubs on the USB lines (see Figure 20 and Figure 21).

USB_D- / **USB_D+** pins of SARA-U2, SARA-R4, SARA-R5, and LARA modules share the same pads with the **RXD_AUX** / **TXD_AUX** pins of SARA-G3 modules: 0 Ω series resistors are provided on the bottom layer, close to SARA / LARA pads, to detach the signals and avoid stubs on the impedance-controlled USB lines (see Figure 20 and Figure 21).

In the nested design BoM variants for TOBY-R2, LISA-U2, SARA-U2, SARA-R41, SARA-R5, LARA-R2, and LARA-R6 modules there are two 0 Ω series resistors to route the VBUS supply (+5V) from the USB connector to the **VUSB_DET** pin of TOBY-R2 (pin 4), LISA-U2 (pin 18), or SARA-U2 / SARA-R41 / SARA-R5 / LARA-R2 / LARA-R6 (pin 17) respectively (see Figure 20).

TOBY-L2 modules do not support the **VUSB_DET** functionality: the **VUSB_DET** pin (pin 4) must be left unconnected, and it is accordingly left unconnected in the nested design variants for TOBY-L2 modules. TOBY-L1 modules do not require an additional pin for VBUS USB supply, so they have no **VUSB_DET** pin.

The LISA **VUSB_DET** pin 18 shares the pad on the top layer of the nested application board with the TOBY **RSVD** pin 19, while the LISA **GND** pin 3 shares the pad with the TOBY pin 4, which is **RSVD** on TOBY-L1, not supported on TOBY-L2, **VUSB_DET** on TOBY-R2. A 0 Ω series resistor is used to connect the pad to GND only if LISA is mounted. The pad for SARA-U2 / SARA-R4 / SARA-R5 / LARA-R2 / LARA-R6 **VUSB_DET** pin is not shared with any TOBY and LISA pin; the signal is routed from the pad designed for LISA **VUSB_DET** pin to the pad designed for the SARA-U2 / SARA-R4 / SARA-R5 / LARA-R2 / LARA-R6 **VUSB_DET** pin (see Figure 20).

See the module's data sheet and system integration manual for detailed USB features description, and for guidelines about **USB_D-** and **USB_D+** High-Speed data lines routing rules.

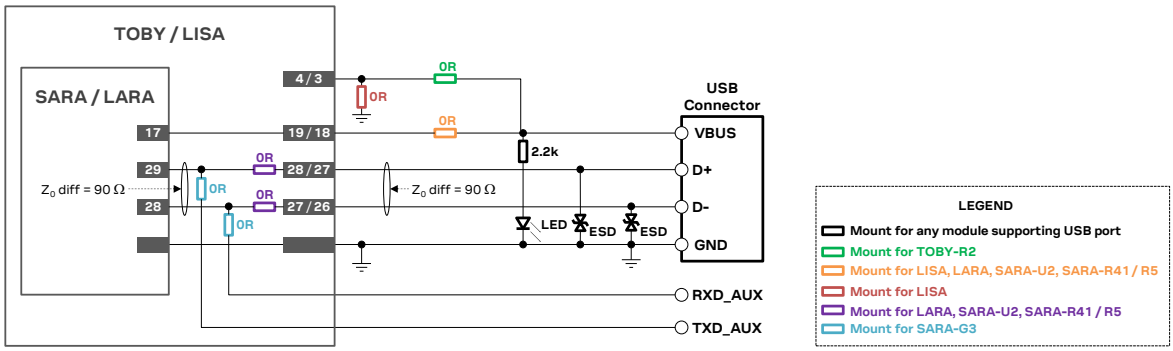

Figure 20: TOBY / LISA / LARA / SARA USB and SARA-G3 UART AUX signals schematic diagram

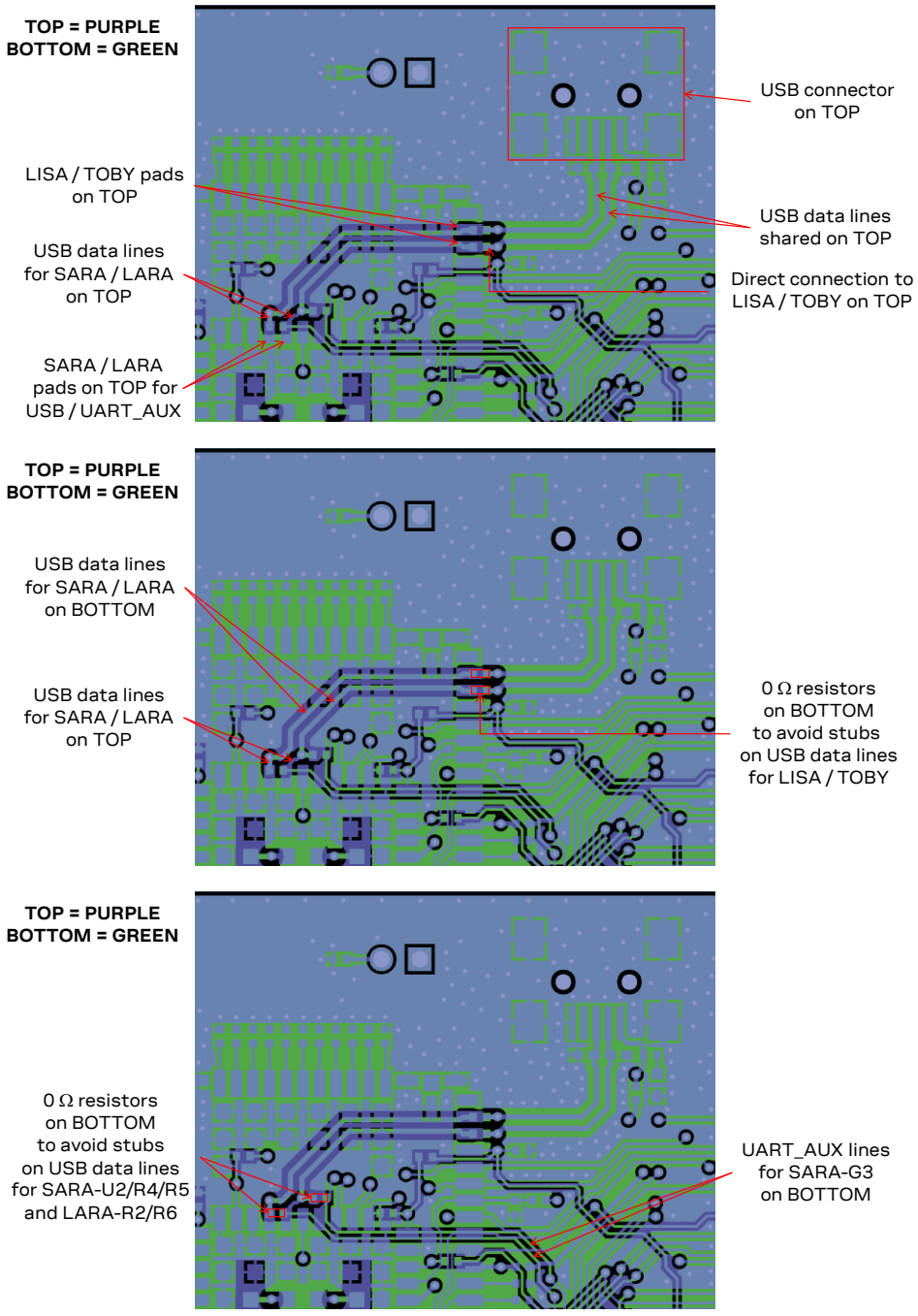

Figure 21 : TOBY / LISA / SARA-U2 / SARA-R4 / LARA USB / SARA-G3 UART AUX signals layout description

3.5.4 HSIC interface

LARA-R2 modules provide a High-Speed USB Inter-Chip interface (**HSIC_DATA**, **HSIC_STRB**), which is not available on the other modules. The HSIC interface pins of LARA-R2 modules do not share pads on the top layer of the nested application board with pins of the other modules.

3.5.5 SPI interface

LISA-U2 modules provide a 5-wire Inter-Processor Communication SPI interface that is not available on the other modules in this application note.

SPI interface pins of LISA-U2 modules share pads on the top layer of the nested application board with **RSVD** (reserved) pins of TOBY-L1 modules and with SDIO interface pins of TOBY-L2 and TOBY-R2 modules, while the same pads are not shared with any SARA / LARA pins.

SARA-R5 modules include a 4-wire SPI interface that is not supported by current products versions, except for diagnostic purposes. SPI interface pins of SARA-R5 modules share pads on the top layer of the nested application board with SDIO pins of SARA-R41 and LARA-R2 modules (that do not support this interface with current FW), with GNSS peripheral interfaces pins of SARA-R42 modules, with **RSVD** (reserved) pins of SARA-N3 and LARA-R6 modules, and with the analog audio interface pins of SARA-G3 / G4 modules. To select between SPI, SDIO, RSVD, or analog audio interfaces, 0 Ω resistors are needed in series with the related pins. SARA-R5 SPI interface pins are not shared with any LISA / TOBY module.

See the LISA-U series system integration manual [16] and the SARA-R5 series system integration manual [23] for application circuits and further details.

3.5.6 I2C interface

All the modules, except SARA-G300, SARA-G310, TOBY-L1, and some initial product versions of TOBY-L2, SARA-G4, SARA-N3 and SARA-R41 modules, provide a 1.8 V I2C bus compatible interface.

The same compatible external circuit can be implemented: all the modules except TOBY-L1 and TOBY-L2 support communication with u-blox GNSS receivers over the I2C interface, and all the modules except TOBY-L1 and SARA-G3 support communication with any I2C target over the I2C.

The I2C pins of TOBY-L2, TOBY-R2, and LISA-U2 modules share pads on the top layer of the nested application board. The same pads are used by TOBY-L1 **RSVD** (reserved) pins and are positioned very close to the I2C pads shared by SARA / LARA modules to facilitate routing.

Table 4 summarizes additional GNSS functionalities provided over GPIOs, where supported by module FW (more details in the module's data sheet, system integration manual and AT commands manual).

Function	SARA / LARA	LISA-U2	TOBY-R2	Comments
GNSS data ready	**GPIO3** / pin 24	**GPIO3** / pin 23	**GPIO3** / pin 24	The GNSS receiver sends this interrupt to the cellular module to claim data available on I2C
GNSS RTC sharing	**GPIO4** / pin 25	**GPIO4** / pin 24	**GPIO4** / pin 25	The cellular module sends this interrupt to the GNSS receiver to provide timing information
GNSS supply enable	**GPIO2** / pin 23	**GPIO2** / pin 21	**GPIO2** / pin 22	This is an output of the cellular module used to enable/disable the supply of the GNSS receiver

Table 4: GNSS custom function overview over GPIOs

3.5.7 SDIO interface

TOBY-L2 modules support a 4-bit SDIO (Secure Digital Input Output) high speed serial interface for communicating with an external u-blox short range radio communication Wi-Fi module.

The SDIO interface is available but not supported as communication interface on TOBY-R2, LARA-R2, SARA-R41, and SARA-R5 modules, and the pins are configured in high-impedance mode accordingly. The SDIO interface is not provided by TOBY-L1, LISA, and SARA modules not previously mentioned.

SDIO interface pins of TOBY-L2 and TOBY-R2 modules share pads on the top layer of the nested application board with **RSVD** (reserved) pins of TOBY-L1 and with SPI / I2S1 pins of LISA-U2 modules.

SDIO interface pins of LARA-R2, SARA-R4, and SARA-R5 modules share pads on the top layer of the nested application board with analog audio pins of SARA-G350 and SARA-G340 modules, and with **RSVD** (reserved) pins of SARA-U2, SARA-G300, and SARA-G310 modules.

The pads for the SDIO pins of TOBY-L2 and TOBY-R2 modules are positioned very close to the pads for the SDIO pins of LARA-R2 in order to facilitate routing.

See the modules' system integration manuals and data sheets for application circuits and further details.

3.6 Audio interface

3.6.1 Analog audio

TOBY, LISA-U2, LARA, SARA-R4, SARA-R5, SARA-U2, SARA-N3, SARA-G300, and SARA-G310 modules do not provide an analog audio interface, but SARA-G340, SARA-G350, and SARA-G450 modules do.

All the modules, except SARA-R4, SARA-R5, SARA-N3, SARA-G300, SARA-G310, TOBY-L1, and the data-only variants of LARA-R6 and TOBY-L2 modules, provide digital audio interface: analog audio capability can be provided by converting the digital signal with an external audio codec. This is implemented on the nested application board for all the modules supporting digital audio, except SARA-G340 and SARA-G350, which have the analog audio interface available directly at module pin level. The external audio codec has DAC and ADC integrated, converting an incoming digital data stream to analog audio output and converting the microphone signal to the digital bit stream over the digital audio interface.

The analog audio interface pins of SARA-G340 / SARA-G350 modules and the digital audio interface pins of TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, and LARA modules are positioned to ease routing.

The same compatible external audio circuit can be implemented, as the one shown in Figure 22:

- TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, LARA-R2, and LARA-R6 modules:
  - **I2S_TXD**, **I2S_RXD**, **I2S_WA**, **I2S_CLK** digital audio interface is routed by 0 Ω series resistors to the audio codec, which provides the digital / analog audio conversion
  - **SDA**, **SCL** I2C interface is routed to the audio codec configurable by AT commands over I2C
  - **GPIO6** / **CODEC_CLK** digital clock output is routed to the audio codec providing the host clock
  - Codec analog audio input lines are routed as differential pair to an external microphone, also providing the bias for the external microphone by a two 2.2 kΩ resistors circuit
  - Codec analog audio output lines are routed as differential pair to an external speaker

- SARA-G340 / SARA-G350 modules:
  - **MIC_BIAS** supply output is routed to bias an external microphone by a bridge structure created by two 2.2 kΩ and one 4.7 kΩ resistors circuit, plus an additional 1.5 kΩ series resistor
  - **MIC_GND** is routed as sense line providing the star connection to ground for microphone lines
  - **MIC_P**, **MIC_N** analog audio input lines are routed as differential pair to the microphone bias circuit with two 100 nF DC-blocking series capacitors
  - **SPK_P**, **SPK_N** analog audio output lines are routed as differential pair to an external speaker

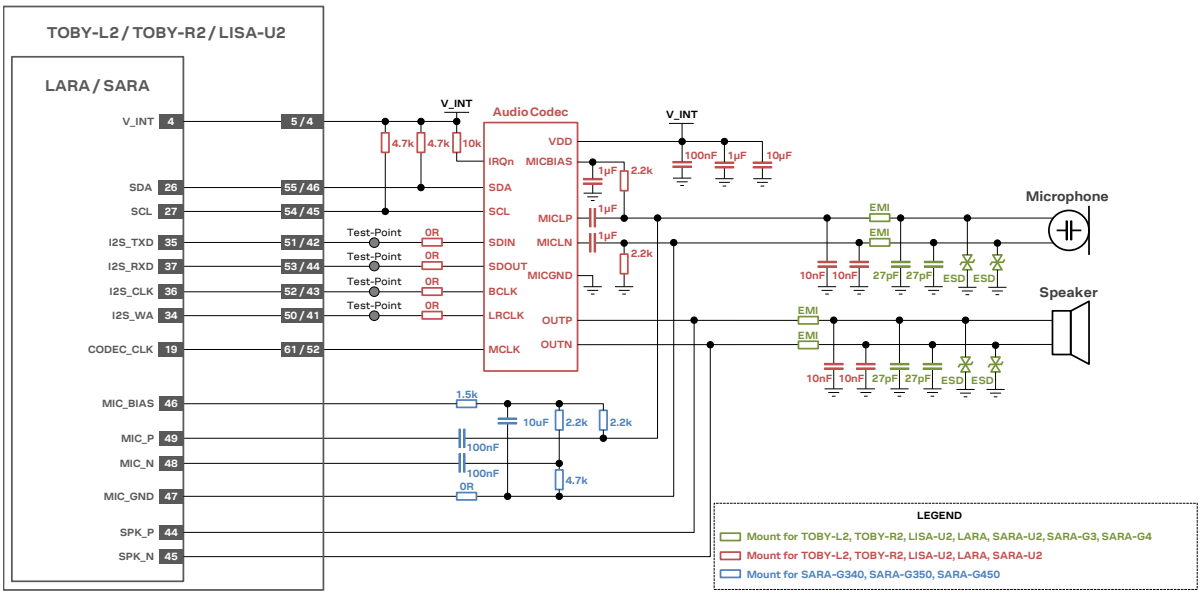

Figure 22: Compatible TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, LARA, and SARA-G340 / SARA-G350 audio circuit example

3.6.2 Digital audio

3.6.2.1 First digital audio interface

All the modules, except SARA-G300, SARA-G310, SARA-R4, SARA-R5, TOBY-L1 and some product versions of TOBY-L2 and LARA modules, support digital audio.

A digital audio interface is provided on the **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA** pins of TOBY, LISA, SARA, and LARA modules, where supported by the module firmware. The same compatible external circuit can be implemented according to external digital audio device capabilities. For more details, see the module's data sheet, system integration manual and AT commands manual.

The digital audio interface pins of TOBY / LISA share the same pads on the top layer of the nested application board, which are positioned very close to the SIM pads shared by SARA / LARA modules to facilitate routing, as shown in Figure 23.

Optionally, compatibility for digital audio interface is also provided for LISA-U1 series modules.

For further details regarding digital audio interface settings and application circuits, see the module's data sheet, system integration manual and AT commands manual.

3.6.2.2 Second digital audio interface

LISA-U2 modules provide a second I2S interface on the **I2S1_TXD**, **I2S1_RXD**, **I2S1_CLK**, **I2S1_WA** pins. On TOBY, SARA, and LARA modules the second I2S interface (I2S1) is not available.

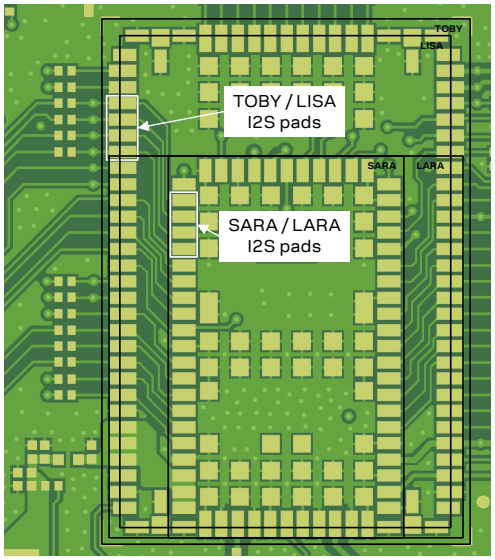

Figure 23: I2S interface pads for TOBY / LISA and SARA / LARA modules' I2S pins are positioned to facilitate routing

3.6.2.3 Enabling analog audio feature on supported modules

Analog audio capability can be made available by using an external audio codec connected to the digital audio interface of TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, SARA-G3, and LARA modules, providing digital / analog conversion and vice versa, as shown in Figure 22.

The I2C bus compatible interface of the module can control the external audio codec. A digital clock output is provided for the external audio codec host clock. For more details on external codec integration, see the module's system integration manual, I2S interface application circuits section.

3.7 General Purpose Input/Output (GPIO)

TOBY, LISA, SARA, and LARA modules provide different numbers of GPIO pins:

- TOBY-L1 modules provide 6 GPIOs (**GPIO1**-**GPIO6**), not supported by FW except for the "Wireless Wide Area Network status" indication configured on the **GPIO1**
- TOBY-L2 modules provide 14 GPIOs (**GPIO1**-**GPIO6**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**, **DTR**, **DSR**, **DCD**, **RI**), not supported by product versions "00", "01" and "60" except for the "Wireless Wide Area Network status" indication configured on the **GPIO1**
- TOBY-R2 modules provide 9 GPIOs (**GPIO1**-**GPIO5**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**)
- LISA-U2 modules provide 14 GPIOs (**GPIO1**-**GPIO14**)
- SARA-G3 modules provide 4 GPIOs (**GPIO1**-**GPIO4**), not supported by SARA-G300 / SARA-G310
- SARA-G4 modules provide 4 GPIOs (**GPIO1**-**GPIO4**)
- SARA-U2 modules provide 9 GPIOs (**GPIO1**-**4**, **SIM_DET**, **I2S_RXD**, **I2S_TXD**, **I2S_CLK**, **I2S_WA**)
- SARA-N3 modules provide 8 GPIOs (**GPIO1-GPIO5, RI, RTS, CTS**)
- SARA-R4 modules provide 6 GPIOs (**GPIO1**-**GPIO6**)
- SARA-R5 modules provide 8 GPIOs (**GPIO1-GPIO6, EXT_INT, SDIO_CMD**)
- LARA-R2 modules provide 9 GPIOs (**GPIO1**-**GPIO5**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**)
- LARA-R6 modules provide 9 GPIOs (**GPIO1**-**GPIO5**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**)

The same compatible external circuit can be implemented using the same function on the 1.8 V GPIOs provided by the modules.

For further details about the available GPIO functions / settings and application circuits, see the module's data sheet, system integration manual, and the AT commands manual.

The GPIO pins of TOBY / LISA share pads on the nested design application board, and the SARA / LARA pins are positioned to minimize routing effort.

3.8 Reserved pins (RSVD)

All the modules have pins reserved for future use, marked as **RSVD**:

- TOBY-L1: **RSVD** pins **16**, **17** and **49** must be connected to test points for diagnostic,
  All the other **RSVD** pins should be left unconnected.
- TOBY-L2: **RSVD** pin **6** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- TOBY-R2: **RSVD** pin **6** must be connected to GND,
  RSVD pins **18** and **19** must be connected to test points diagnostic,
  All the other **RSVD** pins should be left unconnected.
- LISA-U2: **RSVD** pin **5** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- SARA-G3: **RSVD** pin **33** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- SARA-G4: **RSVD** pin **33** can be connected to GND or left unconnected,
  All the other **RSVD** pins should be left unconnected.
- SARA-N3: **RSVD** pin **33** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- SARA-U2: **RSVD** pin 33 must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- SARA-R41: **RSVD** pin **33** can be connected to GND or left unconnected,
  All the other **RSVD** pins can be left unconnected.
- SARA-R42: **RSVD** pin **33** must be connected to a test point for direct accessibility (diagnostic),
  All the other **RSVD** pins can be left unconnected.
- SARA-R5: single **RSVD** pin which should be left unconnected.
- LARA-R2: **RSVD** pin **33** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- LARA-R6: **RSVD** pin **33** must be connected to a test point for direct accessibility (diagnostic),
  All the other **RSVD** pins should be left unconnected.

To accommodate different modules, for the **RSVD** pins that must be connected to GND, a 0 Ω shunt resistor can be used. Such resistor should be placed for modules requiring GND connection on their relevant pin and should be marked as do not place / do not mount otherwise. The resistor pads will also serve as test points in case of diagnostic access to **RSVD** pins.

4 Production guidelines

As described in Figure 2, a different stencil is needed for the production of TOBY, LISA, SARA, and LARA variants because the paste mask Gerber files are different for TOBY, LISA, SARA, and LARA (see section 4.1 to identify the different Gerber files within the delivered package).

Note that on this reference design a step stencil has been used, with the following different thicknesses:

- 150 µm stencil thickness for the USB connector and the TOBY / LISA / SARA / LARA modules
- 120 µm stencil thickness for any other component on the PCB

For more details on TOBY, LISA, SARA, and LARA handling and soldering on the nested design board, see the specific module's system integration manual.

4.1 Description of the delivered package

The TOBY / LISA / SARA / LARA Nested Design Reference Design package has three folders:

- **HS_Schematic** contains the hardware schematic (TO_R30_HS_271A00 file), which has all the necessary text comments explaining the different BoM mounting options for the different hardware release variants.
- **BM_Bom** contains the seven Bill of Materials variants (TO_R30_BM_271A**x**0 files, where "**x**" denotes the specific variant for the related module), available as mounting options on the same nested PCB, so that any TOBY-L1, TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, SARA-G3, SARA-R41, LARA-R2, or LARA-R6 module can be alternatively mounted on the same nested board with all the suitable components provided in the mounting options:
  - TO_R30_BM_271A**A**0 — LARA-R2 series BoM mounting variant "**A**"
  - TO_R30_BM_271A**B**0 — TOBY-L2 series BoM mounting variant "**B**"
  - TO_R30_BM_271A**C**0 — TOBY-R2 series BoM mounting variant "**C**"
  - TO_R30_BM_271A**D**0 — TOBY-L1 series BoM mounting variant "**D**"
  - TO_R30_BM_271A**E**0 — SARA-U2 series BoM mounting variant "**E**"
  - TO_R30_BM_271A**F**0 — SARA-G3 series BoM mounting variant "**F**"
  - TO_R30_BM_271A**G**0 — LISA-U2 series BoM mounting variant "**G**"
  - TO_R30_BM_271A**H**0 — SARA-R4a series BoM mounting variant "**H**"
  - TO_R30_BM_271A**J**0 — LARA-R6 series BoM mounting variant "**J**"
- **CS_Gerber** contains the Gerber files for the PCB production. Gerber files are the same for each variant, as the PCB is the same for all the hardware releases, but a different top-side stencil is needed for production because top-side soldering paste masks are different for TOBY, LISA, SARA, and LARA variants, as described in Figure 2. Paste mask Gerber files are the following:
  - 07_PASTEMASK_TOP_TOBY — Top-side paste mask for variants with TOBY
  - 07_PASTEMASK_TOP_LISA — Top-side paste mask for variants with LISA
  - 07_PASTEMASK_TOP_SARA — Top-side paste mask for variants with SARA
  - 07_PASTEMASK_TOP_LARA — Top-side paste mask for variants with LARA
  - 08_PASTEMASK_BOT — Bottom-side paste mask for all the variants

☞ It is possible to mount different modules with the same BOM, intended as any other part populated on the board except the module, due to the hardware / pin compatibility within TOBY-L2 series modules (BoM variant 'B'), LISA-U2 series modules (BoM variant 'G'), SARA-G3 series modules (BoM variant 'F'), SARA-U2 series modules (BoM variant 'E'), SARA-R41 series modules (BoM variant 'H'), and LARA-R2 series modules (BoM variant 'A'). The provided Bill of Materials files remark any further optimization reducing the number of components required for specific modules within each series.

5 Design checklist

5.1 Schematic checklist

The following are the most important points for a check of a nested design schematic:

☑ DC supply must provide a nominal voltage at **VCC** pins within the operating range limits:
- TOBY-L1: 3.40 V min / 4.50 V max
- TOBY-L2: 3.40 V min / 4.35 V max
- TOBY-R2: 3.30 V min / 4.40 V max
- LISA-U2: 3.30 V min / 4.40 V max
- SARA-G3: 3.35 V min / 4.50 V max
- SARA-G4: 3.40 V min / 4.20 V max
- SARA-N3: 3.20 V min / 4.20 V max
- SARA-U2: 3.30 V min / 4.40 V max
- SARA-R4: 3.20 V min / 4.20 V max
- SARA-R5: 3.30 V min / 4.40 V max
- LARA-R2 : 3.30 V min / 4.40 V max
- LARA-R6 : 3.30 V min / 4.50 V max

☑ DC supply must be capable of supporting both the highest peak and the highest averaged VCC current consumption values in connected mode, as specified in the module's data sheet:
- Considerable max average current for modules supporting LTE FDD full-duplex and/or 3G radio access technology
- Considerable max current pulses for modules supporting 2G radio access technology

☑ **VCC** voltage profile must be clean, with very low ripple/noise, providing the suggested parts to filter EMI, in particular if the application device integrates an internal antenna:
- 100 nF bypass capacitor, for any module
- 10 nF bypass capacitor for any module
- 68 pF or 56 pF bypass capacitor, with SRF ~800/900 MHz, for any module
- 15 pF bypass capacitor with SRF ~1800/1900 MHz, for any module
- 8.2 pF bypass capacitor, with SRF ~2600 MHz, for modules supporting bands in this high frequency range (as LTE band 7, 38, 40, 41)
- 330 µF bypass capacitor, with very low ESR for modules supporting 2G, LTE-TDD, or LTE half duplex
- Series ferrite bead for GHz band noise, for LISA-U2, SARA-U2, SARA-R4, LARA-R6 modules

☑ The **VCC** and/or the **PWR_ON** and/or the **RESET_N** circuits must be capable to generate appropriate module's power-on events as summarized in Table 3

☑ The **PWR_ON / PWR_CTL** line should be driven by an open-drain/collector, with pull-up necessity as following:
- TOBY-L1: Provide external 100k pull-up to **V_BCKP** or **VCC**
- TOBY-L2: Do not provide external pull-up, as there is an internal 50 k pull-up to **VCC**
- TOBY-R2: Do not provide external pull-up, as there is an internal 10 k pull-up to **V_BCKP**
- LISA-U2: Provide external 100k pull-up to **V_BCKP** or **VCC**
- SARA-G3: Provide external 100k pull-up to **V_BCKP** or **VCC**
- SARA-G4: Do not provide external pull-up, as there is an internal 28 k pull-up
- SARA-N3: Do not provide external pull-up, as there is an internal 90 k pull-up
- SARA-U2: Provide external 100k pull-up to **V_BCKP** or **VCC**
- SARA-R4: Do not provide external pull-up, as there is an internal 200 k pull-up
- SARA-R5: Do not provide external pull-up, as there is an internal 10 k pull-up
- LARA-R2: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**
- LARA-R6: Do not provide external pull-up, as there is an internal 200 k pull-up

☑ The **RESET_N** line should be driven by an open drain/collector, without external pull-up necessity:

- TOBY-L1: Do not provide external pull-up, as there is an internal 10 k pull-up to **V_BCKP**
- TOBY-L2: Do not provide external pull-up, as there is an internal 50 k pull-up to **VCC**
- TOBY-R2: Do not provide external pull-up, as there is an internal 10 k pull-up to **V_BCKP**
- LISA-U2: Do not provide external pull-up, as there is an internal 10 k pull-up to **V_BCKP**
- SARA-G3: Do not provide external pull-up, as there is an internal 10 k pull-up to **V_INT**
- SARA-G4: **RESET_N** pin not available
- SARA-U2: Do not provide external pull-up, as there is an internal 10 k pull-up to **V_BCKP**
- SARA-N3: Do not provide external pull-up, as there is an internal 70 k pull-up
- SARA-R41: Do not provide external pull-up, as there is an internal 37 k pull-up
- SARA-R42: **RESET_N** pin not available
- SARA-R5: Do not provide external pull-up, as there is an internal active pull-up
- LARA-R2: Do not provide external pull-up, as there is an internal 10 k pull-up to **V_BCKP**
- LARA-R6: Do not provide external pull-up, as there is an internal 37 k pull-up

☑ The **PWR_ON** and **RESET_N** lines must be accessible (by test-point for LGA modules), for diagnostic / FW update purposes

☑ The **V_INT** output should be monitored by the application to sense the end of the switch-off routine of the module, for a safe **VCC** supply removal (see section 3.2.2 and Figure 8)

☑ The **V_INT** must be accessible (by test-point for LGA modules) for diagnostic purposes

☑ The selected antennas must provide optimal return loss / V.S.W.R. figure and optimal efficiency figure over all the required operating frequencies, considering that there are some differences in the operating bands frequency ranges of the modules as summarized in Figure 10

☑ Consider antenna ESD immunity precautions, as an external high pass filter, consisting of a series 15 pF capacitor and a shunt 39 nH coil (see section 3.3, and in particular the circuits illustrated in Figure 11, Figure 12 and Figure 13), may be necessary according to application requirements:

- TOBY-L1: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- TOBY-L2: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- TOBY-R2: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- LISA-U2: Add an high pass filter (series 15 pF and shunt 39 nH) on **ANT** line, if the application requires reaching 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2, but mind that this will prevent the usage of the antenna detection functionally
- SARA-G3: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- SARA-G4: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- SARA-N3: Add an high pass filter (series 15 pF and shunt 39 nH) on **ANT** line, to improve ESD immunity, and note that this will not prevent the antenna detection functionality
- SARA-R4: Add an high pass filter (series 15 pF and shunt 39 nH) on **ANT** line, to improve ESD immunity, and note that this will not prevent the antenna detection functionality
- SARA-R5: Add an high pass filter (series 15 pF and shunt 39 nH) on **ANT** line, to improve ESD immunity, and note that this will not prevent the antenna detection functionality
- SARA-U2: Add an high pass filter (series 15 pF and shunt 39 nH) on **ANT** line to improve ESD immunity, and note that this will not prevent the antenna detection functionality
- LARA-R2: Add an high pass filter (series 15 pF and shunt 39 nH) on **ANT2** line, to improve ESD immunity, and note that this will not prevent antenna detection functionality
- LARA-R6: Add a high pass filter (series 15 pF and shunt 39 nH) on **ANT2** line, to improve ESD immunity, and note that this will not prevent antenna detection functionality

☑ Consider antenna detection function, as an appropriate external antenna circuit (see section 3.3, and in particular the circuits illustrated in Figure 11, Figure 12, and Figure 13), may be necessary if the antenna detection functionality is required by the application:

- TOBY-L1: Antenna detection is not supported
- TOBY-L2: Implement the external antenna circuit illustrated in Figure 11 if the antenna detection functionality (not supported by '00', '01', '60' versions) is required by the application
- TOBY-R2: Implement the external antenna circuit illustrated in Figure 11 if the antenna detection functionality is required by the application
- LISA-U2: The modules are equipped with an internal circuit for antenna detection support: external components on the board are not necessary to provide the functionality
- SARA-G3: Implement the external antenna circuit illustrated in Figure 13 if the antenna detection functionality (not supported by SARA-G300 / G310) is required by the application
- SARA-G4: Implement the external antenna circuit illustrated in Figure 13 if the antenna detection functionality is required by the application
- SARA-N3: Implement the external antenna circuit illustrated in Figure 13 if the antenna detection functionality is required by the application
- SARA-U2: Implement the external antenna circuit illustrated in Figure 13 if the antenna detection functionality is required by the application
- SARA-R4: Implement the external antenna circuit illustrated in Figure 13 if the antenna detection functionality is required by the application
- SARA-R5: Implement the external antenna circuit illustrated in Figure 13 if the antenna detection functionality is required by the application
- LARA-R2: Implement the external antenna circuit illustrated in Figure 14 if the antenna detection functionality is required by the application
- LARA-R6: Implement the external antenna circuit illustrated in Figure 14 if the antenna detection functionality is required by the application

☑ The UART must be accessible (by test-point for LGA modules) for diagnostic and FW update purposes

- TOBY-L1: Provide accessible test-points directly connected to **RSVD** pin 16 and **RSVD** pin 17 for diagnostic purposes, even if the UART is not supported
- TOBY-L2: Provide accessible test-points directly connected to all the UART pins (**TXD**, **RXD**, **RTS**, **CTS**, **DTR**, **DSR**, **DCD**, **RI**) for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor, even if the UART is not supported by "00" modules' product versions
- TOBY-R2: Provide accessible test-points directly connected to the **TXD** and **RXD** pins and to the **DTR** and **DCD** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- LISA-U2: Provide accessible test-points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- SARA-G3: Provide accessible test-points directly connected to the **TXD_AUX** and **RXD_AUX** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- SARA-G4: Provide accessible test-points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- SARA-N3: Provide accessible test points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor

- SARA-U2: Provide accessible test-points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- SARA-R4: Provide accessible test-points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- SARA-R5: Provide accessible test-points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- LARA-R2: Provide accessible test-points directly connected to the **TXD** and **RXD** pins and to the **DTR** and **DCD** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor
- LARA-R6: Provide accessible test points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, provide 0 Ω series jumpers to detach each line from the DTE application processor

☑ The UART interface of all the modules is not tolerant up to 3.0 V, so that the following topics must be considered for the connection to a 3.0 V DTE application processor:

- it is recommended to use appropriate unidirectional push-pull voltage translators (as the TI SN74AVC4T774, providing partial power-down feature so that the external DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply of the module), using **V_INT** as supply source for the translators on the module side
- alternatively, the voltage scaling from 3.0 V to 1.8 V can be implemented by a voltage divider, but consider the different values of the pull-ups integrated at each UART input of the modules (see Table 2) for the correct selection of the voltage divider resistance values
- mind that any DTE signal connected to the module must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence, at least until the activation of the **V_INT** supply output of the module, to avoid latch-up of circuits and allow a proper boot

☑ The USB interface has to be designed with controlled impedance on the **USB_D+** / **USB_D-** signal lines, and the USB interface lines have to be connected on the nested board as in Figure 20 and Figure 21

☑ The USB must be accessible (by test-point for LGA modules) for diagnostic and FW update purposes:

- Provide accessible test-points directly connected to the **VUSB_DET** / **USB_5V0**, **USB_3V3**, **USB_D+** and **USB_D-** pins, in particular provide a 0 Ω series jumpers to detach each line from the DTE application processor

☑ The HSIC must be designed with controlled impedance on the **HSIC_DATA** / **HSIC_STRB** lines

☑ The HSIC must be accessible (e.g. by test-point for LGA modules) for diagnostic purposes, if the interface is not connected to the host application processor

☑ The I2C interface of all the modules except SARA-G3 series is not tolerant up to 3.0 V: the connection to the related I2C pins of a u-blox 3.0 V GNSS receiver must be implemented using a proper I2C-bus bidirectional voltage translator with proper pull-up resistors (as the TI TCA9406, providing the partial power down feature, so that the GNSS 3.0 V supply can be ramped up before the **V_INT** supply which has to be used as supply source for the translator on the module side)

☑ The SIM interface must provide bypass capacitor of about 22 pF to 47 pF, very close to each pad of the SIM connector, to prevent RF coupling especially in case of internal antenna

☑ ESD protections with low capacitance and series resistance must be added on SIM lines if accessible

☑ Analog audio interface must provide the suggested passive EMI / EMC filtering parts, and the analog audio functionality should be provided on the nested board as shown in Figure 22

☑ The I2S and GPIO3 pins of SARA-G3 modules "02" product versions onwards must be accessible (e.g. by test-point for LGA modules) for diagnostic purposes, providing 0 Ω series jumpers to detach each line if connected to the application circuit

☑ All the pins reserved for future use (**RSVD**) must be left unconnected, except:

- TOBY-L1: **RSVD** pins 16, 17 and 49 should be connected to a test point for direct accessibility
- TOBY-L2: **RSVD** pin 6 must be connected to GND
- TOBY-R2: **RSVD** pin 6 must be connected to GND
  RSVD pins 18 and 19 should be connected to a test point for direct accessibility
- LISA-U2: **RSVD** pin 5 must be connected to GND
- SARA-G3: **RSVD** pin 33 must be connected to GND
- SARA-G4: **RSVD** pin 33 can either be connected to GND or left unconnected
- SARA-N3: **RSVD** pin 33 must be connected to GND
- SARA-U2: **RSVD** pin 33 must be connected to GND
- SARA-R41: **RSVD** pin 33 can be connected to GND or left unconnected
- SARA-R42: **RSVD** pin 33 must be connected to a test point for direct accessibility
- SARA-R5: **RSVD** pin 2 must be connected to GND
- LARA-R2: **RSVD** pin 33 must be connected to GND
- LARA-R6: **RSVD** pin 33 must be connected to a test point for direct accessibility

5.2 Layout checklist

The following are the most important points for a check of a nested design layout:

☑ The modules' footprint on the top layer of the nested board has to be designed as implemented in the available 01_TOP.art gerber file, with Non Solder Mask Defined (NSMD) pad type as implemented in the available 05_SOLDERMASK_TOP.art gerber file

☑ Depending on the module mounted on the nested board, four different paste masks must be used for the top layer. The paste masks have to be designed as in the available gerber files:

- 07_PASTE_TOP_TOBY.art top-side paste mask for variants with TOBY
- 07_PASTE_TOP_LISA.art top-side paste mask for variants with LISA
- 07_PASTE_TOP_SARA.art top-side paste mask for variants with SARA
- 07_PASTE_TOP_LARA.art top-side paste mask for variants with LARA

☑ The **VCC** lines have to be designed with bypass capacitors in the pF range and the additional series ferrite bead placed as close as possible to the modules' **VCC** pins, in particular if the application device integrates an internal antenna (see Figure 4)

☑ The antennas RF transmission lines have to be designed with nominal characteristic impedance as close as possible to 50 Ω (see Figure 11, Figure 12 and Figure 13)

☑ The RF and analog parts / circuits must be clearly separated from any possible source of radiated energy (primarily USB signals, high-speed digital lines, and SIM signals), and must be clearly separated from any sensitive part / circuit which may be affected by EMI.

☑ The antennas terminations have to provide optimal return loss (or V.S.W.R.) figure and optimal efficiency figure over all the required operating frequencies, considering that there are some differences in the operating bands frequency ranges of the modules as summarized in Figure 10

☑ The recommendations of the antenna producer for correct antenna installation and deployment must be strictly followed (PCB layout and matching circuitry)

☑ High and similar efficiency must be provided for both the primary and the secondary antenna

☑ High isolation between the primary and the secondary antenna must be provided

☑ Low Envelope Correlation Coefficient between primary and secondary antennas must be provided: the 3D antenna radiation patterns should have radiation lobes in different directions

- ☑ The maximum gain of the transmitting antenna must not exceed the regulatory limits specified in related countries, as the limits defined for FCC United States regulatory conformity, for ISED Canada regulatory conformity, for RED Europe regulatory conformity, for GITEKI Japan regulatory conformity, etc. (see related remarks in the modules' system integration manual and/or related certificate of conformity).
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part (see Figure 21)
- ☑ **HSIC_DATA** / **HSIC_STRB** traces should meet the characteristic impedance requirement (50 Ω nominal)
- ☑ Optimal ground connection has to be provided using as many vias as possible to connect the ground planes on multilayer PCB, adding additional vias along the RF lines, the high-speed data lines and in general at the edges of each ground area
- ☑ One layer of the application board should be implemented as ground plane, and all the layers should be filled with ground plane as much as possible, connecting each ground area with complete via stack down to the main ground layer of the board.

Appendix

A Glossary

Abbreviation	Definition
2G	2nd Generation Cellular Technology (GSM, GPRS, EGPRS)
3G	3rd Generation Cellular Technology (UMTS, HSDPA, HSUPA, or HSPA)
3GPP	3rd Generation Partnership Project
8-PSK	8 Phase-Shift Keying modulation
16QAM	16-state Quadrature Amplitude Modulation
ADC	Analog to Digital Converter
AT	AT Command Interpreter Software Subsystem
AUX	Auxiliary
BAW	Bulk Acoustic Wave
BJT	Bipolar Junction Transistor
BoM	Bill of Material
Cat	Category
CDMA	Code-Division Multiple Access
CE	European Conformity
CLK	Clock
CS	Circuito Stampato (Printed Circuit Board)
CTS	Clear To Send
DAC	Digital to Analog Converter
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DDC	Display Data Channel interface (I2C)
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution (EGPRS)
eDRX	Extended Discontinuous Reception
EGPRS	Enhanced General Packet Radio Service (EDGE)
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FD	Full-Duplex
FDD	Frequency Division Duplex
FW	Firmware
GLONASS	(Russian) GLObal Navigation Satellite System
GMSK	Gaussian Minimum-Shift Keying modulation

Abbreviation	Definition
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Services
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HD	Half-Duplex
HR	Hardware Release
HS	Hardware Schematic
HSIC	High Speed Inter Chip
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HW	Hardware
I2C	Inter-Integrated Circuit interface
I2S	Inter IC Sound interface
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IMEI	International Mobile Equipment Identity
IPC	Inter-Processor Communication
ISED	Innovation, Science and Economic Development Canada
LCC	Leadless Chip Carrier
LDO	Low-Dropout
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPWA	Low Power Wide Area
LTE	Long Term Evolution
MIC	Microphone
MIMO	Multiple In Multiple Out
N/A	Not Applicable
NB-IoT	Narrowband Internet of Things (LTE Category NB1 / LTE Category NB2)
NSMD	Non Solder Mask Defined
OTA	Over The Air
PA	Power Amplifier
PCB	Printed Circuit Board
PMU	Power Management Unit
PSM	Power Saving Mode
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RI	Ring Indicator
RSE	Radiated Spurious Emission
RSVD	Reserved
RTC	Real Time Clock
Rx	Receive

Abbreviation	Definition
SAR	Specific Absorption Rate
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input Output
SIM	Subscriber Identification Module
SMD	Solder Mask Defined
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
SPK	Speaker
SRF	Self Resonant Frequency
TBD	To Be Defined
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
THT	Through-Hole Technology
TI	Texas Instruments
TP	Test-Point
TRP	Total Radiated Power
TTFF	Time-To-First-Fix
Tx	Transmit
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
VCC	Voltage Collector Collector (power supply)
VoLTE	Voice over LTE
VSWR	Voltage Standing Wave Ratio
WA	Word Alignment
WCDMA	Wideband Code-Division Multiple Access
Wi-Fi	Wireless Local Area Network (IEEE 802.11 short range radio technology)
VSWR	Voltage Standing Wave Ratio

Table 5: Explanation of the abbreviations and terms used

Related documentation

[1] u-blox TOBY-L1 series data sheet, UBX-13000868
[2] u-blox TOBY-L2 series data sheet, UBX-13004573
[3] u-blox TOBY-R2 series data sheet, UBX-16005785
[4] u-blox LISA-U2 series data sheet, UBX-13001734
[5] u-blox SARA-G3 series data sheet, UBX-13000993
[6] u-blox SARA-G4 series data sheet, UBX-18006165
[7] u-blox SARA-U2 series data sheet, UBX-13005287
[8] u-blox SARA-N3 series data sheet, UBX-18066692
[9] u-blox LARA-R2 series data sheet, UBX-16005783
[10] u-blox LARA-R6 series data sheet, UBX-21004391
[11] u-blox SARA-R4 series data sheet, UBX-16024152
[12] u-blox SARA-R5 series data sheet, UBX-19016638
[13] u-blox TOBY-L1 / MPCI-L1 series system integration manual, UBX-13001482
[14] u-blox TOBY-L2 / MPCI-L2 series system integration manual, UBX-13004618
[15] u-blox TOBY-R2 series system integration manual, UBX-16010572
[16] u-blox LISA-U2 series system integration manual, UBX-13001118
[17] u-blox SARA-N2 / N3 series system integration manual, UBX-17005143
[18] u-blox SARA-G4 series system integration manual, UBX-18046432
[19] u-blox SARA-G3 / SARA-U2 series system integration manual, UBX-13000995
[20] u-blox LARA-R2 series system integration manual, UBX-16010573
[21] u-blox LARA-R6 series system integration manual, UBX-21010011
[22] u-blox SARA-R4 series system integration manual, UBX-16029218
[23] u-blox SARA-R5 series system integration manual, UBX-19041356
[24] u-blox TOBY-L1 / MPCI-L1 series AT commands manual, UBX-13002211
[25] u-blox SARA-R4 series AT commands manual, UBX-17003787
[26] u-blox AT commands manual, UBX-13002752
[27] u-blox SARA-N2 / SARA-N3 series AT commands manual, UBX-16014887
[28] u-blox SARA-R5 series AT commands manual, UBX-19047455
[29] u-blox LARA-R6 AT commands manual, UBX-21046719
[30] u-blox SARA modules migration guidelines application note, UBX-19045981
[31] u-blox LARA modules migration guidelines application note, UBX-21010015

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	13-Apr-2016	sses	Initial release
R02	11-Jul-2016	sses	Document applicability updated to TOBY-R200, TOBY-R201, TOBY-R202, LARA-R204 and LARA-R211 as TOBY-R2 series and LARA-R2 series modules
R03	23-Sep-2016	sses	Document status updated to Advance Information Updated Power on, GPIO and Clock Output interface description
R04	05-May-2017	sses	Document applicability extended to SARA-R41 series modules Updated Power on and Power off description Other minor corrections and update
R05	30-Aug-2022	psca / sses	Document applicability extended to LARA-R6 series modules, with notes also for SARA-G4, SARA-N3, SARA-R42, SARA-R5 series modules. Editorial changes implemented, corrections and clarifications added.

Contact

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