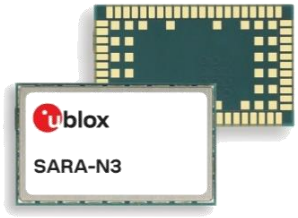
# SARA-N3 series

## Multi-band NB-IoT (LTE Cat NB2) modules

Data sheet




**Abstract**

Technical data sheet describing SARA-N3 Narrowband Internet of Things cellular modules. These modules are a complete and cost-efficient solution offering multi-band data transmission for the Internet of Things technology in a compact form factor.

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# Document information

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| **Functional sample** | Draft | For functional testing. Revised and supplementary data will be published later. |
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| **Mass production / End of life** | Production information | Final product specification. |

This document applies to the following products:

| Product name | Type number | Modem version | Application version | PCN reference | Product status |
|---|---|---|---|---|---|
| SARA-N310 | SARA-N310-00X-00 | 18.13 | A01.01 | UBX-21017614 | End of life |
| | SARA-N310-00X-01 | 18.13 | A01.02 | UBX-21039338 | End of life |
| | SARA-N310-00X-02 | 18.13 | A01.03 | UBX-22003602 | End of life |
| | SARA-N310-00X-03 | 18.13 | A01.04 | UBX-22023924 | Mass production |

# Contents

# 1 Functional description

## 1.1 Overview

The SARA-N3 series are multi-band NB-IoT (LTE Cat NB2) modules supporting a preliminary set of features based on 3GPP release 14 in the miniature SARA LGA form factor (16.0 x 26.0 mm, 96-pin).

The modules offer multi-band NB-IoT data communication enabling multi-regional coverage over an extended operating temperature range of –40 °C to +85 °C, with extremely low power consumption.

The SARA-N3 series modules introduce several new functionalities for NB-IoT products, including features like TCP, DTLS, LwM2M, MQTT, MQTT-SN, SSL/TLS, HTTP(S). They enable a diverse and broad set of new IoT applications and simplify customer migration to NB-IoT from other cellular or unlicensed technologies. u-blox nested design eases migration between other u-blox LTE, 3G and 2G modules, while enabling future-proof, seamless scalability across technologies.

Critical firmware updates can be delivered over the air using the u-blox uFOTA client / server solution with LwM2M, which is a more lightweight solution compared to OMA-DM.

The SARA-N3 series modules are the optimal choice for IoT devices designed to operate in locations with a very limited coverage and requiring low energy consumption to permit a very long operating life of the primary batteries. Examples of applications include and are not limited to smart grids, smart metering, telematics, street lighting, environmental monitoring and control, security and asset tracking.

## 1.2 Product features

| Module | Region | Cellular RAT | | | Interfaces | | | | | | Features | | | | | | | | | | | | Grade | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 3GPP release baseline | 3GPP LTE category | LTE FDD bands | UARTs | USB | DDC (I2C) | USIM | ADCs | GPIOs | Antenna supervisor | Power Save Mode | eDRX | Bluetooth 4.2 (BR/EDR and BLE) | Embedded TCP/UDP stack | Embedded CoAP, MQTT, MQTT-SN | Embedded HTTP, FTP, PPP, DNS | Embedded TLS, DTLS | Dual stack IPv4 / IPv6 | LwM2M Device Management | Last gasp | FW update over AT (FOAT) | FW update over the air (FOTA) | Standard | Professional | Automotive |
| **SARA-N310** | Global | 14 | NB2 | 3, 5, 8<br>20, 28<br>★ | ● | | ○ | ● | ● | ● | ● | ● | ● | ○ | ● | ● | ● | ● | ● | ● | ● | ● | ● | | ● | |

● = Supported ○ = Available in future FW ★ = Additional bands (1, 2, 4, 12, 13, 18, 19, 26, 66, 71, 85) available in future FW

**Table 1: SARA-N3 series main features summary**

## 1.3 Block diagram

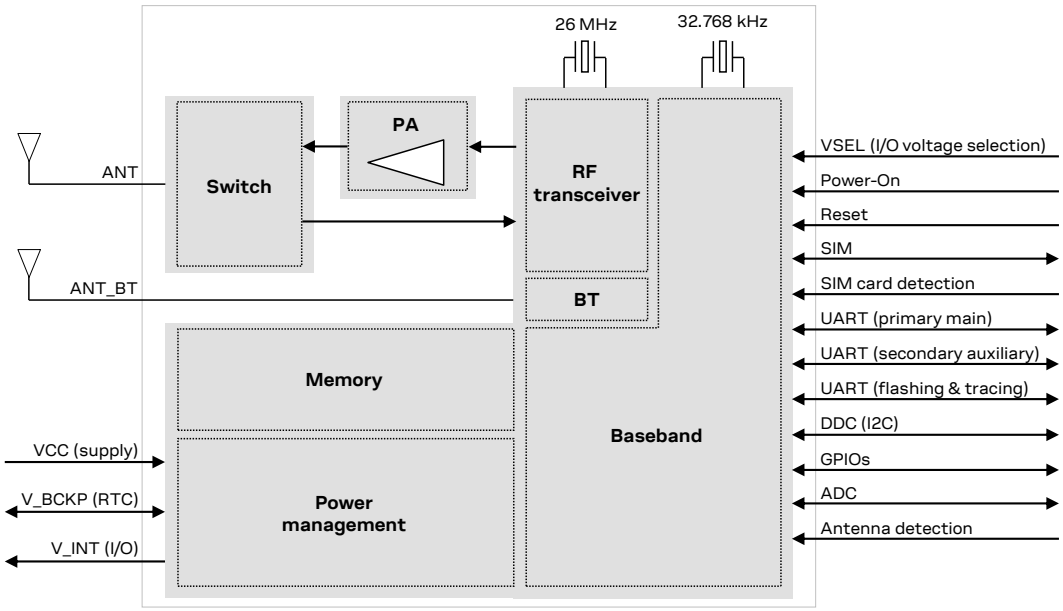


**Figure 1: SARA-N3 series block diagram**

The “00" product versions of SARA-N3 series modules do not support the following interfaces, which should not be driven by external devices:

- Bluetooth interface (ANT_BT)
- Secondary auxiliary serial interface (UART AUX)
- SPI interface
- DDC (I2C) interface

## 1.4 Product description

| Item | SARA-N310 [1] |
|---|---|
| Protocol stack | 3GPP release 14 [2] |
| Radio Access Technology | LTE category NB2 Half-Duplex |
| Operating bands | Band 3 (1800 MHz)<br>Band 5 (850 MHz)<br>Band 8 (900 MHz)<br>Band 20 (800 MHz)<br>Band 28 (700 MHz) |
| Deployment modes | In-Band<br>Guard-Band<br>Standalone |
| Power class | Class 3 (23 dBm) [3] |
| Sustained data rate | LTE category NB2:<br>Up to 140 kb/s UL<br>Up to 125 kb/s DL |

**Table 2: SARA-N3 series NB-IoT characteristics summary**

[1] Additional LTE bands (1, 2, 4, 12, 13, 18, 19, 26, 66, 71, 85) available in future FW versions
[2] Key subset of features
[3] Configurable to other power class by AT command

## 1.5 AT command support

The SARA-N3 series modules support AT commands according to the 3GPP standards, plus the u-blox AT command extensions.

☞ For the complete list of all supported AT commands and their syntax description, see the SARA-N2 / SARA-N3 series AT commands manual [1].

## 1.6 Supported features

Table 3 lists some of the features supported by SARA-N3 series modules.

| Feature | Description |
|---|---|
| Network indication | Pin configured to indicate the network status: registered home network, registered roaming, data call enabled, no service. The feature can be enabled through the +UGPIOC AT command. |
| Antenna detection | The **ANT_DET** pin provides antenna presence detection capability, evaluating the resistance from the **ANT** pin to GND by means of an external antenna detection circuit implemented on the application board. The feature can be enabled through the +UANTR AT command. |
| Jamming detection | Detects “artificial” interference that obscures the operator’s carriers providing access to the NB-IoT service and reports the start and stop of such conditions to the application processor (AP). The AP can react appropriately, e.g. by switching off the radio transceiver to reduce power consumption and monitoring the environment at constant periods. |
| Dual stack IPv4/IPv6 | Capability to move between IPv4 and IPv6, dual stack network infrastructures IPv4 and IPv6 addresses can be used. |
| TCP/UDP | Embedded TCP/IP and UDP/IP stack, to establish a transparent end-to-end communication through TCP or UDP sockets via serial interface. |
| DTLS (v1.2) | Embedded Datagram Transport Layer Security (DTLS) provides security for CoAP, LwM2M, MQTT-SN and UDP communications. |
| CoAP (RFC 7252 [5]) | Embedded Constrained Application Protocol (CoAP) datagram-based client/server application protocol designed to easily translate from HTTP for simplified integration with the web. |
| SSL/TLS (v1.0, v1.1, v1.2) | Transport Layer Security (TLS) provides security for HTTP, MQTT and TCP communications. |
| MQTT (v3.1.1) and MQTT-SN (v1.2) | Embedded Message Queuing Telemetry Transport (MQTT) and MQTT for Sensor Networks (MQTT-SN) publish-subscribe messaging protocols designed for lightweight M2M communications over TCP (MQTT) or over UDP (MQTT-SN). These allow one-to-one, one-to-many and many-to-one communications over a TCP or UDP connection. |
| FTP | Embedded File Transfer Protocol functionality is supported via AT commands. |
| HTTP and HTTPS (v1.0, v1.1) | Embedded Hyper-Text Transfer Protocol as well as embedded Secure Hyper-Text Transfer Protocol functionalities are supported via AT commands. |
| Release Assistance | The Release Assistance feature introduced in 3GPP release 13 allows the module to request for the RRC connection to be dropped as soon as the message has been received by the network. This feature allows a reduction in the module power consumption. |
| Firmware update Over AT commands (FOAT) | Firmware module update over AT command interface.<br>The feature can be enabled and configured through the +UFWUPD AT command. |
| u-blox Firmware update Over The Air (uFOTA) | u-blox firmware update over the LTE air interface client/server solution using LwM2M (v1.0). |
| RPM | The Radio Policy Manager (RPM) feature allows a reduction in the module power consumption as the module does not retry an unnecessary service request. |
| Last gasp | In case of power supply outage (i.e. main supply interruption, battery removal, battery voltage below a certain threshold) the cellular module can be configured to send an alarm notification to a remote entity.<br>The feature can be enabled and configured through the +ULGASP AT command. |

| Feature | Description |
|---|---|
| Power Saving Mode (PSM) | The Power Saving Mode (PSM) feature, defined in 3GPP release 13, allows further reduction of the module current consumption maximizing the amount of time a device can remain in extremely low power deep sleep mode during periods of data inactivity. It can be activated and configured by the +CPSMS AT command. |
| Deep-sleep mode | The SARA-N3 series modules enters in extremely low power deep sleep mode whenever possible, using the internal 32 kHz clock to maintaining an extremely low current consumption. This optimizes the lifetime of the battery pack used to supply the system. |
| eDRX | Extended mode DRX, based on 3GPP release 13, reduces the amount of signaling overhead decreasing the frequency of scheduled measurements and/or transmissions performed by the module. This in turn leads to a reduction in the module power consumption while maintaining a perpetual connection with the base station. |
| Coverage Enhancement | Coverage Enhancements modes introduced in 3GPP release 13 for the NB-IoT system improve the cell signal penetration allowing a 20 dB coverage enhancement over standard GSM systems. |
| Mobility Enhancement | Mobility Enhancements introduced in 3GPP release 14 for the NB-IoT system. |

**Table 3: Main features of SARA-N3 series modules**

# 2 Interfaces

## 2.1 Power management

### 2.1.1 Module supply input (VCC)

SARA-N3 series modules must be supplied through the three **VCC** pins by a proper DC power supply. Voltage must be stable during module operation, taking into account that the current drawn through the **VCC** pins may vary significantly based on the power consumption profile of the NB-IoT system.

### 2.1.2 RTC supply input/output (V_BCKP)

**V_BCKP** is the Real Time Clock (RTC) supply of SARA-N3 series modules. When **VCC** voltage is within the valid operating range, the internal Power Management Unit (PMU) supplies the RTC and the same supply voltage is available on the **V_BCKP** pin. If the **VCC** voltage is under the minimum operating limit (e.g. during not powered mode), the RTC can be externally supplied through the **V_BCKP** pin.

### 2.1.3 Digital I/O interfaces supply output (V_INT)

SARA-N3 series modules provide supply rail output on the **V_INT** pin, which is used internally to supply the digital I/O interfaces of the modules (UART interfaces, I2C interface, and GPIO pins).

The **V_INT** operating voltage can be selected using the **VSEL** input pin:

- If the **VSEL** input pin is connected to GND, the digital I/O interfaces operate at 1.8 V
- If the **VSEL** input pin is left unconnected, the digital I/O interfaces operate at 2.8 V

The **V_INT** supply output is internally generated when the module is switched on, outside PSM.

☞ If the **VSEL** input pin is left unconnected, the **VCC** voltage shall be inside normal operating range to let the digital I/O interfaces work correctly (see section 4.2.2).

☞ Provide a test point connected to the **V_INT** pin for diagnostic purpose.

## 2.2 Antenna

### 2.2.1 Cellular antenna RF interface (ANT)

The **ANT** pin has an impedance of 50 Ω and provides the LTE Cat NB2 (NB-IoT) RF interface of the SARA-N3 series modules, to be connected to a proper external cellular antenna.

### 2.2.2 Bluetooth antenna RF interface (ANT_BT)

The **ANT_BT** pin has an impedance of 50 Ω and provides the Bluetooth RF antenna interface of the SARA-N3 series modules.

☞ The Bluetooth functionality is not supported by "00" product versions of SARA-N3 series modules. The **ANT_BT** pin can be left unconnected or it can also be connected to GND.

### 2.2.3 Antenna detection (ANT_DET)

The **ANT_DET** pin is an Analog to Digital Converter (ADC) input to sense the antenna presence (as optional feature), evaluating the resistance from the **ANT** pin to GND by means of an external antenna detection circuit implemented on the application board.

## 2.3 System functions

### 2.3.1 Module power-on

When the SARA-N3 series modules are in the not-powered mode (i.e. switched off with the **VCC** module supply not applied), the switch on routine of the module can be triggered by:

- Applying a **VCC** supply within the normal operating range of the module (see section 4.2.2), and then forcing a low level on the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see section 4.2.5).
- Alternately, the **RESET_N** pin can be held low during the **VCC** rising edge, so that the module switches on by releasing the **RESET_N** pin when the **VCC** voltage stabilizes at its nominal value within the normal range.

When the SARA-N3 series modules are in power off mode (i.e. switched off, with valid **VCC** supply applied), the switch on routine of the module can be triggered by:

- Forcing a low level on the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see section 4.2.5).

When the SARA-N3 series modules are in the deep sleep mode (i.e. in Power Saving Mode defined in 3GPP Rel. 13, with valid **VCC** supply applied), the wake-up routine of the module can be triggered by:

- Forcing a low level on the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see section 4.2.5).

☞ Provide a test point connected to the **PWR_ON** pin for diagnostic purposes.

### 2.3.2 Module power-off

SARA-N3 series modules can be properly switched off, with storage of current parameter settings in the module's non-volatile memory and clean network detach, by:

- AT+CPWROFF command (see the SARA-N2 / SARA-N3 series AT commands manual [1]).
- Low level on the **PWR_ON** input pin, i.e. forcing the pin (normally high due to internal pull-up) to a low level for a valid time period (see section 4.2.5).

An abrupt under-voltage shutdown occurs on SARA-N3 series modules when the **VCC** supply drops below the extended operating range minimum limit (see section 4.2.2), but in this case it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory as well as a clean network detach.

### 2.3.3 Module reset

SARA-N3 series modules can be properly reset (rebooted), with storage of current parameter settings in the module's non-volatile memory and clean network detach, by:

- AT+CFUN command (see the SARA-N2 / SARA-N3 series AT commands manual [1]), triggering an "internal" or "software" reset / re-boot of the module

An abrupt hardware reset occurs on SARA-N3 series modules when a low voltage level is applied at the **RESET_N** input pin, which is normally set high by an internal pull-up, for a valid time period (see the section 4.2.6), triggering an "external" or "hardware" reset / re-boot of the module. In this case it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory as well as a clean network detach. The **RESET_N** line is intended to be driven by open drain, open collector or contact switch.

☞ Provide a test point connected to the **RESET_N** pin for diagnostic purposes.

### 2.3.4 Digital I/O interfaces voltage selection (VSEL)

The digital I/O interfaces of SARA-N3 series modules (the UARTs, I2C, and GPIOs pins) operate at the **V_INT** voltage, which can be set to 1.8 V or 2.8 V using the **VSEL** input:

- If the **VSEL** input pin is connected to GND, the digital I/O interfaces operate at 1.8 V
- If the **VSEL** input pin is left unconnected, the digital I/O interfaces operate at 2.8 V

The operating voltage cannot be changed dynamically: the **VSEL** input pin configuration has to be set before the boot of SARA-N3 series modules and then it cannot be changed after switched on.

☞ If the **VSEL** input pin is left unconnected, the **VCC** voltage shall be inside normal operating range to let the digital I/O interfaces work correctly (see section 4.2.2).

## 2.4 SIM interface

☞ SIM card detection is not supported by "00" product version.

SARA-N3 series modules include a SIM interface on the **VSIM**, **SIM_IO**, **SIM_CLK** and **SIM_RST** pins, which can operate at 1.8 V and/or 3.0 V voltage (**VSIM** domain). Activation and deactivation of the SIM interface, with automatic 1.8 V / 3.0 V voltage switch according to the voltage class of the external SIM connected to the module are implemented according to the ISO-IEC 7816-3 specifications.

SARA-N3 series modules include also the **GPIO5** pin to detect the presence of an external SIM card, as intended to be appropriately connected to the mechanical switch of an external SIM card holder. The **GPIO5** pin operates at the **V_INT** voltage, which can be set to 1.8 V or 2.8 V using the **VSEL** input.

☞ If a 3.0 V SIM is used, the **VCC** voltage shall be inside normal operating range to let the SIM interface work correctly (see section 4.2.2).

## 2.5 Serial interfaces

SARA-N3 series modules include the following serial interfaces:

- UART: main primary serial interface, for communication with host processor (2.5.1)
- UART AUX: auxiliary secondary serial interface for communication with host processor (2.5.2)
- UART FT: additional serial interface for Firmware update and Tracing (2.5.3)
- DDC: I2C-bus compatible interface for communication with I2C devices and sensors (2.5.4)

### 2.5.1 Main primary serial interface (UART)

SARA-N3 series modules include a main primary unbalanced asynchronous serial interface (UART) available for communication with an application host processor:

- AT communication
- FW upgrades by means of the FOAT feature

The characteristics of the main primary serial interface (UART) are:

- Complete serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [4]
- CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V / 2.8 V for high data bit or OFF state): the internal power domain for the UART Interface is **V_INT**, with voltage value set according to external **VSEL** pin configuration
- Data lines (**RXD** as output, **TXD** as input), hardware flow control lines (**CTS** as output, **RTS** as input), modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output)
- Hardware flow control disabled by default
- UART works in low power idle mode, supporting 4800, 9600, 19200, 38400, 57600 b/s baud-rates
- One-shot automatic baud rate detection enabled by default
- 8N1 default frame format

☞ The functionality of **DTR**, **DSR** and **DCD** lines is not supported by "00" product versions.

The UART interface settings can be suitably configured by AT commands (for more details, see the SARA-N2 / SARA-N3 series AT commands manual [1]).

### 2.5.2 Secondary auxiliary serial interface (UART AUX)

☞ The secondary auxiliary serial interface (UART AUX) is not supported by "00" product versions.

SARA-N3 series modules include a secondary auxiliary unbalanced asynchronous serial interface (UART AUX) available for communication with an application host processor

The characteristics of the secondary auxiliary serial interface (UART AUX) are:

- 2-wire serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [4]
- CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V / 2.8 V for high data bit or OFF state): the internal power domain for the UART AUX Interface is **V_INT**, with voltage value set according to external **VSEL** pin configuration
- Data lines (**RXD_AUX** as output, **TXD_AUX** as input)

The UART AUX interface settings can be suitably configured by AT commands (for more details, see the SARA-N2 / SARA-N3 series AT commands manual [1]).

### 2.5.3 Additional serial interface for FW upgrade and Tracing (UART FT)

SARA-N3 series modules include an additional unbalanced asynchronous serial interface available for Firmware upgrade and Tracing (UART FT):

- FW upgrades by means of the u-blox EasyFlash tool
- Diagnostic purpose

The characteristics of the additional serial interface for Firmware upgrade and Tracing (UART FT) are:

- 2-wire serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [4]
- CMOS compatible signal levels (0 V for low data bit or ON state and 1.8 V / 2.8 V for high data bit or OFF state): the internal power domain for the UART FT interface is **V_INT**, with voltage value set according to external **VSEL** pin configuration
- Data lines (**RXD_FT** as output, **TXD_FT** as input)

☞ For diagnostic and FW update purposes, connect test points to the **RXD_FT** and **TXD_FT** pins.

☞ The trace diagnostic log is temporarily stopped when the module is in deep-sleep mode.

### 2.5.4 DDC (I2C) interface

☞ The DDC (I2C) interface is not supported by "00" product versions.

SARA-N3 series modules include an I2C-bus compatible DDC interface (**SDA** data input/output, **SCL** clock output) available for the communication with external I2C devices and sensors.

The internal power domain for the I2C-bus compatible DDC interface is **V_INT**, with 1.8 V / 2.8 V voltage value set according to external **VSEL** pin configuration.

## 2.6 ADC

SARA-N3 series modules include two Analog-to-Digital Converter input pins, **ANT_DET** and **ADC1**, configurable via a dedicated AT command (for further details, see the SARA-N2 / SARA-N3 series AT commands manual [1]).

## 2.7 GPIO

SARA-N3 series modules include General Purpose Input/Output pins that can be configured via u-blox AT commands (for further details, see the SARA-N2 / SARA-N3 series AT commands manual [1]).

The internal power domain for the GPIO pins is **V_INT**, with 1.8 V / 2.8 V voltage value set according to external **VSEL** pin configuration.

Table 4 summarizes the custom functions available on the GPIO pins of SARA-N3 series modules.

| Function | Description | Default GPIO | Configurable GPIOs |
|---|---|---|---|
| Network status indication | Output to indicate the network status: registered home network, registered roaming, data transmission, no service | -- | GPIO1, GPIO2, CTS |
| Module status indication | Output indicating module status: power-off, sleep or deep-sleep mode versus idle, active or connected mode | -- | GPIO4 |
| Last gasp | Input to trigger last gasp execution | -- | GPIO3 |
| SIM card detection | Input to sense external SIM card physical presence | GPIO5[4] | GPIO5[4] |
| HW flow control (RTS) | UART request to send input | RTS | RTS |
| HW flow control (CTS) | UART clear to send output | CTS | CTS |
| Ring indication | UART ring indicator output | RI | RI |
| General purpose input | Input to sense high or low digital level | -- | GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, RI, RTS, CTS |
| General purpose output | Output to set high or low digital level | -- | GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, RI, RTS, CTS |
| Pin disabled | Output tri-stated, with an internal active pull-down enabled | GPIO1, GPIO2, GPIO3, GPIO4, GPIO5[5] | GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, RI, RTS, CTS |

**Table 4: GPIO custom functions configuration**

[4] Not supported by “00” product version.
[5] On “00” product version only.

# 3 Pin definition

## 3.1 Pin assignment

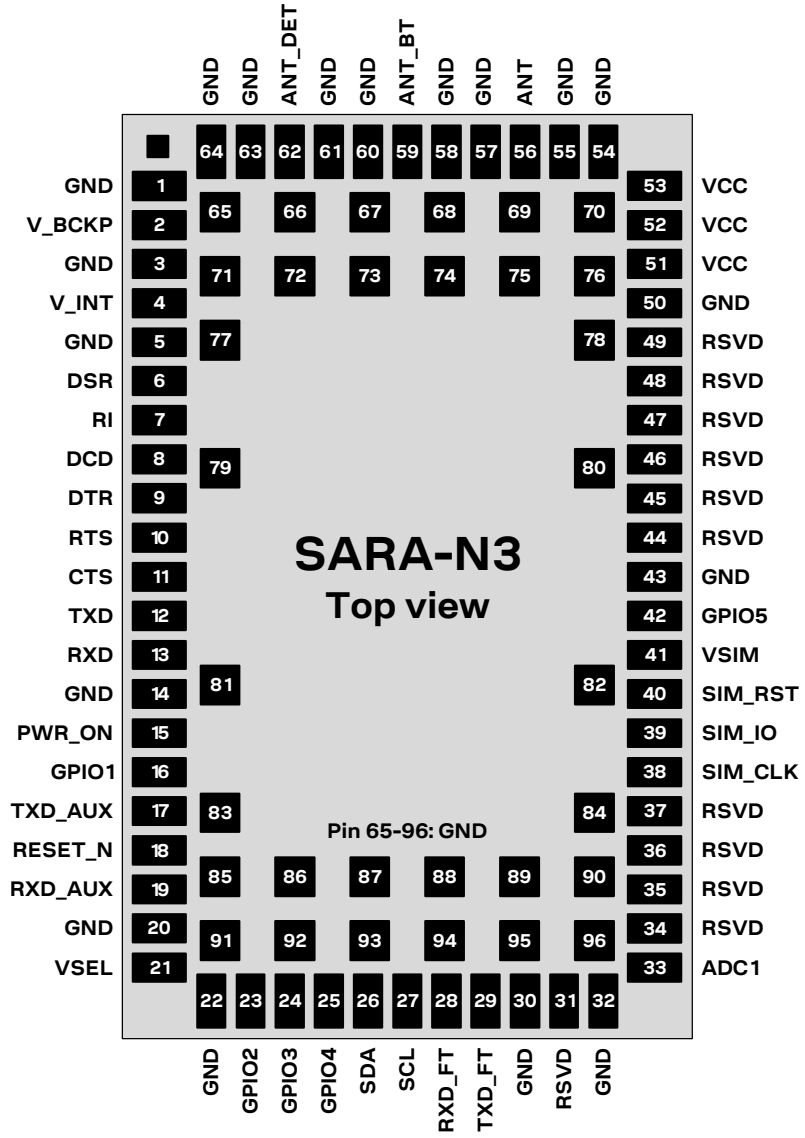


**Figure 2: SARA-N3 series modules pin assignment**

| No | Name | Power domain | I/O | Description | Remarks |
|---|---|---|---|---|---|
| 1 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 2 | V_BCKP | - | I/O | Real Time Clock supply input/output | See section 4.2.2 for detailed electrical specs. |
| 3 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 4 | V_INT | - | O | Digital I/O interfaces supply output | V_INT supply output, rail of the Digital I/O interfaces, generated by the module when switched-on.<br>V_INT = 1.8 V (typical), if VSEL pin is connected to GND.<br>V_INT = 2.8 V (typical), if VSEL pin is unconnected.<br>Test-point recommended for diagnostic purpose.<br>See section 4.2.2 for detailed electrical characteristics. |
| 5 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 6 | DSR | GDI | O | UART data set ready | DSR not supported by '00' product versions.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical specs. |
| 7 | RI | GDI | O | UART ring indicator | Circuit 125 (RI) in ITU-T V.24.<br>PU/PD class b.<br>Configurable as GPIO, as described in section 2.7.<br>See section 4.2.8 for detailed electrical specs. |
| 8 | DCD | GDI | O | UART data carrier detect | DCD not supported by '00' product versions.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical specs. |
| 9 | DTR | GDI | I | UART data terminal ready | DTR not supported by '00' product versions.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical specs. |
| 10 | RTS | GDI | I | UART request to send | Circuit 105 (RTS) in ITU-T V.24.<br>Internal active pull-up enabled, if HW flow control enabled.<br>PU/PD class b.<br>Configurable as GPIO, as described in section 2.7.<br>See section 4.2.8 for detailed electrical characteristics. |
| 11 | CTS | GDI | O | UART clear to send | Circuit 106 (CTS) in ITU-T V.24.<br>PU/PD class b.<br>Configurable as GPIO, as described in section 2.7.<br>See section 4.2.8 for detailed electrical characteristics. |
| 12 | TXD | GDI | I | UART data input | Circuit 103 (TxD) in ITU-T V.24.<br>Internal active pull-up enabled.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 13 | RXD | GDI | O | UART data output | Circuit 104 (RxD) in ITU-T V.24.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 14 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 15 | PWR_ON | PWR_ON | N/A | Power-on input | Internal active pull-up enabled.<br>See section 4.2.5 for detailed electrical characteristics.<br>For diagnostic purposes, connect a test point to this pin |
| 16 | GPIO1 | GDI | I/O | GPIO | GPIO configurable as described in section 2.7.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 17 | TXD_AUX | GDI | I | UART AUX data input | TXD_AUX not supported by '00' product versions.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 18 | RESET_N | RESET_N | I | External reset input | Internal active pull-up enabled.<br>See section 4.2.6 for detailed electrical characteristics.<br>For diagnostic purposes, connect a test point to this pin. |

| No | Name | Power domain | I/O | Description | Remarks |
|---|---|---|---|---|---|
| 19 | RXD_AUX | GDI | O | UART AUX data output | RXD_AUX not supported by '00' product versions.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 20 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 21 | VSEL | - | I | Voltage selection | Input to select the operating voltage of the digital I/O interfaces of the module (UART, I2C and GPIO pins).<br>V_INT = 1.8 V (typical), if VSEL pin is connected to GND.<br>V_INT = 2.8 V (typical), if VSEL pin is unconnected. |
| 22 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 23 | GPIO2 | GDI | I/O | GPIO | GPIO configurable as described in section 2.7.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 24 | GPIO3 | GDI | I/O | GPIO | GPIO configurable as described in section 2.7.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 25 | GPIO4 | GDI | I/O | GPIO | GPIO configurable as described in section 2.7.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 26 | SDA | GDI | I/O | I2C bus data line | I2C interface not supported by '00' product versions.<br>Internal pull-up to V_INT.<br>See section 4.2.8 for detailed electrical characteristics. |
| 27 | SCL | GDI | O | I2C bus clock line | I2C interface not supported by '00' product versions.<br>Internal pull-up to V_INT.<br>See section 4.2.8 for detailed electrical characteristics. |
| 28 | RXD_FT | GDI | O | UART FT data output | For firmware update and trace log diagnostic purposes, connect a test point to this pin.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 29 | TXD_FT | GDI | I | UART FT data input | For firmware update and trace log diagnostic purposes, connect a test point to this pin.<br>Internal active pull-up enabled.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |
| 30 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 31 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 32 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 33 | ADC1 | ADC | I | ADC input | 10-bit Analog to Digital Converter input.<br>This pin can be externally connected to GND, if the ADC function is not needed in the application.<br>See section 4.2.9 for detailed electrical characteristics. |
| 34 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 35 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 36 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 37 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 38 | SIM_CLK | SIM | O | SIM clock | See section 4.2.7 for detailed electrical specs. |
| 39 | SIM_IO | SIM | I/O | SIM data | See section 4.2.7 for detailed electrical specs. |
| 40 | SIM_RST | SIM | O | SIM reset | See section 4.2.7 for detailed electrical specs. |
| 41 | VSIM | - | O | SIM supply output | See section 4.2.2 for detailed electrical characteristics. |
| 42 | GPIO5 | GDI | I/O | GPIO | GPIO configurable as described in section 2.7.<br>PU/PD class b.<br>See section 4.2.8 for detailed electrical characteristics. |

| No | Name | Power domain | I/O | Description | Remarks |
|---|---|---|---|---|---|
| 43 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 44 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 45 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 46 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 47 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 48 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 49 | RSVD | - | N/A | RESERVED pin | Leave unconnected. |
| 50 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 51 | VCC | VCC | I | Module supply input | All VCC pins must be connected to external supply.<br>See 4.2.2 and 4.2.3 for detailed electrical characteristics. |
| 52 | VCC | VCC | I | Module supply input | All VCC pins must be connected to external supply.<br>See 4.2.2 and 4.2.3 for detailed electrical characteristics. |
| 53 | VCC | VCC | I | Module supply input | All VCC pins must be connected to external supply.<br>See 4.2.2 and 4.2.3 for detailed electrical characteristics. |
| 54 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 55 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 56 | ANT | - | I/O | RF cellular antenna | 50 Ω nominal characteristic impedance.<br>See section 4.2.4 for detailed RF characteristics. |
| 57 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 58 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 59 | ANT_BT | - | I/O | RF BT antenna | Bluetooth not supported by '00' product versions.<br>50 Ω nominal characteristic impedance. |
| 60 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 61 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 62 | ANT_DET | ADC | I | Antenna detection | 10-bit Analog to Digital Converter input.<br>See section 4.2.8 for detailed electrical characteristics. |
| 63 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 64 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |
| 65-96 | GND | GND | N/A | Ground | All GND pads must be connected to ground. |

**Table 5: SARA-N3 series modules pin-out**

☞ For an explanation of abbreviations and terms used, see appendix A.

# 4 Electrical specification

⚠ Stressing the device above one or more of the ratings listed in the Absolute maximum rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating conditions section (section 4.2) of the specification should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ Electrical characteristics are defined according to the verification on a representative number of samples or according to the simulation.

☞ Where application information is given, it is advisory only and does not form part of the specification.

## 4.1 Absolute maximum rating

☞ Limiting values given below are in accordance with Absolute Maximum Rating System (IEC 134).

| Symbol | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Module supply voltage | Input DC voltage at VCC pin | –0.2 | 4.2 | V |
| V_BCKP | RTC supply voltage | Input DC voltage at V_BCKP pin | –0.2 | 3.4 | V |
| GDI | Generic digital interfaces | Input DC voltage at Generic digital interfaces pins | –0.2 | 3.0 | V |
| PWR_ON | Power-on signal | Input DC voltage at PWR_ON pin | –0.2 | 1.3 | V |
| RESET_N | External reset signal | Input DC voltage at RESET_N pin | –0.2 | 1.3 | V |
| ADC | ADC signal | Input DC voltage at ANT_DET and ADC pins | –0.2 | 2.0 | V |

**Table 6: Absolute maximum ratings**

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification given in table above must be limited to values within the specified boundaries by using appropriate protection devices.

### 4.1.1 Maximum ESD

| Parameter | Min | Typical | Max | Unit | Remarks |
|---|---|---|---|---|---|
| ESD sensitivity for all pins | | | 1000 | V | Human Body Model according to JS-001-2017 |
| | | | 500 | V | Charged Device Model according to JS-002-2018 |

**Table 7: Maximum ESD ratings**

⚠ u-blox cellular modules are Electrostatic Sensitive Devices and require special precautions when handling. See section 7.4 for ESD handling instructions.

## 4.2 Operating conditions

Unless otherwise indicated, all operating condition specifications are at an ambient temperature of +25 °C.

Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.

### 4.2.1 Operating temperature range

| Parameter | Min | Typical | Max | Unit | Remarks |
|---|---|---|---|---|---|
| Normal operating temperature | –20 | +25 | +85 | °C | Operating within 3GPP / ETSI specifications |
| Extended operating temperature | –40 | | +85 | °C | Operating with possible slight deviation in RF performance outside normal operating range |

**Table 8: Environmental conditions**

### 4.2.2 Supply/power pins

| Pin name | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| VCC | Module supply normal operating input voltage[6] | 3.2 | 3.8 | 4.2 | V |
| | Module supply extended operating input voltage[7] | 2.6 | | 4.2 | V |
| V_BCKP | Real Time Clock supply input voltage | 1.6 | | 3.3 | V |

**Table 9: Input characteristics of Supply/Power pins**

| Pin name | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| VSIM | SIM interface supply output voltage, external SIM = 1.8V type | | 1.8 | | V |
| | SIM interface supply output voltage, external SIM = 3.0V type | | 3.0 | | V |
| V_BCKP | Real Time Clock supply output voltage | | 2.5 | | V |
| | Real Time Clock supply output current capability | | | 0.5 | mA |
| V_INT | Digital I/O interfaces supply output voltage, VSEL = GND | | 1.8 | | V |
| | Digital I/O interfaces supply output voltage, VSEL unconnected | | 2.8 | | V |
| | Digital I/O interfaces supply output current capability | | | 70 | mA |

**Table 10: Output characteristics of Supply/Power pins**

[6] Operating within 3GPP / ETSI specifications.
[7] Operating with possible slight deviation in RF performance outside normal operating range. The input voltage has to be above the extended operating range minimum limit to switch-on the module and to avoid possible switch-off of the module.

### 4.2.3 Current consumption

| Mode | Condition | Tx power | Min | Typ[8] | Max | Unit |
|---|---|---|---|---|---|---|
| Power-off mode | Average current value (power-off mode) | -- | | 3 | | µA |
| PSM deep-sleep mode | Average current value (PSM deep-sleep mode) | -- | | 3 | | µA |
| Cyclic deep-sleep / active mode (+NVSETPM: 9) | Average current value (rock bottom) | -- | | 3 | | µA |
| | Average current value (DRX = 2.56 s, PTW = 20.48 s, eDRX = 655.36 s) | -- | | 50 | | µA |
| Cyclic sleep / active mode (+NVSETPM: 9) | Average current value (rock bottom) | -- | | 100 | | µA |
| | Average current value (DRX = 2.56 s, PTW = 20.48 s, eDRX = 81.92 s) | -- | | 230 | | µA |
| | Average current value (DRX = 2.56 s, PTW = 5.12 s, eDRX = 20.48 s) | -- | | 230 | | µA |
| | Average current value (DRX = 2.56 s, no eDRX) | -- | | 0.6 | | mA |
| | Average current value (DRX = 1.28 s, no eDRX) | -- | | 1.0 | | mA |
| Cyclic idle / active mode (+NVSETPM : 1) | Average current value (rock bottom) | -- | | 0.8 | | mA |
| | Average current value (DRX = 2.56 s, no eDRX) | -- | | 1.2 | | mA |
| | Average current value (DRX = 1.28 s, no eDRX) | -- | | 1.5 | | mA |
| Active mode (+NVSETPM: 0) | Average current value (DRX 1.28 s) | -- | | 20 | | mA |
| | Average current value (airplane mode, +CFUN: 0) | -- | | 11 | | mA |
| Connected mode | Average current value (Rx mode) | -- | | 23 | | mA |
| | Average current value (Tx mode) | –40 dBm | | 45 | | mA |
| | | –10 dBm | | 55 | | mA |
| | | 0 dBm | | 75 | | mA |
| | | 8 dBm | | 120 | | mA |
| | | 14 dBm | | 155 | | mA |
| | | 20 dBm | | 235 | | mA |
| | | Maximum | | 275 | | mA |

**Table 11: VCC current consumption [9]**

[8] Typical values with a matched antenna.
[9] Module current consumption through **VCC** input pins, in the listed modes/conditions.

### 4.2.4 RF characteristics

| Parameter | | Min | Max | Unit | Remarks |
|---|---|---|---|---|---|
| Frequency range Band 3 | Uplink | 1710 | 1785 | MHz | Module transmit |
| | Downlink | 1805 | 1880 | MHz | Module receive |
| Frequency range Band 5 | Uplink | 824 | 849 | MHz | Module transmit |
| | Downlink | 869 | 894 | MHz | Module receive |
| Frequency range Band 8 | Uplink | 880 | 915 | MHz | Module transmit |
| | Downlink | 925 | 960 | MHz | Module receive |
| Frequency range Band 20 | Uplink | 832 | 862 | MHz | Module transmit |
| | Downlink | 791 | 821 | MHz | Module receive |
| Frequency range Band 28 | Uplink | 703 | 748 | MHz | Module transmit |
| | Downlink | 758 | 803 | MHz | Module receive |

**Table 12: Operating RF frequency bands**

| Parameter | Min. | Typical | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Receiver input sensitivity | | –140 | | dBm | Maximum possible repetitions |

**Table 13: Receiver sensitivity performance**

### 4.2.5 PWR_ON pin

| Parameter | Min. | Typical | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Internal supply for PWR_ON Input Signal | | 1.1 | | V | Internal supply rail |
| Low-level input | 0.0 | | 0.2 | V | |
| High-level input | 0.9 | | 1.1 | V | |
| Pull-up resistance | | 90 | | kΩ | Internal active pull-up |
| PWR_ON low-level time | 1 | | 2.5 | s | Low time to trigger module switch-on |
| | 1 | | 2.5 | s | Low time to trigger module wake-up from PSM |
| | 2.5 | | | s | Low time to trigger module switch-off |

**Table 14: PWR_ON pin characteristics**

### 4.2.6 RESET_N pin

| Parameter | Min. | Typical | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Internal supply for RESET_N Input Signal | | 1.1 | | V | Internal supply rail |
| Low-level input | 0.0 | | 0.2 | V | |
| High-level input | 0.9 | | 1.1 | V | |
| Pull-up resistance | | 70 | | kΩ | Internal active pull-up |
| RESET_N low-level time | 1 | | | s | Low time to trigger module reset (re-boot) |

**Table 15: RESET_N pin characteristics**

### 4.2.7 SIM interface pins

| Parameter | Min. | Typical | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Internal supply domain for SIM interface | | 1.8 | | V | VSIM, with external 1.8 V SIM type |
| | | 3.0 | | V | VSIM, with external 3.0 V SIM type |
| Low-level input | 0.0 | | 0.3*VSIM | V | |
| High-level input | 0.7*VSIM | | VSIM | V | |
| Low-level output | | 0.0 | | V | |
| High-level output | | VSIM | | V | |
| Internal pull-up on SIM_IO | | 4.7 | | kΩ | Internal pull-up to VSIM |
| Clock frequency on SIM_CLK | | 3 | | MHz | |

**Table 16: SIM pins characteristics**

### 4.2.8 Generic Digital Interface pins

| Parameter | Min. | Typical | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Internal supply domain for Generic Digital Interfaces | | 1.8 | | V | V_INT, with VSEL connected to GND |
| | | 2.8 | | V | V_INT, with VSEL unconnected |
| Low-level input | 0.0 | | 0.3*V_INT | V | |
| High-level input | 0.7*V_INT | | V_INT | V | |
| Low-level output | | 0.0 | | V | |
| High-level output | | V_INT | | V | |
| Output driver strength | | | 3 | mA | |
| Internal Pull-up / Pull-down | | 41 | | kΩ | PU/PD class a |
| | | 171 | | kΩ | PU/PD class b |

**Table 17: Generic Digital Interface (GDI) pins characteristics**

### 4.2.9 ADC pins

| Parameter | Min. | Typical | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Resolution | | 10 | | Bits | |
| Input voltage range | 0 | | 1.9 | V | |
| Input resistance | | 1 | | MΩ | With respect to GND |

**Table 18: Analog to Digital Converter input pins (ANT_DET, ADC1) characteristics**

# 5 Mechanical specifications

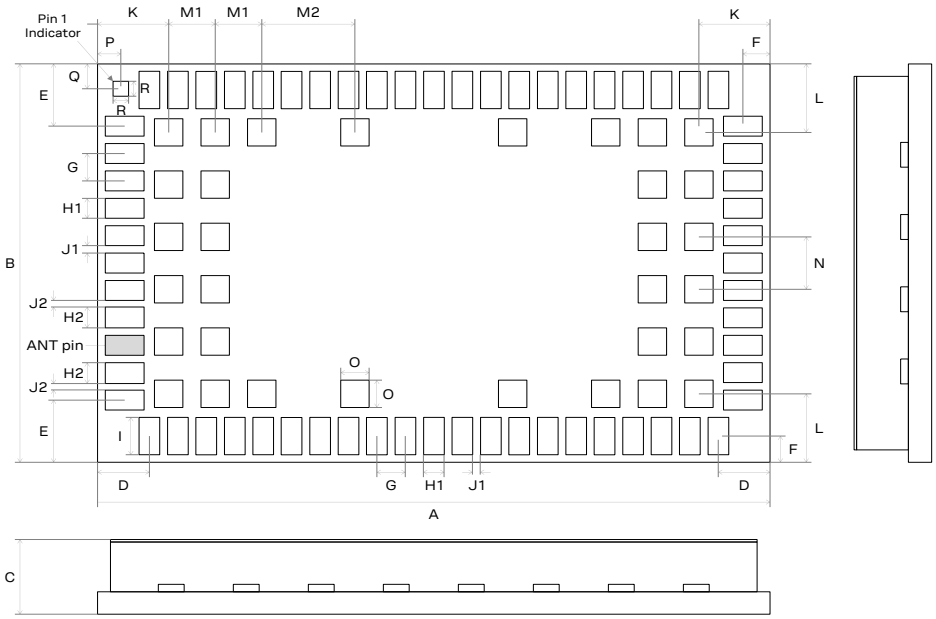


**Figure 3: SARA-N3 series dimensions (bottom and side views)**

| Parameter | Description | Typical | Tolerance | | |
|---|---|---|---|---|---|
| A | Module height [mm] | 26.0 | (1023.6 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| B | Module width [mm] | 16.0 | (629.9 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| C | Module thickness [mm] | 2.4 | (94.5 mil) | +0.25/-0.15 | (+9.8/-5.9 mil) |
| D | Horizontal edge to lateral pin pitch [mm] | 2.0 | (78.7 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| E | Vertical edge to lateral pin pitch [mm] | 2.5 | (98.4 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| F | Edge to lateral pin pitch [mm] | 1.05 | (41.3 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| G | Lateral pin to pin pitch [mm] | 1.1 | (43.3 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| H1 | Lateral pin height [mm] | 0.8 | (31.5 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| H2 | Lateral pin close to ANT height [mm] | 0.85 | (33.5 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| I | Lateral pin width [mm] | 1.5 | (59.1 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| J1 | Lateral pin to pin distance [mm] | 0.3 | (11.8 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| J2 | Lateral pin to pin close to ANT distance [mm] | 0.25 | (9.8 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| K | Horizontal edge to central pin pitch [mm] | 2.75 | (108.3 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| L | Vertical edge to central pin pitch [mm] | 2.75 | (108.3 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| M1 | Central pin to pin horizontal pitch [mm] | 1.8 | (70.9 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| M2 | Central pin to pin horizontal pitch [mm] | 3.6 | (141.7 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| N | Central pin to pin vertical pitch [mm] | 2.1 | (82.7 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| O | Central pin height and width [mm] | 1.1 | (43.3 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| P | Horizontal edge to pin 1 indicator pitch [mm] | 0.9 | (35.4 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| Q | Vertical edge to pin 1 indicator pitch [mm] | 1.0 | (39.4 mil) | +0.20/-0.20 | (+7.9/-7.9 mil) |
| R | Pin 1 indicator height and width [mm] | 0.6 | (23.6 mil) | +0.05/-0.05 | (+2.0/-2.0 mil) |
| Weight | Module weight [g] | < 3 | | | |

**Table 19: SARA-N3 series dimensions**

Module Height tolerance may be exceeded close to the corners of the PCB due to the cutting process. In the worst case, the height could be +0.40 mm more than the typical value.

For information regarding the footprint and paste mask recommended for the application board where the cellular module has to be mounted, see SARA-N2/N3 system integration manual [2].

# 6 Qualification and approvals

## 6.1 Reliability tests

Reliability tests for SARA-N3 series modules are executed according to u-blox qualification policy, based on AEC-Q104 standard.

## 6.2 Approvals

SARA-N3 series modules comply with the Directive 2011/65/EU of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

SARA-N3 series modules are RoHS 3 compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

Table 20 lists the main approvals for SARA-N3 series modules.

| Certification Scheme | SARA-N310 |
|---|---|
| CE (European Regulatory Conformity) | • |
| UKCA (Great Britain Regulatory Conformity) | • |
| NCC (Taiwan Regulatory Certificate) | • |
| ACMA RCM (Australian Regulatory Conformity) | • |
| NBTC (Thai Regulatory Certificate) | • |
| IMDA (Singaporean Regulatory Certificate) | • |
| ICASA (South African Regulatory Certificate) | • |
| ATEX / IECEx (Explosive Atmosphere Certificate) | • |
| GCF (Global Certification Forum Conformance) | • |
| Vodafone (Network Operator) | • |
| Deutsche Telekom (Network Operator) | • |

**Table 20: SARA-N3 series main certification approvals**

☞ For all the certificates of compliancy and for the complete list of approvals (including country and network operator approvals) of the SARA-N3 series modules, see our website (www.u-blox.com) or contact the u-blox office or sales representative nearest you.

### 6.2.1 ATEX certification

The SARA-N310 modules are certified as components intended for use in potentially explosive atmospheres compliant to the following standards:

- IEC 60079-0
- IEC 60079-11
- IEC 60079-26

SARA-N310 modules certification number according to the ATEX directive 2014/34/EU:

- SIQ 19 ATEX 305 U

SARA-N310 modules certification number according to the IECEx conformity assessment system:

- IECEx SIQ 19.0008U

According to the standards listed above, SARA-N310 modules are certified and marked as:

- Ⓔx II 1G Ex ia IIC Ga

According to the marking stated above, the modules are certified as electrical equipment of:

- Group “II”: intended for use in areas with explosive gas atmosphere other than mines susceptible to firedamp
- Category “1G”: intended for use in zone 0 hazardous areas, in which explosive atmospheres caused by mixtures of air and gases, vapors or mists are present continuously, for long periods or frequently
- Level of protection “ia”: intrinsically safe apparatus with very high level of protection, not capable of causing ignition in normal operation and with the application of one countable fault or a combination of any two countable fault plus those non-countable faults which give the most onerous condition
- Subdivision “IIC”: intended for use in areas where the nature of the explosive gas atmosphere is considered very dangerous based on the Maximum Experimental Safe Gap or the Minimum Ignition Current ratio of the explosive gas atmosphere in which the equipment may be installed (a typical gas is hydrogen), so that the modules are also suitable for applications intended for use in subdivision IIB (typical gas is ethylene) and subdivision IIA (a typical gas is propane)
- Equipment protection level “Ga”: equipment for explosive gas atmospheres, having a very high level of protection, which is not a source of ignition in normal operation, during expected malfunctions or during rare malfunctions

Section 4.2.1 defines the temperature range of use for SARA-N310 modules.

The RF radiating profile of SARA-N310 modules is compliant to all the applicable 3GPP / ETSI standards, with a maximum of 250 mW RF average power according to the LTE Cat NB2 Power Class stated in Table 2. Section 8.1 describes the nameplate of SARA-N310 modules (see Figure 6).

Table 21 lists the maximum input and equivalent intrinsically safe parameters for the SARA-N310 modules, that must be considered in the sub-division IIC, the sub-division IIB and the sub-division IIA.

| Parameter | SARA-N310 |
|---|---|
| Ui | 4.2 V |
| Ii | 0.5 A |
| Ci | 42.2 µF |
| Li | 11.4 µH |

**Table 21: Maximum input and equivalent intrinsically safe parameters for sub-division IIC, IIB and IIA**

☞ For more information about the integration of these modules in applications intended for use in potentially explosive atmospheres, see the SARA-N2/N3 series system integration manual [2].

# 7 Product handling

## 7.1 Packaging

SARA-N3 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox package information user guide [3].

**Figure 4: Reeled SARA-N3 series modules**

### 7.1.1 Reels

SARA-N3 series modules are deliverable in quantities of 250 pieces on a reel. SARA-N3 series modules are delivered using reel type B2 as described in the u-blox package information user guide [3].

| Parameter | Specification |
|---|---|
| Reel type | B2 |
| Delivery quantity | 250 |

**Table 22: Reel information for SARA-N3 series modules**

☞ Quantities of less than 250 pieces are also available. Contact u-blox for more information.

### 7.1.2 Tapes

Figure 5 and Table 23 specify the dimensions of the tapes for SARA-N3 series modules.

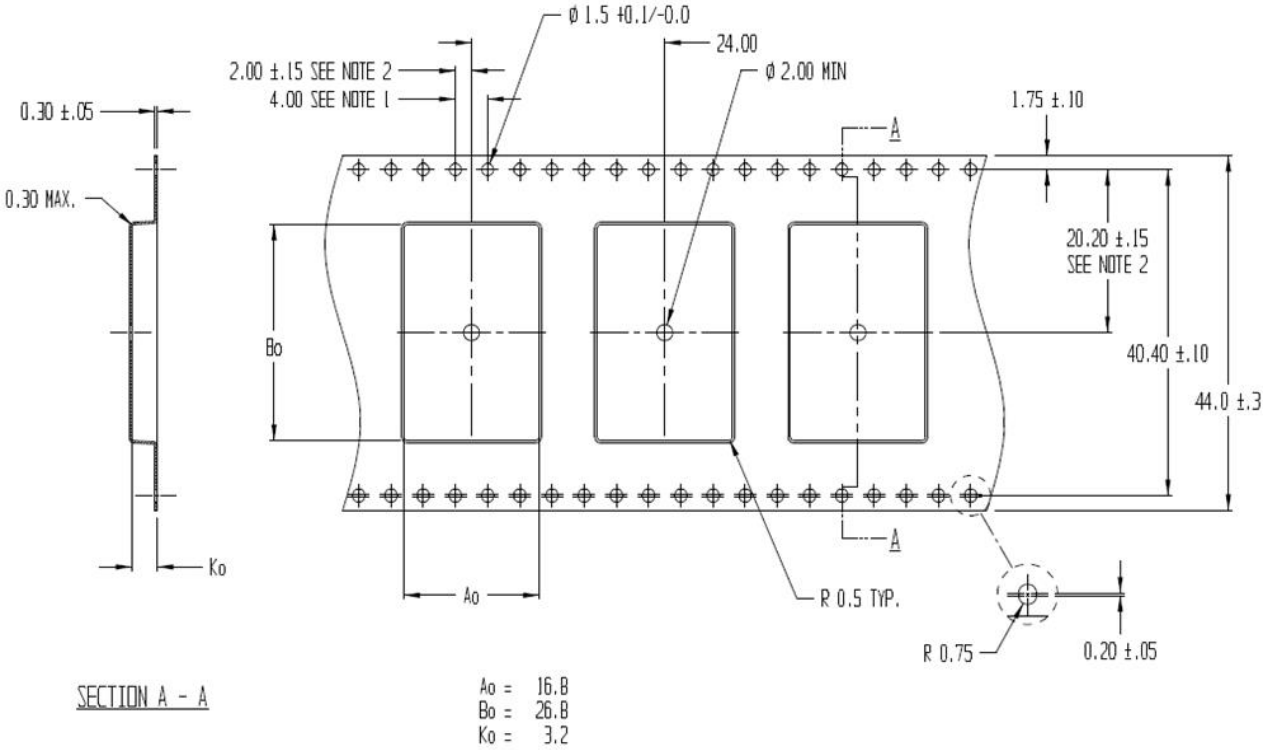


**Figure 5: Dimensions for SARA-N3 series on tape**

| Parameter | Typical value | Tolerance | Unit |
|---|---|---|---|
| $A_0$ | 16.8 | ± 0.2 | mm |
| $B_0$ | 26.8 | ± 0.2 | mm |
| $K_0$ | 3.2 | ± 0.2 | mm |

**Table 23: SARA-N3 series tape dimensions (mm)**

- Note 1: 10 sprocket hole pitch cumulative tolerance ± 0.2 mm.
- Note 2: Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
- Note 3: $A_0$ and $B_0$ are calculated on a plane at a distance “R” above the bottom of the pocket.

## 7.2 Moisture Sensitivity Levels

⚠ SARA-N3 series modules are Moisture Sensitive Devices (MSD) in accordance to IPC/JEDEC specification.

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. SARA-N3 series modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, labeling, storage and drying, see the u-blox package information user guide [3].

☞ For the MSL standard, see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org).

## 7.3 Reflow soldering

Reflow profiles are to be selected according to u-blox recommendations (see the SARA-N2/N3 series system integration manual [2]).

⚠ Failure to observe these recommendations can result in severe damage to the device!

## 7.4 ESD precautions

⚠ SARA-N3 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling SARA-N3 series modules without proper ESD protection may destroy or damage them permanently.

SARA-N3 series modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Table 7 reports the maximum ESD ratings of the SARA-N3 series modules.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates SARA-N3 series module.

ESD precautions should be implemented on the application board where the module is mounted, as described in the SARA-N2/N3 series system integration manual [2].

⚠ Failure to observe these recommendations can result in severe damage to the device!

# 8 Labeling and ordering information

## 8.1 Product labeling

The labels of SARA-N3 series modules include important product information, such as the u-blox logo, production lot, Pb-free marking, product type number, module IMEI number, regulatory certification info applicable for the specific module product version, and production country.

For example, Figure 6 illustrates the label of the SARA-N310 module. This includes the “Ex” marking of explosion protection with related group, category, type / level of protection, subdivision, and equipment protection level classification, the IECEx and ATEX certificate numbers, and the EU Notified Body identification number. To the right of the u-blox logo is the module production lot, Pb-free marking, product type number, module IMEI number, and production country.


**Figure 6: SARA-N310 module label**

## 8.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 24 below details these three different formats:

| Format | Structure |
|---|---|
| **Product name** | SARA-TGVV |
| **Ordering code** | SARA-TGVV-MMQ |
| **Type number** | SARA-TGVV-MMQ-XX |

**Table 24: Product code formats**

Table 25 explains the parts of the product code.

| Code | Meaning | Example |
|---|---|---|
| TG | Platform (technology and generation):<br>• Dominant technology: G: GSM; U: HSUPA; C: CDMA 1xRTT; N: NB-IoT; R: LTE low data rate (Cat 1 and below); L: LTE high data rate (Cat 3 and above)<br>• Generation within the technology: 1…9 | N3 |
| VV | Variant function set based on the same platform: 00…99 | 00 |
| MM | Major product version: 00…99 | 00 |
| Q | Product grade:<br>• A = automotive<br>• B = professional<br>• C = standard<br>• X = ATEX certified | B |
| XX | Minor product version (not relevant for certification) | 00 |

**Table 25: Part identification code**

## 8.3 Ordering codes

| Ordering No. | Product |
|---|---|
| SARA-N310-00X | LTE Cat NB2 multi-band module, designed for global use<br>16.0 x 26.0 x 2.4 mm, 250 pieces/reel |

**Table 26: Product ordering codes**

☞ Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs), see our website.

# Appendix

# A Glossary

| Abbreviation | Definition |
|---|---|
| 3GPP | 3rd Generation Partnership Project |
| ACMA | Australian Communications and Media Authority |
| ADC | Analog to Digital Converter |
| APAC | Asia-Pacific |
| ATEX | EU Explosive Atmosphere Directive |
| Cat | Category |
| CDMA | Code-Division Multiple Access |
| CE | Certification Mark for compliance in the European Economic Area |
| CLK | Clock |
| CoAP | Constrained Application Protocol |
| CTS | Clear To Send |
| DC | Direct Current |
| DDC | Display Data Channel |
| DL | Down Link (Reception) |
| DRX | Discontinuous Reception |
| DTLS | Datagram Transport Layer Security |
| eDRX | Extended Discontinuous Reception |
| ERS | External Reset Input Signal |
| ESD | Electrostatic Discharge |
| ETSI | European Telecommunications Standards Institute |
| FOAT | Firmware (update) Over AT commands |
| FOTA | Firmware (update) Over-The-Air |
| FTP | File Transfer Protocol |
| FW | Firmware |
| GDI | Generic Digital Interface |
| GND | Ground |
| GPIO | General Purpose Input/Output |
| GSM | Global System for Mobile communications |
| HSUPA | High Speed Uplink Packet Access |
| HTTP | HyperText Transfer Protocol |
| HW | Hardware |
| I/O | Input/Output |
| I2C | Inter-Integrated Circuit |
| ICASA | Independent Communications Authority of South Africa |
| IEC | International Electrotechnical Commission |
| IECEx | IEC system for certification to standards relating to equipment for use in Explosive atmospheres |
| IMDA | Infocomm Media Development Authority (Singapore) |
| IMEI | International Mobile Equipment Identity |
| ISO | International Organization for Standardization |
| LGA | Land Grid Array |
| LPWA | Low-Power Wide-Area |
| LTE | Long-Term Evolution |
| LwM2M | Lightweight Machine-to-Machine protocol |
| M2M | Machine to Machine |
| MCS | Modulation Coding Scheme |
| MSD | Moisture Sensitive Device |
| MSL | Moisture Sensitivity Level |
| MQTT | Message Queuing Telemetry Transport |
| N/A | Not Applicable |

| Abbreviation | Definition |
|---|---|
| NCC | National Communications Commission (Taiwan) |
| NBTC | National Broadcasting and Telecommunications Commission (Thailand) |
| PCB | Printed Circuit Board |
| PCN | Product Change Notification |
| PSM | Power Saving Mode |
| RAT | Radio Access Technology |
| RCM | Regulatory Compliance Mark |
| RF | Radio Frequency |
| RRC | Radio Resource Control |
| RTS | Request To Send |
| SCL | Serial Clock |
| SDA | Serial Data |
| SIM | Subscriber Identity Module |
| SPI | Serial Peripheral Interface |
| SSL | Secure Sockets Layer |
| TCP | Transmission Control Protocol |
| TLS | Transport Layer Security |
| TXD | Transmit Data |
| UART | Universal Asynchronous Receiver/Transmitter |
| UDP | User Datagram Protocol |
| UL | Uplink (Transmission) |
| URC | Unsolicited Result Code |
| USB | Universal Serial Bus |
| VSWR | Voltage Standing Wave Ratio |

**Table 27: Abbreviations and terms**

# Related documentation

[1] u-blox SARA-N2/N3 series AT commands manual, UBX-16014887
[2] u-blox SARA-N2/N3 series system integration manual, UBX-17005143
[3] u-blox package information user guide, UBX-14001652
[4] ITU-T recommendation V24, 02-2000. List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Connection Equipment (DCE)
[5] RFC 7252 - Constrained Application Protocol (CoAP)
[6] u-blox SARA-N3 series application development guide, UBX-19026709

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

# Revision history

| Revision | Date | Name | Status / Comments |
|---|---|---|---|
| R01 | 10-Dec-2018 | sses | Initial release. |
| R02 | 08-Mar-2019 | sses | Remarked SARA-N3 series LTE Cat NB2 modules support key subset of features of 3GPP Release 14.<br>Revised Power-on, UART, ADC, GPIO and Approval sections.<br>Added current consumption figures. Other minor changes. |
| R03 | 18-Jul-2019 | fvid | Updated current consumption and ADC electrical specification. |
| R04 | 01-Oct-2019 | fvid / sses | Updated SARA-N300-00B / SARA-N310-00X product status.<br>Added ATEX / IECEx approval info.<br>Revised VCC normal operating input voltage range.<br>Added and revised current consumption figures.<br>Other minor changes. |
| R05 | 29-Jun-2020 | fvid | Specified that EasyFlash can be used for FW upgrade.<br>Added “Module status indication” GPIO function.<br>Updated RESET_N min low-level time.<br>Other minor changes. |
| R06 | 14-Oct-2020 | fvid / sses / alos | Updated SARA-N310-00X product status to initial production.<br>Updated current consumption figures.<br>Added ICASA certification.<br>Other minor changes. |
| R07 | 21-May-2021 | alos | Updated SARA-N310-00X application version and PCN reference. |
| R08 | 01-Oct-2021 | alos / fvid | Extended document applicability to SARA-N310-00X-01.<br>Removed document applicability to SARA-N300-00B-00.<br>Other minor corrections and clarifications with no impact for integrators. |
| R09 | 23-Nov-2021 | alos | Updated SARA-N310-00X-01 status to mass production.<br>Editorial changes and other minor clarifications. |
| R10 | 02-Mar-2022 | alos | Extended document applicability to SARA-N310-00X-02. |
| R11 | 27-Sep-2022 | fvid | Extended document applicability to SARA-N310-00X-03.<br>Updated RESET_N pin low-level time specification.<br>Updated “Approvals” section. |

# Contact

For further support and contact information, visit us at www.u-blox.com/support.