



# NEO-D9S-00A

**Correction data receiver**

**Automotive grade**

**Data sheet**



## **Abstract**

Technical data sheet describing the u-blox D9 automotive-grade correction data receiver. The module provides global and easy access to satellite L-band GNSS corrections.

# Document information

<b>Title</b>	<b>NEO-D9S-00A</b>	
<b>Subtitle</b>	Correction data receiver	
<b>Document type</b>	Data sheet	
<b>Document number</b>	UBX-21008859	
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<b>Disclosure restriction</b>	C1-Public	

<b>Product status</b>	<b>Corresponding content status</b>	
<b>Functional sample</b>	Draft	For functional testing. Revised and supplementary data will be published later.
<b>In development / prototype</b>	Objective specification	Target values. Revised and supplementary data will be published later.
<b>Engineering sample</b>	Advance information	Data based on early testing. Revised and supplementary data will be published later.
<b>Initial production</b>	Early production information	Data from product verification. Revised and supplementary data may be published later.
<b>Mass production / End of life</b>	Production information	Document contains the final product specification.

This document applies to the following products:

<b>Product name</b>	<b>Type number</b>	<b>FW version</b>	<b>IN/PCN reference</b>	<b>Product status</b>
NEO-D9S	NEO-D9S-00A-00	PMP 1.04	UBX-22039049 UBX-23000084	End of life
NEO-D9S	NEO-D9S-00A-01	PMP 1.06	UBX-22039058 UBX-22039049 UBX-23000084	Mass production

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# 1 Functional description

## 1.1 Overview

NEO-D9S-00A is a satellite data receiver for L-band correction broadcast. The receiver can be configured for use with a variety of correction services. It decodes the satellite transmission and outputs a correction stream, enabling a high precision GNSS receiver to reach accuracy down to centimeter level.

## 1.2 Performance

Parameter	Specification	
Receiver type	NEO-D9S correction data receiver	
<b>L-band satellite</b>		
<b>Specification</b>		
Time to first frame <sup>1</sup>	< 10 s at 2400 bps	
Sensitivity acquisition <sup>2</sup>	-133 dBm for BER <10e-5 at 2400 bit/s	
Specification compliance	L-band SESTB28A	
Boot time	<1 s	
Center frequency configuration steps	1 Hz	
Center frequency search window	0 to 65 kHz	
User data rates	600, 1200, 2400, 4800 bps	
Service identifier	Configurable	
De-scrambler	Configurable	
De-scrambling initialization vector	Configurable	
Pre-scrambler	Enable/disable	
Number of concurrent reception channels	1	
UniqueWord	Configurable	
Frequency range	1525 MHz to 1559 MHz	
Vehicle dynamics	Dynamics	+/- 2g acceleration for all data rates (600 bit/s, 1200 bit/s, 2400 bit/s, 4800 bit/s)
	Velocity	Up to and including 300 km/h

Table 1: NEO-D9S-00A performance

## 1.3 Supported GNSS augmentation systems

### 1.3.1 Satellite L-band

The satellite L-band communication system allows GNSS correction service providers to broadcast a variety of services on specific channels, satellites and beams. Consult your service provider on the region their service covers and the specific frequency used. The NEO-D9S-00A must be configured according to the specific service as initial identification and decoding of the service provider stream is required.

<sup>1</sup> With respect to an L-band signal using a 20-25 dB external LNA

<sup>2</sup> Success rate of acquiring an L-band signal > 95% using a 20-25 dB external LNA

## 1.4 Supported protocols

NEO-D9S-00A supports the following protocols:

Protocol	Type
UBX	Input/output, binary, u-blox proprietary

**Table 2: Supported protocols**

For specification of the protocols, see the Interface description [\[2\]](#).

## 2 System description

### 2.1 Block diagram

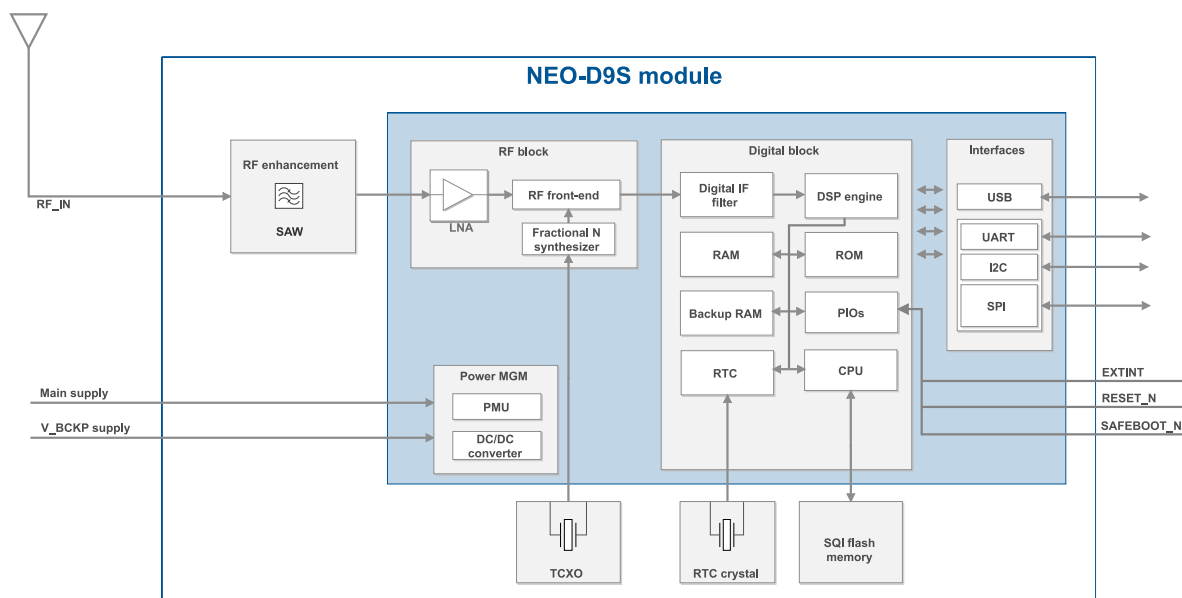


Figure 1: NEO-D9S-00A block diagram

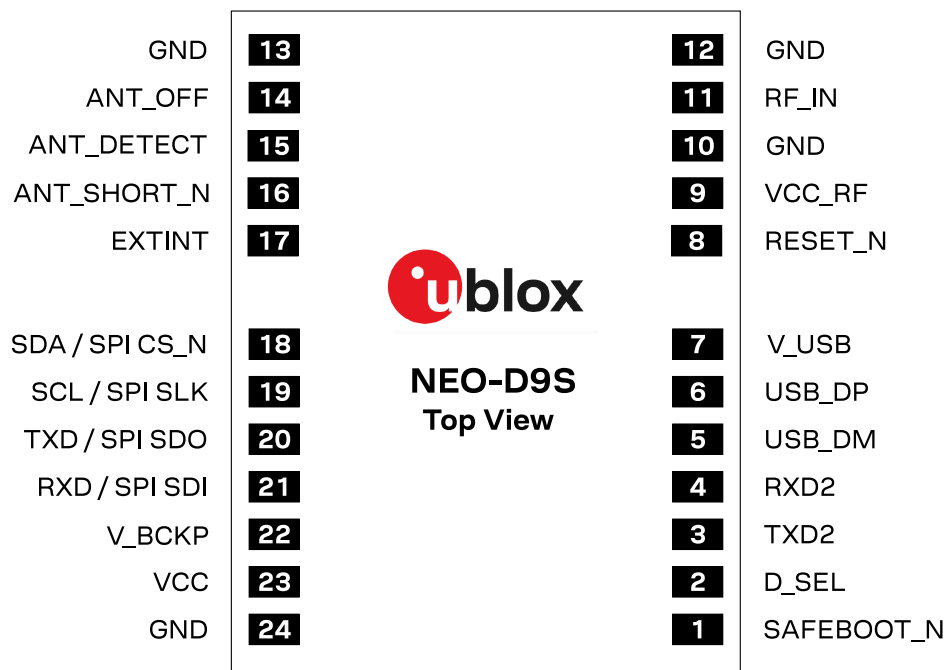


An active antenna is mandatory with the NEO-D9S-00A.

## 3 Pin definition

### 3.1 Pin assignment

The pin assignment of the NEO-D9S-00A module is shown in [Figure 2](#). The defined configuration of the PIOs is listed in [Table 3](#).



**Figure 2: NEO-D9S-00A pin assignment**

Pin no.	Name	I/O	Description
1	SAFEBOOT_N	I	SAFEBOOT_N (used for FW updates and reconfiguration, leave open)
2	D_SEL	I	UART 1 / SPI select. (open or high = UART 1)
3	TXD2	O	UART 2 TXD
4	RXD2	I	UART 2 RXD
5	USB_DM	I/O	USB data (DM)
6	USB_DP	I/O	USB data (DP)
7	V_USB	I	USB supply
8	RESET_N	I	RESET (active low)
9	VCC_RF	O	External LNA power
10	GND	I	Ground
11	RF_IN	I	Active antenna L-band signal input
12	GND	I	Ground
13	GND	I	Ground
14	ANT_OFF	O	External LNA disable - default active high
15	ANT_DETECT	I	Active antenna detect - default active high

Pin no.	Name	I/O	Description
16	ANT_SHORT_N	O	Active antenna short detect - default active low
17	EXTINT	I	External interrupt pin
18	SDA / SPI CS_N	I/O	I2C data if D_SEL = VCC (or open); SPI chip select if D_SEL = GND
19	SCL / SPI SLK	I/O	I2C clock if D_SEL = VCC (or open); SPI clock if D_SEL = GND
20	TXD / SPI SDO	O	UART1 output if D_SEL = VCC (or open); SPI SDO if D_SEL = GND
21	RXD / SPI SDI	I	UART1 input if D_SEL = VCC (or open); SPI SDI if D_SEL = GND
22	V_BCKP	I	Connect to VCC or leave it open
23	VCC	I	Supply voltage
24	GND	I	Ground

**Table 3: NEO-D9S-00A pin assignment**



For detailed information on the pin functions and characteristics see the Integration manual [1].

## 4 Electrical specifications

### 4.1 Absolute maximum ratings

- CAUTION. Risk of device damage. Exceeding the absolute maximum ratings may affect the lifetime and reliability of the device or permanently damage it. Do not exceed the absolute maximum ratings.
- This product is not protected against overvoltage or reversed voltages. Use appropriate protection to avoid device damage from voltage spikes exceeding the specified boundaries.

Parameter	Symbol	Condition	Min	Max	Units
Power supply voltage	VCC		-0.5	3.6	V
Voltage ramp on VCC <sup>3</sup>			20	8000	µs/V
Input pin voltage	V <sub>in</sub>		-0.5	VCC + 0.5	V
VCC_RF output current	ICC_RF			300	mA
Supply voltage USB	V_USB		-0.5	3.6	V
USB signals	USB_DM, USB_DP		-0.5	V_USB + 0.5 V	
Input power at RF_IN	Pr <sub>fin</sub>	Source impedance = 50 Ω, continuous wave		10	dBm
Storage temperature	T <sub>stg</sub>		-40	+105	°C

**Table 4: Absolute maximum ratings**

### 4.2 Operating conditions

- Extreme operating temperatures can significantly impact the specified values. If an application operates near the min or max temperature limits, ensure the specified values are not exceeded.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Power supply voltage	VCC	2.7	3.0	3.6	V	
Supply voltage for USB interface	V_USB	3.0		3.6	V	
V_USB current	I_USB		2.0		mA	
SW backup current	I_SWBCKP		1.4		mA	
Input pin voltage range	V <sub>in</sub>	0		VCC	V	
Digital IO pin low level input voltage	V <sub>il</sub>			0.4	V	
Digital IO pin high level input voltage	V <sub>ih</sub>	0.8 * VCC			V	
Digital IO pin low level output voltage	V <sub>ol</sub>			0.4	V	I <sub>ol</sub> = 2 mA
Digital IO pin high level output voltage	V <sub>oh</sub>	VCC - 0.4			V	I <sub>oh</sub> = 2 mA
DC current through any digital I/O pin (except supplies)	I <sub>pin</sub>			5	mA	
Pull-up resistance for RXD2, TXD2, SDA / SPI_CS_N, SCL / SPI_CLK	R <sub>pu</sub>	7	15	30	kΩ	
Pull-up resistance for ANT_DETECT, ANT_OFF, ANT_SHORT_N, TXD / SPI_SDO, RXD / SPI_SDI, EXTINT	R <sub>pu</sub>	30	75	130	kΩ	
Pull-up resistance for RESET_N	R <sub>pu</sub>	7	10	13	kΩ	
VCC_RF voltage	VCC_RF		VCC - 0.1		V	

<sup>3</sup> Exceeding the ramp speed may permanently damage the device


Parameter	Symbol	Min	Typical	Max	Units	Condition
VCC_RF output current	ICC_RF			50	mA	
Input impedance at RF_IN	Z <sub>in</sub>		50		Ω	
Receiver chain noise figure <sup>4</sup>	NF <sub>tot</sub>		11		dB	
Recommended LNA gain into module	LNA_gain		20		dB	
Operating temperature	Topr	-40	+25	+105	°C	

**Table 5: Operating conditions**

### 4.3 Indicative power requirements

Table 6 provides examples of typical current requirements when using a cold start command. The given values are total system supply current for a possible application including RF and baseband sections.

All values in Table 6 have been measured at 25 °C ambient temperature.

 The actual power requirements vary depending on the FW version used, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	L - band SESTB28A	Unit
I <sub>PEAK</sub>	Peak current	Acquisition & tracking	130	mA
I <sub>AVERAGE</sub>	Average current	Acquisition & tracking	55	mA

**Table 6: Currents to calculate the indicative power requirements**

<sup>4</sup> Only valid for the L-band band

## 5 Communications interfaces

NEO-D9S-00A has several communications interfaces<sup>5</sup>, including UART, SPI, I2C and USB.

All the inputs have internal pull-up resistors in normal operation and can be left open if not used. All the PIOs are supplied by VCC, therefore all the voltage levels of the PIO pins are related to VCC supply voltage.

### 5.1 UART

The UART interfaces support configurable baud rates. For further information, see the Integration manual [1].

Hardware flow control is not supported.

UART1 is the primary host communications interface.

Symbol	Parameter	Min	Max	Unit
$R_u$	Baud rate	9600	921600	bit/s
$\Delta_{Tx}$	Tx baud rate accuracy	-1%	+1%	-
$\Delta_{Rx}$	Rx baud rate tolerance	-2.5%	+2.5%	-

Table 7: NEO-D9S-00A UART specifications

### 5.2 SPI

The SPI interface is disabled by default. The SPI interface shares pins with UART and I2C and can be selected by setting  $D\_SEL = 0$ . The SPI interface can be operated in peripheral mode only. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.

The SPI timing parameters for peripheral operation are defined in Figure 3. Default SPI configuration is  $CPOL = 0$  and  $CPHA = 0$ .

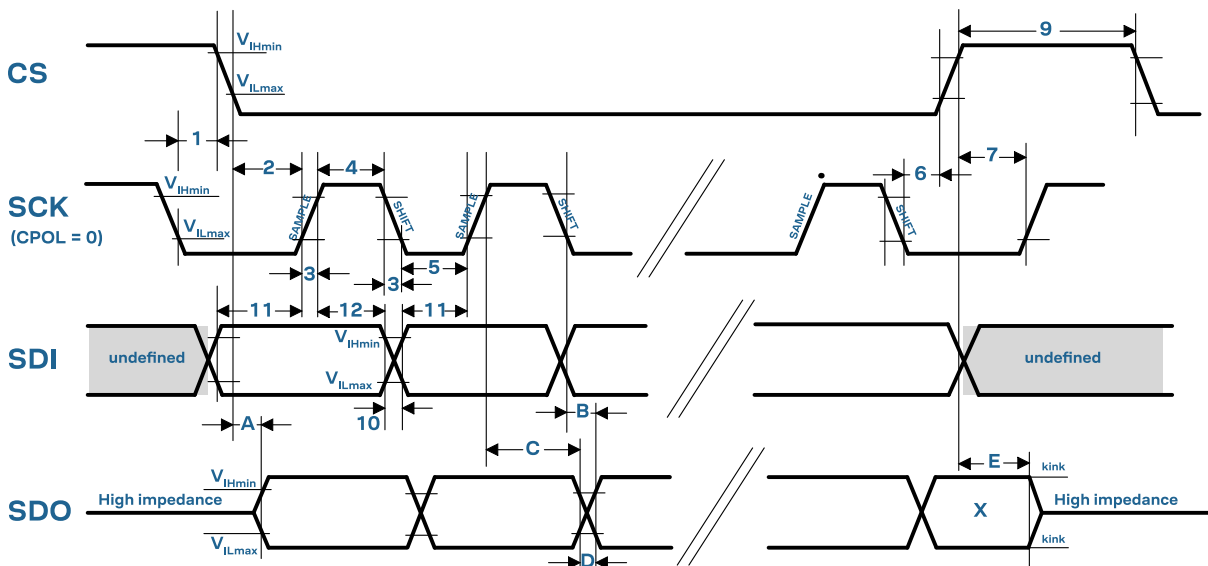


Figure 3: NEO-D9S-00A SPI specification mode 1:  $CPHA=0$   $SCK = 5.33$  MHz

<sup>5</sup> The signal names and related terms have been replaced with new terminology in this document.

Symbol	Parameter	Min	Max	Unit
1	CS deassertion hold time	23	-	ns
2	Chip select time (CS to SCK)	20	-	ns
3	SCK rise/fall time	-	7	ns
4	SCK high time	24	-	ns
5	SCK low time	24	-	ns
6	Chip deselect time (SCK falling to CS)	30	-	ns
7	Chip deselect time (CS to SCK)	30	-	ns
9	CS high time	32	-	ns
10	SDI transition time	-	7	ns
11	SDI setup time	16	-	ns
12	SDI hold time	24	-	ns

**Table 8: SPI peripheral input timing parameters 1 - 12**

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	12	40	ns
B	SDO data valid time (SCK), weak driver mode	15	40	ns
C	SDO data hold time	100	140	ns
D	SDO rise/fall time, weak driver mode	0	5	ns
E	SDO data disable lag time	15	35	ns

**Table 9: SPI peripheral timing parameters A - E, 2 pF load capacitance**

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	16	55	ns
B	SDO data valid time (SCK), weak driver mode	20	55	ns
C	SDO data hold time	100	150	ns
D	SDO rise/fall time, weak driver mode	3	20	ns
E	SDO data disable lag time	15	35	ns

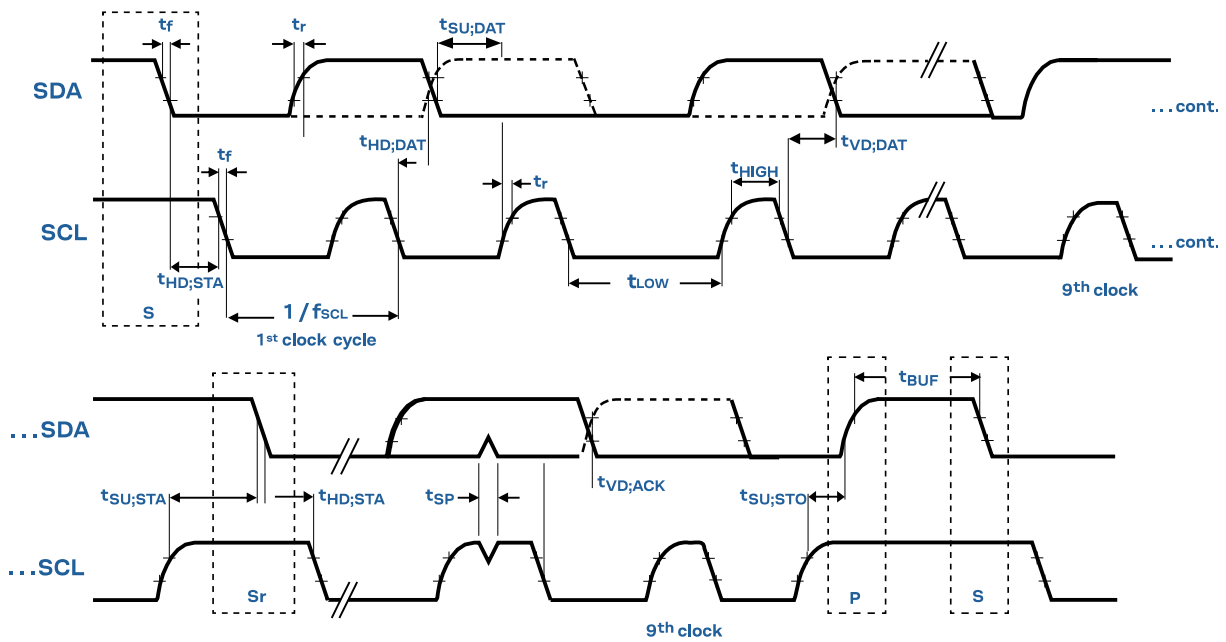
**Table 10: SPI peripheral timing parameters A - E, 20 pF load capacitance**

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	26	85	ns
B	SDO data valid time (SCK), weak driver mode	30	85	ns
C	SDO data hold time	110	160	ns
D	SDO rise/fall time, weak driver mode	13	45	ns
E	SDO data disable lag time	15	35	ns

**Table 11: SPI peripheral timing parameters A - E, 60 pF load capacitance**

## 5.3 I2C

An I2C interface is available for communication with an external host CPU in I2C Fast-mode. Backwards compatibility with Standard-mode I2C bus operation is not supported. The interface can be operated only in peripheral mode with a maximum bit rate of 400 kbit/s. The interface can make use of clock stretching by holding the SCL line LOW to pause a transaction. In this case, the bit transfer rate is reduced. The maximum clock stretching time is 20 ms.



$$V_{IL} = 0.3 V_{DD}$$

$$V_{IH} = 0.7 V_{DD}$$

Figure 4: NEO-D9S-00A I2C peripheral specification

Symbol	Parameter	I2C Fast-mode		Unit
		Min	Max	
$f_{SCL}$	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	0.6	-	$\mu s$
$t_{LOW}$	Low period of the SCL clock	1.3	-	$\mu s$
$t_{HIGH}$	High period of the SCL clock	0.6	-	$\mu s$
$t_{SU;STA}$	Setup time for a repeated START condition	0.6	-	$\mu s$
$t_{HD;DAT}$	Data hold time	$0^6$	$_7$	$\mu s$
$t_{SU;DAT}$	Data setup time	$100^8$		ns
$t_r$	Rise time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
$t_f$	Fall time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6	-	$\mu s$
$t_{BUF}$	Bus-free time between a STOP and START condition	1.3	-	$\mu s$
$t_{VD;DAT}$	Data valid time	-	$0.9^7$	$\mu s$
$t_{VD;ACK}$	Data valid acknowledge time	-	$0.9^7$	$\mu s$
$V_{nL}$	Noise margin at the low level	$0.1 V_{IO}$	-	V

<sup>6</sup> External device must provide a hold time of at least one transition time (max 300 ns) for the SDA signal (with respect to the min  $V_{ih}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

<sup>7</sup> The maximum  $t_{HD;DAT}$  must be less than the maximum  $t_{VD;DAT}$  or  $t_{VD;ACK}$  with a maximum of  $0.9 \mu s$  by a transition time. This maximum must only be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

<sup>8</sup> When the I2C peripheral is stretching the clock, the  $t_{SU;DAT}$  of the first bit of the next byte is 62.5 ns.

Symbol	Parameter	I2C Fast-mode		Unit
		Min	Max	
V <sub>nH</sub>	Noise margin at the high level	0.2 V <sub>IO</sub>	-	V

**Table 12: NEO-D9S-00A I2C peripheral timings and specifications**


The I2C interface is only available with the UART default mode. If the SPI interface is selected by using D\_SEL = 0, the I2C interface is not available.

## 5.4 USB

The USB 2.0 FS (full speed, 12 Mbit/s) interface can be used for host communication. Due to the hardware implementation, it may not be possible to certify the USB interface. The V\_USB pin supplies the USB interface.

## 5.5 Default interface settings

Interface	Settings
UART	9600 baud, 8 bits, no parity bit, 1 stop bit. Output protocol: UBX. Input protocols without need of additional configuration: UBX.
USB	Output messages activated as in UART. Input protocols available as in UART.
I2C	Output messages activated as in UART. Input protocols available as in UART.
SPI	Output messages activated as in UART. Input protocols available as in UART.

**Table 13: Default interface settings**


The boot message is still output using \$GNTXT messages. The messages are output when the NEO-D9S-00A is powered up.



Refer to the applicable Interface description [2] for information about further settings.

## 6 Mechanical specifications

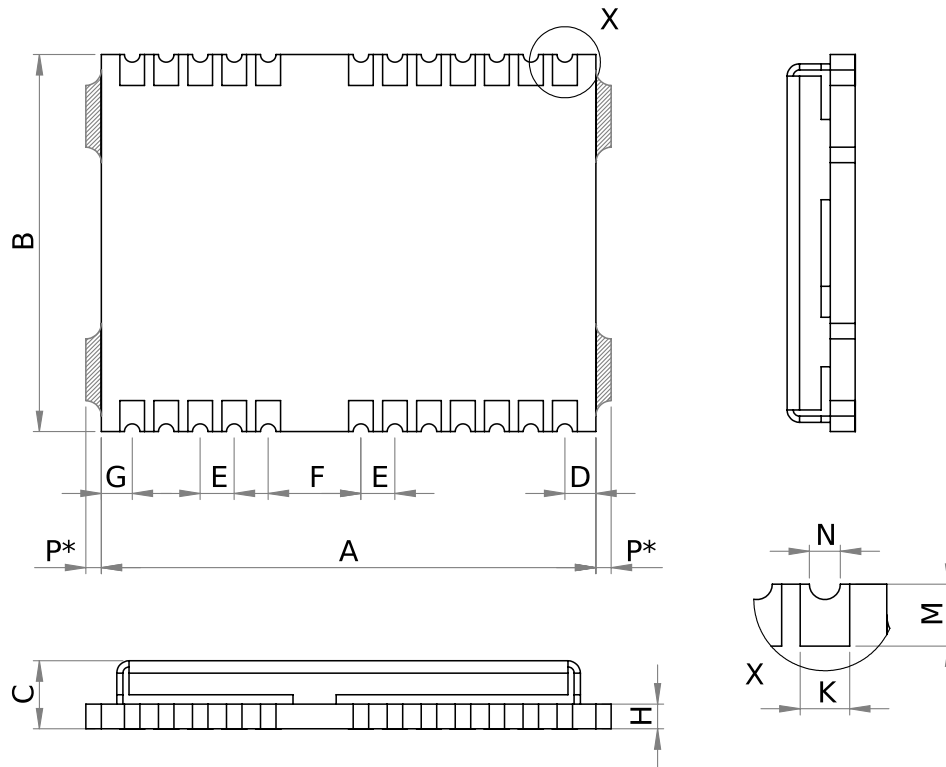




Figure 5: NEO-D9S-00A mechanical drawing

Symbol	Min (mm)	Typical (mm)	Max (mm)	
A	15.9	16.0	16.1	
B	12.1	12.2	12.3	
C	2.2	2.4	2.6	
D	0.9	1.0	1.1	
E	1.0	1.1	1.2	
F	2.9	3.0	3.1	
G	0.9	1.0	1.1	
H	-	0.82	-	
K	0.7	0.8	0.9	
M	0.8	0.9	1.0	
N	0.4	0.5	0.6	
P*	0.0	-	0.5	The de-paneling residual tabs may be on either side (not both).
Weight		1.0 g		

Table 14: NEO-D9S-00A mechanical dimensions

-  The mechanical picture of the de-paneling residual tabs (P\*) is an approximate representation. The shape and position may vary, but the overall size of the residual tabs remains within the maximum dimensions even when the tab sizes differ.
-  Take the size of the de-paneling residual tabs into account when designing the component keep-out area.

## 7 Qualifications and approvals

<b>Quality and reliability</b>	
Product qualification	Qualified according to AEC-Q104
Chip qualification	Modules are based on AEC-Q100 qualified GNSS chips
Manufacturing	Manufactured at ISO/TS 16949 certified sites
<b>Environmental</b>	
RoHS compliance	Yes
Moisture sensitivity level (MSL) <sup>9, 10</sup>	3
<b>Type approvals</b>	
European RED certification (CE)	Declaration of Conformity (DoC) is available on the <a href="#">u-blox website</a> .
UK conformity assessment (UKCA)	Yes

**Table 15: Qualifications and approvals**

<sup>9</sup> For the MSL standard, see IPC/JEDEC J-STD-020 and J-STD-033, available on [www.jedec.org](http://www.jedec.org)

<sup>10</sup> For more information regarding moisture sensitivity levels, labelling, storage and drying, see the Product packaging reference guide [4]

## 8 Product marking and ordering information

This section provides information about product marking and ordering.

### 8.1 Product marking

The product marking provides information on NEO-D9S-00A and its revision, as in [Figure 6](#). For a description of the product marking, see [Table 16](#).

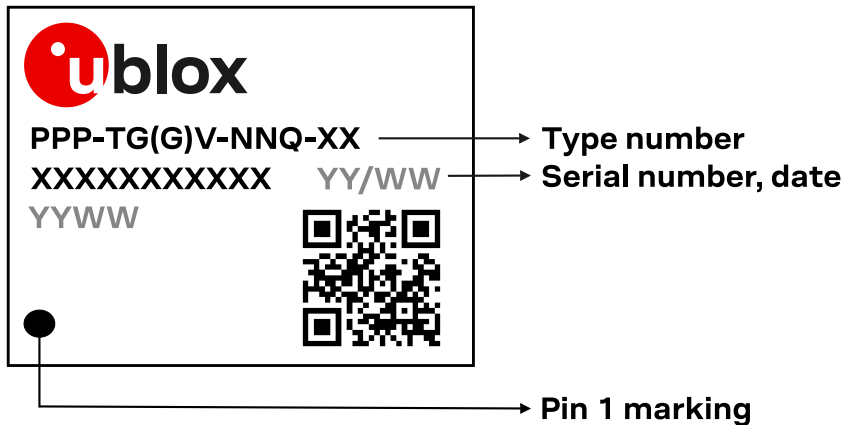


Figure 6: Example of NEO-D9S-00A product marking

Code	Meaning	Example
PPP	Form factor	NEO
TG(G)	Platform	D9 = u-blox D9
V	Variant	S = L-band corrections
NN	Major product version	00, 01, ..., 99
Q	Product grade	A = Automotive, B = Professional, C= Standard
XX	Revision	Hardware and firmware revisions
YY/WW or YYWW	Production date	Year/week, e.g. 24/04 or 2404
XXXXXXXXXXXX	Serial number	Alphanumeric characters, e.g. BN600001181
Other information	QR code	For internal/technical use.

Table 16: Description of product marking

### 8.2 Product identifiers

The NEO-D9S-00A label features three product identifiers: product name, ordering code, and type number. The product name identifies all u-blox products. It is used in documentation such as this Data sheet and is independent of packaging and product grade. The ordering code indicates the major product version and product grade, and the type number additionally specifies the hardware and firmware revisions.

[Table 17](#) describes the three different product identifiers used in the NEO-D9S-00A label

Identifier	Format	Example
Product name	PPP-TG(G)V	NEO-D9S
Ordering code	PPP-TG(G)V-NNQ	NEO-D9S-00A
Type number	PPP-TG(G)V-NNQ-XX	NEO-D9S-00A-00

Table 17: Product identifiers

### 8.3 Ordering codes

Ordering code	Product	Remark
NEO-D9S-00A	NEO-D9S correction data receiver	u-blox D9 automotive grade correction data receiver for L-band broadcast

**Table 18: Product ordering codes**

u-blox provides information on product changes affecting the form factor, size or function of the product. For the Product change notifications (PCNs), see our website at <https://www.u-blox.com/en/product-resources>.

## Related documents

- [1] NEO-D9S Integration manual [UBX-19026111](#)
- [2] PMP 1.06 Interface description, [UBX-22038891](#)
- [3] PMP 1.04 Interface description [UBX-21040023](#)
- [4] Product packaging reference guide, [UBX-14001652](#)



For regular updates to u-blox documentation and to receive product change notifications please register on our homepage <https://www.u-blox.com>.

## Revision history

Revision	Date	Status / comments
R01	21-Oct-2021	Advance information
R02	24-Jan-2022	Early production information UART2 interface general update. Voltage ramp on VCC value added in Absolute maximum ratings table. V_BCKP general update
R03	08-Aug-2022	Production information
R04	05-Jan-2023	Updated NEO-D9S-00A-01 version. Overall text improvement Updated the section Mechanical specification
R05	29-Mar-2023	Updated I2C and SPI timing specifications in section Communications interfaces Updated VCC_RF output current in table Absolute maximum ratings
R06	7-Feb-2024	End of life for NEO-D9S-00A-00 with PMP 1.04 FW Mass production for NEO-D9S-00A-01 with PMP 1.06 FW Editorial changes throughout the document
R07	29-Oct-2025	Updated weight in Mechanical specifications Editorial changes in sections Qualifications and approvals and Product marking

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