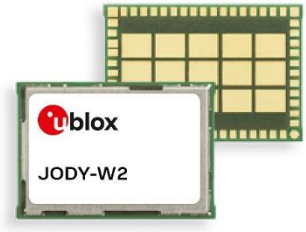
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JODY-W2

Host-based multiradio modules with Wi-Fi 5 and Bluetooth 5.2

System integration manual



Abstract

This document describes the system integration of JODY-W2 series modules. These host-based modules support Wi-Fi 802.11n/ac and Bluetooth® 5.2 and are designed for both simultaneous and independent operations. The JODY-W2 modules include an integrated MAC/baseband processor and RF front-end components and are offered in both professional and automotive grades.

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Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	**Document status**
JODY-W263-A	Production information
JODY-W263	Production information

☞ For information about the related hardware, software, and status of listed product types, refer to the respective data sheet [2].

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1 System description

1.1 Overview and applications

The JODY-W2 series provides a complete short range transceiver solution that can be easily integrated into automotive and industrial applications. The modules are designed for both simultaneous and independent operation of the following technologies:

- Wi-Fi interface supporting IEEE 802.11a/b/g/n/ac data rates up to 433 Mbit/s
- Bluetooth 5.2

JODY-W2 series modules are surface-mount device (SMD) components and can be used as a Wi-Fi micro-access point for up to eight clients. A coexistence feature on chip level improves parallel use of Bluetooth and Wi-Fi communication. For highest throughput and performance, Wi-Fi and Bluetooth have separate antenna pins.

1.1.1 Product features

Item	JODY-W263-A	JODY-W263
Grade	Automotive	Professional
Chipset	NXP 88W8987A/S	NXP 88W8987
Antenna type	Two antenna pins for Wi-Fi and Bluetooth	Two antenna pins for Wi-Fi and Bluetooth
Supported Wi-Fi radio modes	IEEE 802.11 a/b/g/n/ac	IEEE 802.11 a/b/g/n/ac
Supported Wi-Fi bands	2.5 / 5 GHz	2.5 / 5 GHz
Max. Wi-Fi output power	19 dBm (at antenna pin)	19 dBm (at antenna pin)
Bluetooth version	5.2	5.2
Bluetooth profiles	HCI	HCI
Supported Bluetooth radio modes	Bluetooth BR/EDR Bluetooth Low Energy	Bluetooth BR/EDR Bluetooth Low Energy
Supported Bluetooth LE data rates	1 Mbps 2 Mbps	1 Mbps 2 Mbps
LTE coexistence filter	-	-
OS support	Linux / Android	Linux / Android
Interfaces	SDIO 3.0 (Wi-Fi/Bluetooth) UART (Bluetooth) PCM (Bluetooth digital audio)	SDIO 3.0 (Wi-Fi/Bluetooth) UART (Bluetooth) PCM (Bluetooth digital audio)
Features	Micro access point with max. 8 connected clients	Micro access point with max. 8 connected clients
	Simultaneous client and access point mode	Simultaneous client and access point mode
	WPA3	WPA3
	RF parameters/MAC addresses in OTP	RF parameters/MAC addresses in OTP
Max. ambient operating temperature	85 °C (JODY-W263-00A) 105 °C (JODY-W263-01A)	85 °C
Module size	19.8 x 13.8 mm	19.8 x 13.8 mm

Table 1: JODY-W2 series product features

1.1.2 Module architecture

Table 2 shows the available antenna (ANT0 and ANT1) and host interface configurations for the different JODY-W2 series module variants.

Product type	ANT0 configuration	ANT1 configuration	Host interface
JODY-W263 JODY-W263-A	2.4 GHz Bluetooth	2.4 GHz and 5 GHz Wi-Fi	SDIO Wi-Fi (optional Bluetooth) UART Bluetooth

Table 2: Supported configurations of the JODY-W2 module series

JODY-W2 series module has two antenna pins with one dedicated for dual band Wi-Fi (2.4 GHz and 5 GHz) and the other for Bluetooth. The block diagram shown in Figure 1 is applicable for both professional and automotive-grade variants.

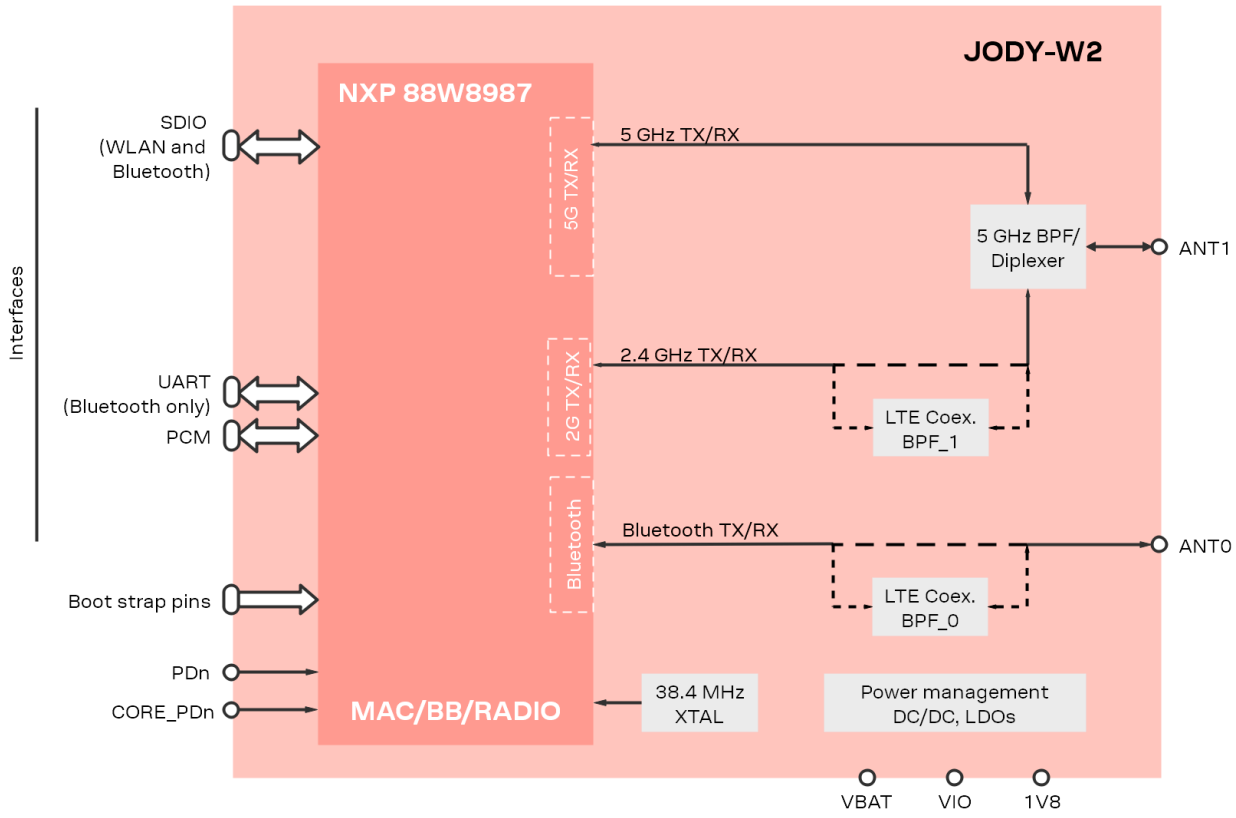


Figure 1: Block diagram of JODY-W2

JODY-W2 variants with a dedicated LTE Coexistence Filter (2.4 GHz BPF) are available on request. Coexistence filters are only needed if LTE bands 7, 38, 40, and 41 are used.

1.1.3 Power management

JODY-W2 series modules have several operation modes. The operation modes and general guidelines for Wi-Fi and Bluetooth operation are defined in Table 3.

General Status	Power State	Description
Power-down	Not Powered	**VBAT**, **VIO,** and **1V8** supply not present or below the operating range: module is switched off.
	Power Down	This is done by asserting **PDn** and **CORE_PDn** low. This is the lowest power condition with active voltage rails. All internal clocks are shut down; register and memory states are not maintained. Upon exiting power down mode, a reset is automatically performed, and a firmware re-download is required to re-enter any of the normal operation modes.
General operation	Deep Sleep	This is a low-power state used in the sleep state of many power save modes. It is a low-power state where the internal reference clock and many blocks in the chip are switched off. Only a slow sleep clock is used to maintain register and memory states. Wake-up does not require a firmware re-download.
	Active	TX/RX data connection enabled, with the system running at the specified power consumption.
Wi-Fi operation	IEEE Power Save (Station mode)	The device automatically wakes up for beacon reception. This is dependent on the DTIM value of the AP it is connected to. If it is a DTIM value of 1 along with a beacon interval of 100 ms, the device wakes up every 100 ms. Similarly, with DTIM =2, the device wakes up at every 200 ms, and so on.
Bluetooth operation	Page scan	The device accepts connection and waits for a connection.
	Page & Inquiry Scan	The device is actively searching for connection.
	LE advertisement	Bluetooth LE advertisement, transmits advertisement data periodically.

Table 3: Power states

1.2 Pin configuration and function

1.2.1 Pin attributes

- **FUNCTION**: Pin function
- **PIN NAME**: The name of the package pin or terminal
- **PIN NUMBER**: Package pin numbers associated with each signal.
- **POWER**: The voltage domain that powers the pin
- **TYPE**: Signal type description:
  - I = Input
  - O = Output
  - I/O = Input and Output
  - D = Open drain
  - DS = Differential
  - PWR = Power
  - GND = Ground
  - PU = Internal pull-up
  - PD = Internal pull-down
  - H = High-Impedance pin
  - RF = Radio interface
- **SIGNAL NAME**: The signal name for that pin in the mode being used.
- **REMARKS**: Pin description and notes.

1.2.2 Pin list

Figure 2 and Table 4 show the pin-out of the JODY-W2 module, with pins grouped by function.

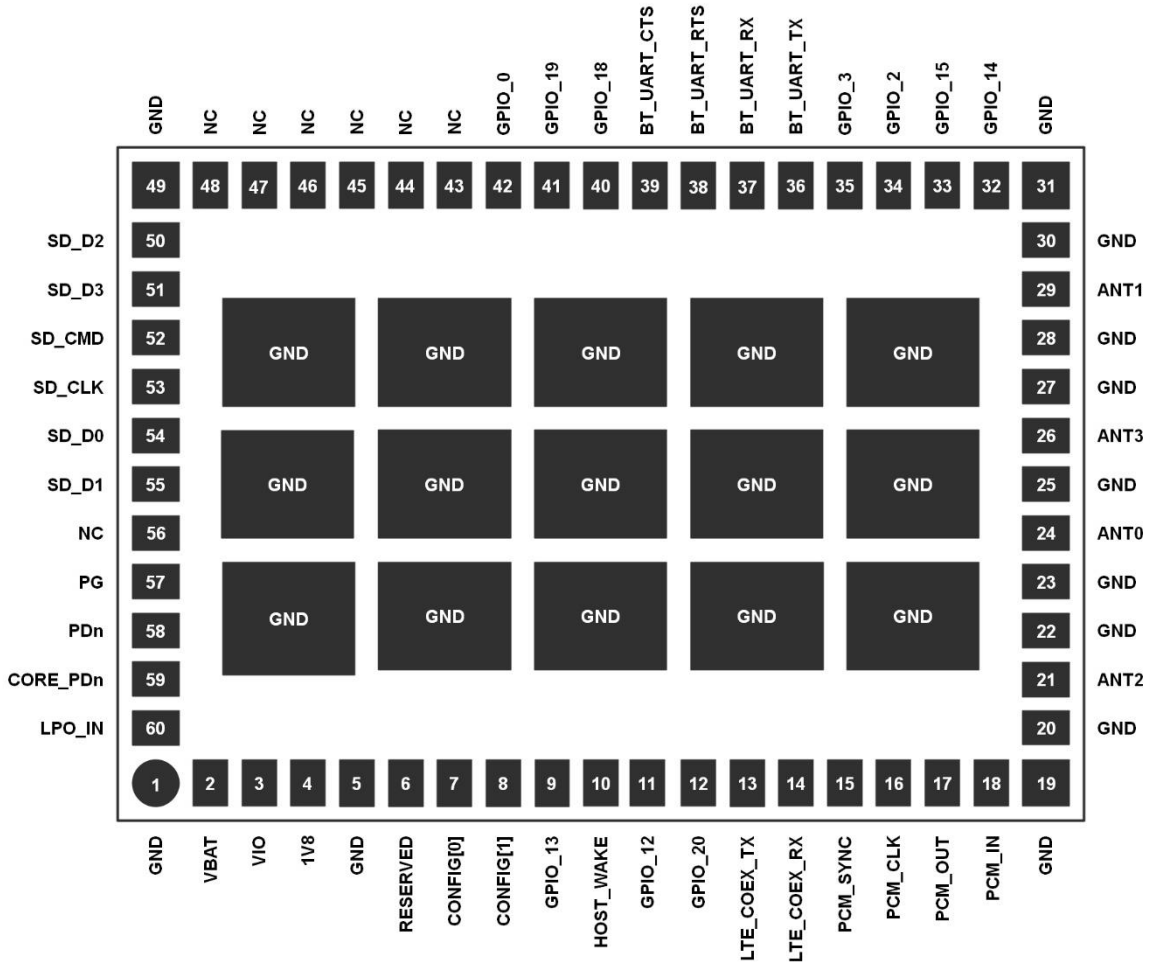


Figure 2: JODY-W2 pin assignment (top view)

No.	Name	Chip pin	I/O[1]	Description	Domain
1	GND		GND	Ground	GND
2	VBAT		PWR	Module supply input (2.8 V – 5.5 V)	VBAT
3	VIO		PWR	VIO supply (1.8 V or 3.3 V)	VIO
4	1V8		PWR	VIO supply for SDIO, Supply for analog part (1.8 V)	1V8
5	GND		GND	Ground	GND
6	CONFIG[2]		NC	Reserved for future use. A “DNI” pull-up resistor should be added at this pin to respond to future chipset changes.	1V8
7	CONFIG[0]	CONFIG_HOST[0]	I	Configuration pin, see also Table 7: Host interface configuration options	1V8
8	CONFIG[1]	CONFIG_HOST[1]	I	Configuration pin, see also Table 7: Host interface configuration options	1V8

[1] I/O notations: I=Input, O=Output, I/O=Input or Output, OD=Open Drain, NC=Not Connected, PWR=Power, GND=Ground, RF=Radio i/f

No.	Name	Chip pin	I/O[1]	Description	Domain
9	GPIO_13	GPIO[13]	I/O	Optional host to Wi-Fi out-of-band wake-up signal (input)	VIO
10	HOST_WAKE	GPIO[1]	I/O	Wi-Fi to host out-of-band wake-up signal (output)	VIO
11	GPIO_12	GPIO[12]	I/O	Optional host to Bluetooth out-of-band wake-up signal (input)	VIO
12	GPIO_20	GPIO[20]	I/O	Bluetooth to host out-of-band wake-up signal (output) GPIO_1 or GPIO_4 can be used as alternative signals.	VIO
13	LTE_COEX_TX	GPIO[17] / JTAG_TDO	I/O	Configuration pin, see also Table 8: Additional configuration pins	VIO
14	LTE_COEX_RX	GPIO[16] / JTAG_TDI	I/O		VIO
15	PCM_SYNC	PCM_SYNC / GPIO[7]	I/O	PCM frame sync, can be output (master) or input (slave)	VIO
16	PCM_CLK	PCM_CLK / GPIO[6]	I/O	PCM clock, can be output (master) or input (slave)	VIO
17	PCM_OUT	PCM_DOUT / GPIO[5]	O	PCM data output Configuration pin, see also Table 8: Additional configuration pins	VIO
18	PCM_IN	PCM_DIN / GPIO[4]	I	PCM data input	VIO
19	GND		GND	Ground	GND
20	GND		GND	Ground	GND
21	ANT2		NC	Reserved (Do not connect)	-
22	GND		GND	Ground	GND
23	GND		GND	Ground	GND
24	ANT0		RF	Bluetooth antenna signal. Do not connect to DC	VBAT
25	GND		GND	Ground	GND
26	ANT3		NC	Reserved (Do not connect)	-
27	GND		GND	Ground	GND
28	GND		GND	Ground	GND
29	ANT1		RF	Wi-Fi dual-band antenna signal. Do not connect to DC	VBAT
30	GND		GND	Ground	GND
31	GND		GND	Ground	GND
32	GPIO_14	GPIO[14] / JTAG_TCK	I/O	Can be used as Wi-Fi independent reset signal (input)	VIO
33	GPIO_15	GPIO[15] / JTAG_TMS	I/O	Can be used as Bluetooth independent reset signal (input)	VIO
34	GPIO_2	GPIO[2]	I/O		VIO
35	GPIO_3	GPIO[3]	I/O		VIO
36	BT_UART_TX	UART_SOUT / GPIO[8]	O	Bluetooth UART serial data output Configuration pin, see also Table 8: Additional configuration pins	VIO
37	BT_UART_RX	UART_SIN / GPIO[9]	I	Bluetooth UART serial data input	VIO
38	BT_UART_RTS	UART_RTSn / GPIO[11]	O	Bluetooth UART active-low request-to-send signal (output) Configuration pin, see also Table 8: Additional configuration pins	VIO
39	BT_UART_CTS	UART_CTSn / GPIO[10]	I	Bluetooth UART active-low clear-to-send signal (input)	VIO
40	GPIO_18	GPIO[18]	I/O		VIO
41	GPIO_19	GPIO[19]	I/O		VIO

No.	Name	Chip pin	I/O[1]	Description	Domain
42	GPIO_0	GPIO[0]	I/O		VIO
43-48	NC		NC	Reserved (Do not connect)	-
49	GND		GND	Ground	GND
50	SD_D2	SD_DAT[2]	I/O	SDIO data line bit [2]	1V8
51	SD_D3	SD_DAT[3]	I/O	SDIO data line bit [3]	1V8
52	SD_CMD	SD_CMD	I/O	SDIO Command line	1V8
53	SD_CLK	SD_CLK	I	SDIO Clock input	1V8
54	SD_D0	SD_DAT[0]	I/O	SDIO data line bit [0]	1V8
55	SD_D1	SD_DAT[1]	I/O	SDIO data line bit [1]	1V8
56	NC		NC	Reserved (Do not connect)	-
57	PG		OD	Open-drain output from the internal DC/DC converter, which indicates the power quality of the 2.2 V rail. High impedance indicates power good. Low level indicates 2.2 V is not in power good. A (100 kΩ) pull-up resistor must be connected to this pin to detect the power good state.	-
58	PDn	PDn	I	Power-down interface of the chipset: 0 = power-down mode 1 = normal mode Can accept an input of 1.8 V to 4.5 V. No Internal pull-up on this pin.	1V8
59	CORE_PDn		I	Enable pin of the core voltage regulator: 0 = power supply off Connect with PDn	1V8
60	LPO_IN	SPL_CLK_IN	I	Sleep clock input (optional) 32.768 kHz clock input used for lower power operation in sleep mode. Only supported on professional grade variants:JODY-W263-xxB	VIO
-	Exposed Pins		GND	15 Ground/Thermal exposed pins Connect to ground, see also Thermal guidelines	GND

Table 4: JODY-W2 pin description

1.2.3 Main supply inputs

JODY-W2 series modules are supplied through the **VBAT/VIO/1V8** pins. **VBAT** supplies power to the internal power management circuitry that includes a SMPS converter and a LDO that source the system ASIC.

The current drawn by the JODY-W2 series through the **VBAT** pin can vary by several orders of magnitude depending on the operation mode and state. It changes from high current consumption during Wi-Fi transmission at maximum RF power level in connected-mode to low current consumption during low power idle-mode with the power saving configuration enabled.

The electrical requirements for supply voltages are described in the JODY-W2 series data sheet [2].

Rail	Allowable Ripple (peak to peak)[2] over DC supply			Current consumption, peak
	10-100 kHz	100 kHz-1 MHz	>1 MHz	
VBAT (3.3 V)	65 mV_{pk-pk}	25 mV_{pk-pk}	10 mV_{pk-pk}	0.8 A
VIO + 1V8	65 mV_{pk-pk}	25 mV_{pk-pk}	10 mV_{pk-pk}	300 mA + sink current to other devices

Table 5: Summary of voltage supply requirements

JODY-W2 series modules are powered by one of the following DC supplies:

- Switching Mode Power Supply (SMPS)
- Low Drop Out (LDO) regulator

The SMPS is the ideal choice when the available primary supply source has significantly higher value than the operating supply voltage of the JODY-W2 series modules. The use of SMPS provides the best power efficiency for the overall application and minimizes current drawn from the main supply source.

⚠ When choosing the SMPS, ensure that the AC voltage ripple at switching frequency does not exceed the requirements as specified in Table 5. The use of an LDO linear regulator is convenient for a primary supply with a relatively small difference to the supply voltage where the typical 85-90% efficiency of the switching regulator leads to minimal current saving. Linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy.

Independent of the selected DC power supply, it is crucial that it can handle the high peak current generated by the module. A margin of at least 20% over the specified peak current is recommended when designing the power supply for the module.

1.3 System function interfaces

1.3.1 Power-up sequence

The module power-up sequence can be initiated by applying the respective voltage to the **VBAT/VIO/1V8** supply pins and deasserting **PDn** (logic level 1) and **CORE_PDn** (logic level 1). Firmware download is required every time **PDn** and **CORE_PDn** signals are asserted. It is advisable to tie **PDn** and **CORE_PDn** together.

JODY-W2 includes an internal SMPS voltage generator followed by an internal LDO which generates the supply voltage to the supply nodes of the internal ASIC.

Figure 4 shows the recommended power-up sequence of the module. With **VIO** set to **3.3V, VIO** must be applied before **VBAT**. With **VIO** set to **1.8 V,** the order of **VIO** and **VBAT** does not matter. Once the internal Switched Mode Power Supply (SMPS) has stabilized to 90% (taking up to 1.15 ms), **1V8** can be applied followed by the de-assertion of **PDn** and **CORE_PDn.**

PG is an open-drain output used to sense when the internal DC/DC has stabilized. The output is set in a high-impedance state when the internal voltage is "good". An external 100 kΩ pull-up resistor must be connected to **PG** to ensure that the signal is in an affirmative logic-high level. A low-level state indicates that the power is “not good”. External power-up logic can monitor the transition of **PG** to high or wait at least 1.15 ms before applying 18V and continuing the power-up sequence.

[2] Ripple measured on the power connectors of u-blox EVK.

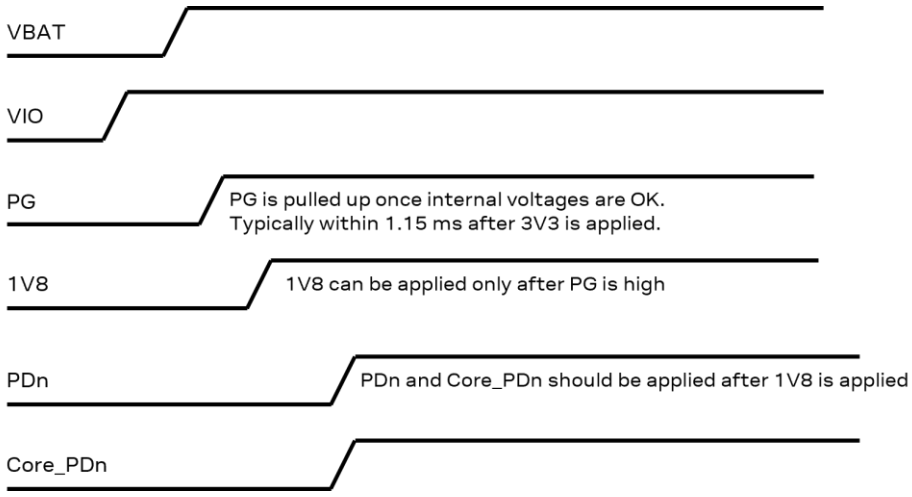


Figure 3: Power-up sequences for VIO=3.3 V or 1.8 V

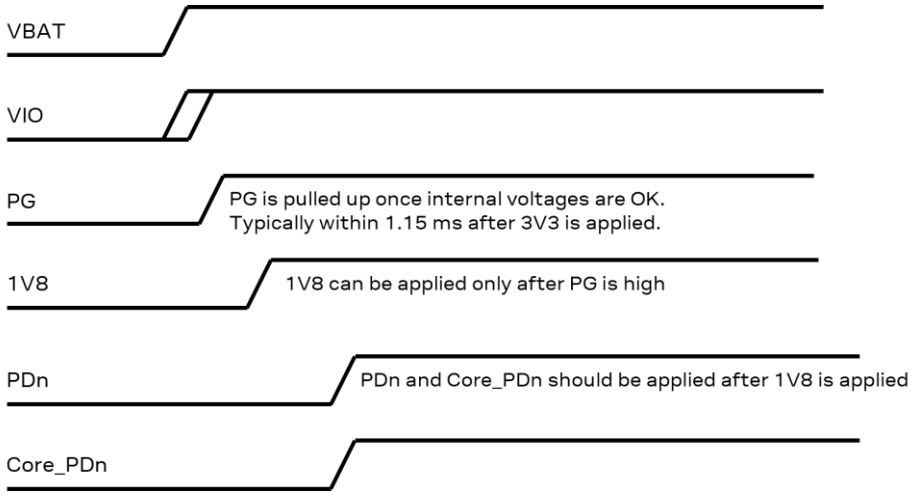


Figure 4: Optional power-up sequences for VIO=1.8 V

1.3.2 Reset

The internal power-up reset logic means that an external reset is not necessary for proper operation, although it can be used by the host controller through **PDn** and **CORE_PDn** in case of abnormal module behavior.

JODY-W2 is reset to its default operating state by any of the following events:

- Module is powered on and internal voltages are good
- Software or firmware reset
- Asserting **PDn** and **CORE_PDn**

1.3.3 Power-off sequence

It is advisable to ramp down **VBAT** followed by **1V8**. **PDn** must be asserted when powering down the module.

One of the following conditions must be met before Power-on Reset is triggered again:

- **PDn** and **CORE_PDn** asserted
- **PDn** asserted and **1V8** discharged to less than 0.2 V

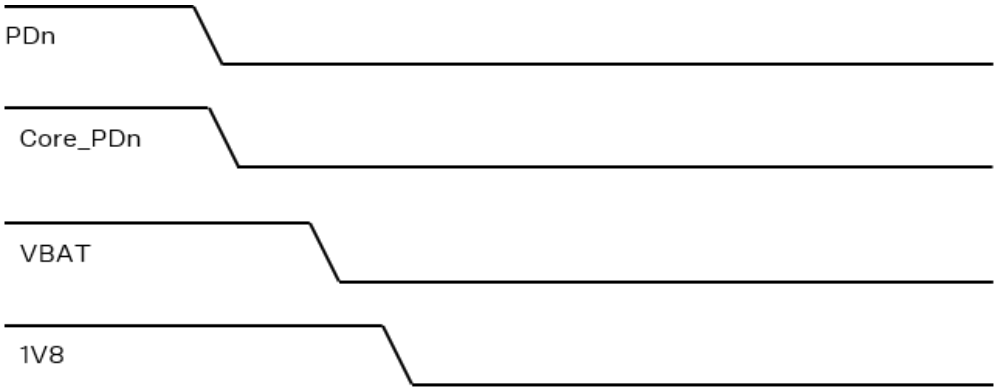


Figure 5: Power-down sequence of JODY-W2 module

1.3.4 Wake-up signals

JODY-W2 provides module-to-host, wake-up signals that are used to exit the host from any sleep mode over Wi-Fi or Bluetooth. The wake-up signals are powered by the **VIO** voltage domain.

Name	Module pin	Chipset GPIO	Description
HOST_WAKE	10	GPIO_1	Wi-Fi to host out-of-band wake-up signal (output)
GPIO_20	12	GPIO_20	Bluetooth to host out-of-band wake-up signal (output)
PCM_IN	18	GPIO_4	Alternative Bluetooth to out-of-band wake-up signal if PCM is not used (output)

Table 6: Wake-up signal definition

1.3.5 Configuration pins

Two dedicated boot-strap configuration pins (**CONFIG[0]**, **CONFIG[1]**) determine the configuration of the host interface after system reset. Additional multiplexed pins (**PCM_OUT**, **LTE_COEX_TX**, **BT_UART_TX**, **BT_UART_RTS**) are used as configuration inputs following a reset and revert to their normal function immediately after system reset.

By default, the configuration pins are high at logic level 1, unless otherwise noted. A 100 kΩ pull down resistor to ground is required to set the pins low. No external circuitry is required to set a configuration pin to a high level.

Table 7 describes the boot-strap configuration options that are set by **CONFIG[0]** and **CONFIG[1]** pins and used to configure the host communication interfaces:

- **SDIO-UART:** Wi-Fi commands and data are transferred through the SDIO bus to the module. The high-speed UART interface is used for Bluetooth communication.
- **SDIO-SDIO:** Wi-Fi and Bluetooth communication are transferred through the SDIO interface.

CONFIG[1]	CONFIG[0]	Wi-Fi	Bluetooth	Firmware download	Number of SDIO functions
1	0	SDIO	UART	SDIO+UART (parallel/Serial)	1 (Wi-Fi)
1	1	SDIO	SDIO	SDIO+SDIO (parallel/Serial)	2 (Wi-Fi, Bluetooth)

Table 7: Host interface configuration options

Additional configuration pins must be set to their pre-requisite states following a reset as shown in Table 8. The Internal PU/PD sets the default logic level if the pin is not connected to any external component.

Name	Pin	Description	Internal PU/PD
PCM_OUT	17	Shall be set high during reset	Weak PU
BT_UART_RTS	38	Shall be set high during reset	Weak PU

Name	Pin	Description	Internal PU/PD
LTE_COEX_TX	13	Shall be set high during reset	Weak PU
BT_UART_TX	36	Shall be set low during reset	A 51 kΩ pull-down resistor is implemented on the module.

Table 8: Additional configuration pins

1.4 Data communication interfaces

JODY-W2 series modules use SDIO 3.0 and high-speed UART as host interface. The Wi-Fi traffic is always communicated through the SDIO host interface. Depending on the configuration, the high-speed UART interface can be configured for the Bluetooth/Bluetooth LE traffic between the host and the JODY-W2 module series.

⚠ Use of the high-speed UART interface is only possible with the SDIO-UART software package. The SDIO-SDIO software package supports only the SDIO host interface.

1.4.1 SDIO 3.0 interface

JODY-W2 series modules include a SDIO device interface compatible with the industry standard SDIO 3.0 specification (UHS-I, up to 104 Mbyte/s) and allows a host controller using the SDIO bus protocol to access Wi-Fi and Bluetooth functions. The modules also support legacy modes, such as default speed and High-Speed modes.

☞ The SDIO signal voltage is fixed to 1.8 V for Default Speed and High-Speed modes.

A module acts as a device on the SDIO bus. Table 9 summarizes the bus speed modes supported by the module.

Bus Speed Mode	Max. Bus Speed [MB/s]	Max. Clock Frequency [MHz]	Signal Voltage (1V8) [V]
SDR104	104	208	1.8
SDR50	50	100	1.8
DDR50	50	50	1.8
SDR25	25	50	1.8
SDR12	12.5	25	1.8
High Speed	25	50	Only supported at 1.8 V
Default Speed	12.5	25	Only supported at 1.8 V

Table 9: SDIO supported rates for JODY-W2

Pull-up resistors are required for all SDIO data and command lines. These pull-up resistors can be provided either externally on the host PCB or internally in the host application processor. JODY-W2 includes programmable internal PU/PD. Depending on the routing of the SDIO lines on the host, termination resistors in series to the traces might also be needed. This to improve signal integrity or reduce EMC radiation. See also Data communication interfaces.

Name	I/O	Description	Remarks
SD_CLK	I	SDIO Clock input	
SD_CMD	I/O	SDIO Command line	Pull-up resistors are required
SD_D0	I/O	SDIO Data line bit [0]	Pull-up resistors are required
SD_D1	I/O	SDIO Data line bit [1]	Pull-up resistors are required
SD_D2	I/O	SDIO Data line bit [2]	Pull-up resistors are required
SD_D3	I/O	SDIO Data line bit [3]	Pull-up resistors are required

Table 10: SDIO signal definition

The SDIO host interface pins of the module are powered by the **1V8** voltage domain.

1.4.2 High Speed UART interface

The JODY-W2 series modules support a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface in compliance with the industry standard 16550 specification. The main features of the UART interface are:

- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit and receive operations
- Two flow control pins (RTS/CTS)
- Interrupt triggers for low-power, high throughput operation
- Supports standard baud rates and high throughput up to 4 Mbit/s. The default baud rate after reset is 3000000 baud.

The UART interface operation includes:

- Uploading the firmware to the module
- Bluetooth data

Name	I/O	Description	Remarks
BT_UART_TX	O	UART TX signal	Connect to Host RX. Used as configuration pin. See also Configuration pins.
BT_UART_RX	I	UART RX signal	Connect to Host TX
BT_UART_RTS	O	UART RTS signal	Connect to Host CTS. Used as configuration pin. See also Configuration pins.
BT_UART_CTS	I	UART CTS signal	Connect to Host RTS

Table 11: UART signal description

High Speed UART signals are powered by the **VIO** voltage domain.

1.4.3 PCM - Audio interface

JODY-W2 series modules provide one bi-directional 4-wire PCM digital audio interface that can be used for digital audio communication with external digital audio devices as an audio codec. The PCM interface supports:

- Master or slave mode
- PCM bit width size of 8 bit or 16 bit
- Up to 4 slots with configurable bit width and start positions
- Short frame and long frame synchronization

Name	I/O	Description	Remarks
PCM_CLK	I/O	PCM clock	Output if Master, Input if Slave
PCM_SYNC	I/O	PCM frame sync	Output if Master, Input if Slave
PCM_IN	I	PCM data in	
PCM_OUT	O	PCM data out	Used as configuration pin. See also Configuration pins.

Table 12: PCM digital audio signal description

The PCM signals are powered by the VIO voltage domain.

1.4.4 Low power oscillator

For professional grade modules, an optional external low-frequency clock for low-power mode timing can be connected to the **LPO_IN** pin. The external LPO must meet the requirements listed in Table 14.

If no external sleep clock is used, leave this pin unconnected.

Name	I/O	Description	Remarks
LPO_IN	I	32.768 kHz clock input	Failsafe pin.

Table 13: External 32.768 kHz sleep clock signal description

LPO_IN is a failsafe input, clock signal that can be applied to the pin when the module is not powered and the requirements in Table 14 are fulfilled.

☞ Not applicable for automotive grade module variants.

Parameter	LPO clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 – 70	%
Input signal accuracy	200 – 3300	mV, pkpk
Signal type	Square-wave or Sine-wave	-
Input impedance[3]	> 100	kΩ
	< 5	pF
Clock jitter (during startup)	< 10,000	ppm

Table 14: External 32.768 kHz sleep clock specification

1.4.5 JTAG – Test Interface

A JTAG test interface is supported on chipset pins GPIO14–17. Table 15 shows the mapping between chipset and module pins.

Chip pin name	Module pin name	Supply domain	Description
GPIO_14	GPIO_14	VIO	JTAG_TCK test clock (Input)
GPIO_15	GPIO_15	VIO	JTAG_TMS controller select (Input)
GPIO_16	LTE_COEX_RX	VIO	UART_LTE_SIN / JTAG_TDI test data input (Input)
GPIO_17	LTE_COEX_TX	VIO	UART_LTE_SOUT / JTAG_TDO test data output (Output)

Table 15: JTAG signal mapping

1.5 Antenna interfaces

1.5.1 Wi-Fi and Bluetooth antennas

JODY-W2 provides two antenna pins, one for dual-band Wi-Fi connectivity (**ANT1**) and another for Bluetooth (**ANT0**). The following recommendations apply to developing an antenna interface for the JODY-W2 module:

- Where possible, consider integrating in the end product the u-blox reference design to minimize the effort on the certification process. For the full list of available reference designs, see the JODY-W2 antenna reference design, application note [15].
- The **ANT0** and **ANT1** pins of JODY-W2 have a nominal characteristic impedance of 50 Ω and must be connected to the external antennas through a 50 Ω transmission line to allow proper RF transmission and reception.
- Good isolation must be provided between the various antennas in the system. Special care shall be taken to maximize isolation between the antennas operating in the same or nearby bands.

For information describing how to properly design circuits compliant with these requirements, see Antenna interfaces.

[3] When power is applied or switched off.

1.5.2 Approved antenna designs

JODY-W2 modules come with a pre-certified design that can be used to save costs and time during the certification process. To minimize this effort, the customer is required to implement antenna layout according to u-blox reference designs. Reference design source files can be provided on request by u-blox.[4]

For Bluetooth and Wi-Fi operation, the module has been tested and approved for use with the antennas listed in the JODY-W2 series data sheet [2]. The module may be integrated with other antennas. In this case, the OEM installer must certify his design with respective regulatory agencies.

1.6 Other remarks

1.6.1 Unused pins

☞ JODY-W2 modules have pins that are reserved for future use (**NC**). These pins must be left unconnected on the application board.

1.6.2 GPIO usage

☞ The reconfiguration of signals marked as GPIOs on the JODY-W2 module for applications not listed in this document depends on the respective firmware release.

[4] Reference design will be available after certification.

2 Design-in

2.1 Overview

For an optimal integration of JODY-W2 series modules in the final application board, it is advisable to follow the design guidelines described in this chapter. Every application circuit must be properly designed to ensure that the related interface functions correctly, but several specific points require special attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

- Module antenna connection: **ANT0** and **ANT1** pins.

  Antenna circuit affects the RF compliance of the device integrating JODY-W2 modules with applicable certification schemes. For schematic and layout design recommendations, see also Antenna interfaces.

- Module supply: **VBAT**, **VIO/1V8**, and **GND** pins.

  The supply circuit affects the RF compliance of the device integrating JODY-W2 modules with applicable certification schemes. Follow the General high-speed layout guidelines.

- High speed interfaces: **SDIO** pins.

  High speed interfaces can be a source of radiated noise and can affect the compliance with regulatory standards for radiated emissions. Follow the General high-speed layout guidelines and recommendations for the SDIO 3.0 interface.

- System functions: **PDn** and pins described as Configuration pins.

  Accurate design is required to ensure that the voltage level is well defined during module boot. Follow the General high-speed layout guidelines.

- Other pins: High speed **UART**, **PCM**, **specific signals** and **NC** pins.

  Accurate design is required to ensure proper functionality. Follow the General high-speed layout guidelines and recommendations for the High-speed UART interface.

2.2 Antenna interfaces

JODY-W2 modules provide the following two RF interfaces for connecting the external antennas:

- The **ANT0** port for Bluetooth connectivity.
- The **ANT1** port for Wi-Fi connectivity.

Both the **ANT0** and the **ANT1** ports have a nominal characteristic impedance of 50 Ω and must be connected to the related antenna through a 50 Ω transmission line to allow proper impedance matching along the RF path. A bad termination of the **ANT0** pin (Bluetooth) or the **ANT1** pin (Wi-Fi) may result in poor performance of the module.

For the dual antenna modules, the isolation between the two antennas should be maximized, the requirements specified in Table 16 and Table 17 should be followed to ensure good performance.

⚠ According to FCC regulations, the transmission line from the antenna pin in the module to the antenna or antenna connector on the host PCB is considered part of the approved antenna design. Consequently, module integrators must either follow exactly one of the antenna reference design used in the module's FCC type approval or certify their own designs. See also the JODY-W2 antenna reference design [15].

2.2.1 RF transmission line design

RF transmission lines such as the ones from the **ANT0** and **ANT1** pins up to the related antenna connectors must be designed so that the characteristic impedance is as close as possible to 50 Ω.

Figure 6 shows the design options for implementing a transmission line, namely:

- Microstrip – track separated with dielectric material and coupled to a single ground plane.
- Coplanar microstrip – track separated with dielectric material and coupled to both the ground plane and side conductor. This in the most common transmission line implementation.
- Stripline – track separated by dielectric material and sandwiched between two parallel ground planes.

The parameters shown in the cross-sectional area of each trace design include:

- Width (W) – shows the width of the copper layer on the top layer
- Distance (S) – shows the distance between the top copper layer and the two adjacent GND planes.
- Dielectric substrate thickness (H) – shows the distance between the GND reference on the bottom plane and the copper layer on the top layer.
- Thickness of the copper layer (T) – can also be represented by "Base Copper Weight", which is commonly used as the parameter for PCB stack-up.
- Dielectric constant (ε_r) defines the ratio between the electric permeability of the material against the electric permeability of free space.

☞ The width of a 50 Ω microstrip depends on "ε_r" and "H", which must be calculated for each PCB layer stack-up.

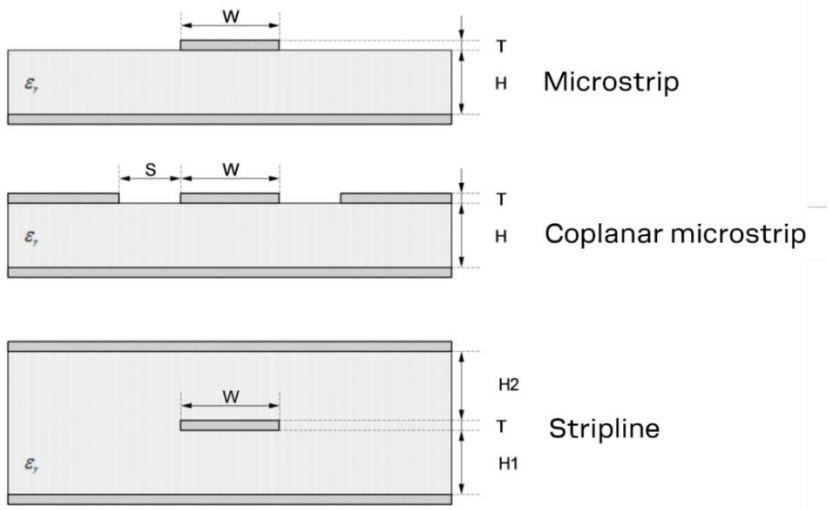


Figure 6: Transmission line trace design

Follow these recommendations to design a 50 Ω transmission line correctly:

- Designers must provide enough clearance from surrounding traces and ground in the same layer. In general, the trace to ground clearance should be at least twice that of the trace width. The transmission line should also be "guarded" by the ground plane area on each side.
- In the first iteration, calculate the characteristic impedance using tools provided by the layout software. Ask the PCB manufacturer to provide the final values usually calculated using dedicated software and production stack-ups. It is sometimes possible to request an impedance test coupon on side of the panel to measure the real impedance of the traces.

- Although FR-4 dielectric material can result in high losses at high frequencies, it can still be an appropriate choice for RF designs. In which case, aim to:
  - Minimize RF trace lengths to reduce dielectric losses.
  - If traces longer than few centimeters are needed, use a coaxial connector and cable to reduce losses.
  - For good impedance control over the PCB manufacturing process, design the stack-up with wide 50 Ω traces with width of at least 200 µm.
  - Contact the PCB manufacturer for specific tolerance of controlled impedance traces. As FR-4 material exhibits poor thickness stability it gives less control of impedance over the trace width.
- For PCBs with components larger than 0402 and dielectric thickness below 200 µm, add a keep-out, that is, some clearance (void area) on the ground reference layer below any pin on the RF transmission lines. This helps to reduce the parasitic capacitance to ground.
- Route RF lines in 45 ° angle and avoid acute angles. The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible..
- Add GND stitching vias around transmission lines as shown in Figure 7.
- Provide a sufficient number of vias on the adjacent metal layer, as shown in Figure 7. Include a solid metal connection between the adjacent metal layer on the PCB stack-up to the main ground layer.
- To avoid crosstalk between RF traces and Hi-impedance or analog signals, route RF transmission lines as far from noise sources (like switching supplies and digital lines) and any other sensitive circuit.
- Avoid stubs on the transmission lines. Any component on the transmission line should be placed with the connected pin located over the trace. Also avoid any unnecessary components on RF traces.

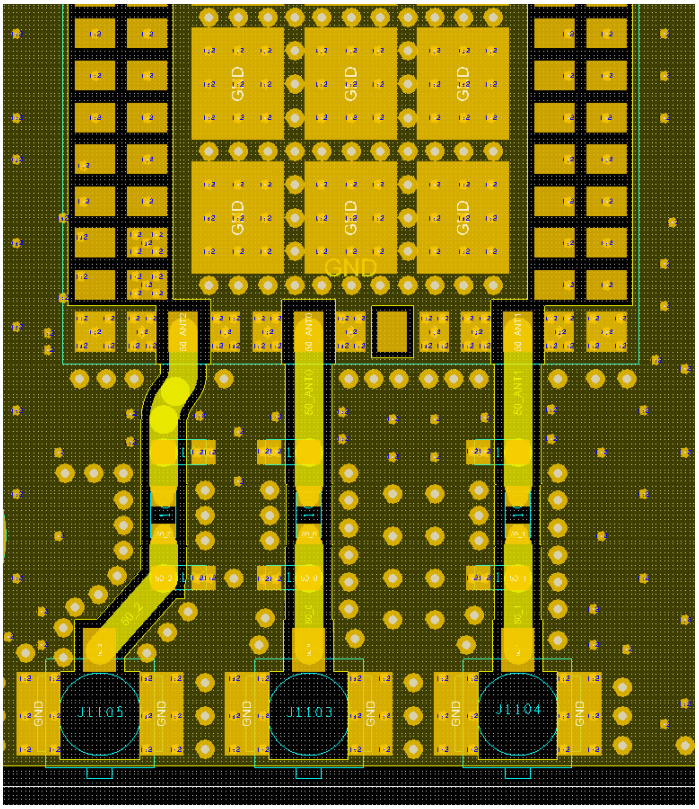


Figure 7: Example of RF trace and ground design from JODY-W2 EVK

2.2.2 Antenna design

Designers must take care of the antennas from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating JODY-W2 module with all the applicable required certification schemes heavily depends on antennas radiating performance.

- External antennas such as linear monopole:
  - External antennas basically do not imply physical restriction to the design of the PCB where the module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected with minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces radiation performance.
  - A high quality 50 Ω coaxial connector provides proper PCB-to-RF-cable transition.
- Integrated antennas such as patch-like antennas:
  - Internal integrated antennas imply physical restriction to the PCB design:
    - Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane related to the antenna element must be considered.
    - The RF isolation between antennas in the system must be as high as possible and the correlation between the 3D radiation patterns of the two antennas has to be as low as possible.
    - In general, an RF separation of at least a quarter wavelength between the two antennas is required to achieve a minimum isolation and low pattern correlation; increased separation should be considered, if possible, to maximize the performance and fulfil the requirements in Table 17.
    - A numerical example for estimating the physical restrictions on a PCB is given here: Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.5 cm
  - Radiation performance depends on the whole product and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.

Table 16 summarizes the requirements for the antenna RF interface while Table 17 specifies additional requirements for dual antenna design implementation.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of Antenna pins.
Frequency range	2400 - 2500 MHz 5150 - 5850 MHz	For 802.11b/g/n and Bluetooth. For 802.11a/n/ac.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the primary antenna RF connection matches the 50 Ω characteristic impedance of antenna pins. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of antenna pins over the operating frequency range, to maximize the amount of power transferred to the antenna.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits.
Maximum gain		The maximum antenna gain must not exceed the value specified in type approval documentation to comply with regulatory agencies radiation exposure limits.

Table 16: Summary of antenna interface requirements

Item	Requirements	Remarks
Isolation (in-band)	S_{21} > 30 dB recommended	The antenna-to-antenna isolation is the S_{21} parameter between the two antennas in the band of operation. Lower isolation might be acceptable depending on use-case scenario and performance requirements.
Isolation (out-of-band)	S_{21} > 35 dB recommended S_{21} > 30 dB acceptable	Out-of-band isolation is evaluated in the band of the aggressor to ensure that the transmitting signal from the other radio is sufficiently attenuated by the receiving antenna to avoid saturation and intermodulation effect at the receiver's port.

Table 17: Summary of Wi-Fi/Bluetooth coexistence requirements

⚠ In dual antenna configuration, a good isolation is critical to achieve optimal throughput performance in Wi-Fi/Bluetooth coexistence mode while operating in the same 2.4 GHz band.

In both the cases, while selecting external or internal antennas, observe the following recommendations:

- Select antennas that provide an optimal return loss (or VSWR) over all operating frequencies.
- Select antennas that provide optimal efficiency figure over all operating frequencies.
- Select antennas that provide appropriate gain not to exceed the regulatory limits specified in some countries like the FCC in the United States.

A method to design for antenna micro-strip evaluation is to place an U.FL connector close to the embedded PCB or chip Antenna. The UFL connector needs only to be mounted on units used for verification.

2.2.2.1 RF connector design

If an external antenna is required, the designer should consider using a proper RF connector. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Table 18 suggests some RF connector plugs that can be used by the designers to connect RF coaxial cables based on the declaration of the respective manufacturers. The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitable mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	

Table 18: U.FL compatible plug connector

Typically, the RF plug is available as a cable assembly. Different types of cable assembly are available; the user should select the cable assembly best suited to the application. The key characteristics are:

- RF plug type: select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Typically, from 0.8 mm to 1.37 mm. Thicker cables minimize insertion loss
- Cable length: Standard length is typically 100 mm or 200 mm; custom lengths may be available on request. Select shorter cables to minimize insertion loss.
- RF connector on the other side of the cable: for example another U.FL (for board-to-board connection) or SMA (for panel mounting)

SMT connectors are typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect U.FL connector to a more robust connector such as SMA fixed on panel.

☞ A de-facto standard for SMA connectors implies the usage of reverse polarity connectors (RP-SMA) on end-user accessible Wi-Fi and Bluetooth interfaces to increase the difficulty to replace the antenna with higher gain versions and exceed regulatory limits.

The following recommendations apply for proper layout of the connector:

- Strictly follow the connector manufacturer's recommended layout. Some examples are provided below:
  - SMA Pin-Through-Hole connectors require GND keep-out (clearance or void area) on all the layers around the central pin up to annular pins of the four GND posts.
  - U.FL surface mounted connectors require no conductive traces (that is, clearance, a void area) in the area below the connector between the GND land pins.
- If the RF pin size on the connector is wider than the microstrip, remove the GND layer beneath the RF connector to minimize the stray capacitance thus keeping the RF line 50 Ω. For example, the active pin of U.FL connector must have a GND keep-out at least on the first inner layer to reduce parasitic capacitance to ground.

2.2.2.2 Integrated antenna design

If integrated antennas are used, the transmission line is terminated by the antennas themselves. Follow the guidelines mentioned below:

- The antenna design process should start together with the mechanical design of the product. PCB mock-ups are useful in estimating overall efficiency and radiation path of the intended design during early development stages.
- Use antennas designed by an antenna manufacturer providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the related integrated antenna requirements. The ground plane of the application PCB may be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated, however overall antenna efficiency may benefit from larger ground planes. Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts such as metal objects or ferrite sheets as they may absorb part of the radiated power, shift the resonant frequency of the antenna or affect the antenna radiation pattern.
- It is highly recommended to strictly follow the specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning/matching to reach the target performance. It is recommended to plan measurement and validation activities with the antenna manufacturer before releasing the end-product to manufacturing.
- The receiver section may be affected by noise sources like hi-speed digital busses. Avoid placing the antenna close to busses as DDR or consider taking specific countermeasures like metal shields or ferrite sheets to reduce the interference.

Take care of interaction between co-located RF systems like LTE sidebands on 2.4 GHz band. Transmitted power may interact or disturb the performance of JODY-W2 modules where specific LTE filter is not present.

2.3 Supply interfaces

2.3.1 Module supply design

Though the GND pins are internally connected, it is recommended to connect all the available ground pins to solid ground on the application board as a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance. JODY-W2 modules must be sourced through **VBAT** and **VIO/1V8** pins with proper DC power supplies that comply with the requirements summarized in Table 5.

Good connection of the JODY-W2 series module power supply pins with DC supply source is required for accurate RF performance. Schematic guidelines for the supply design are summarized below:

- All power supply pins must be connected to an appropriate DC source.
- Any series component with Equivalent Series Resistance (ESR) greater than a few mΩ should be avoided. Only exceptions to this rule are ferrite beads used for DC filtering, however those parts should be used carefully to avoid instability of the DC/DC supply powering the module and are in general not required.
- A minimum bulk capacitance of 10 µF on **VBAT** rail is required close to the module to help filter current spikes from the RF section. The preferred choice is a ceramic capacitor with X7R or X5R dielectric due to low ESR/ESL. Special care should be taken in the selection of X5R/X7R dielectrics due to capacitance derating vs DC bias voltage.
- Additional bypass capacitors in the range of 100nF to 1µF on all supply pins are required for high frequency filtering. The preferred choice is a ceramic capacitor with X7R or X5R dielectric due to low ESR/ESL. The temperature characteristics shall also be considered where X7R is recommended up to 125 °C, X6R up to 105 °C, and X5R up to 85 °C. Smaller size bypass capacitors should be chosen for the manufacturing process to minimize ESL.

2.3.1.1 VCC supply circuit design using a switching regulator

It is recommended to use a Switching Mode Power Supply (SMPS) when the difference from the available supply rail to the **VBAT** rail allows significant power savings. For example, conversion of a 12 V or greater voltage supply to the nominal 3.3 V value for the **VBAT** supply.

The characteristics of the SMPS connected to the **VBAT** pin should meet the following prerequisites to comply with the module requirements summarized in Table 5.

- **Power capability:** The switching regulator together with any additional filter in front of the module must be capable of providing a voltage within the specified operating range. The regulator must be capable of delivering the specified peak current.
- **Low output ripple**: The switching regulator peak-to-peak Voltage ripple must not exceed the specified limits. This requirement applies both to voltage ripple generated by SMPS operating frequency and to high frequency noise generated by power switching.

PWM/PFM mode operation: It is preferable to select regulators with fixed Pulse Width Modulation (PWM) mode. Pulse Frequency Modulation (PFM) mode typically exhibits higher ripple and may affect RF performance. If power consumption is not a concern, PFM/PWM mode transitions should be avoided in favor of fixed PWM operation to reduce the peak-to-peak noise on voltage rails. Switching regulators with mixed PWM/PFM mode can be used provided that the PFM/PWM modes and transition between modes complies with the requirements.

2.3.1.2 Supply circuit design using a Low Drop-Out (LDO) linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VBAT** or **VIO/1V8** value is relatively low. The linear regulators provide acceptable efficiency when transforming a supply of less than 5 V to a voltage value within the normal operating range of the module. A linear regulator can be also considered to power the **VIO/1V8** section due to the low current requirements, especially if cascaded from a SMPS-generated low voltage rail.

The characteristics of the Low Drop-Out (LDO) linear regulator used to power the voltage rails must meet the following prerequisites to comply with the requirements summarized in Table 5.

- **Power capabilities**: The LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VBAT** or **VIO/1V8** pins within the specified operating range and must be capable of withstanding and delivering the maximum specified peak current while in connected mode.
- **Power dissipation**: The power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range. The worst-case junction temperature can be estimated as shown below:

  $T_{j,est} = (V_{in} - V_{out}) * I_{avg} * \theta_{ja} + T_a$

  Where: θ_{ja} is the junction-to-ambient thermal resistance of the LDO's package[5], I_{avg} is the current consumption of the given voltage rail in continuous TX/RX mode and T_a is the maximum operating temperature of the end product inside the housing.

[5] Thermal dissipation capability reported on datasheets is usually tested on a reference board with adequate copper area (ref. to JESD51). Junction temperature on a typical PCB may be higher than the estimated value due to the limited space to dissipate the heat. Thermal reliefs on pads also affect the capability of a device to dissipate the heat.

2.4 Data communication interfaces

2.4.1 SDIO 3.0

As the SDIO 3.0 bus in JODY-W2 modules can support a clock frequency up to 208 MHz, special care must be taken to minimize potential EMI issues and ensure that the signal integrity requirements are met. The signals should be routed with a single ended impedance of 50 Ω.

It is recommended to route all signals in the bus with the same length and have appropriate grounding in the surrounding layers; total bus length should also be minimized. The layout of the SDIO bus should be done so that crosstalk with other parts of the circuit is minimized providing adequate isolation between the signals, clock, and surrounding busses/traces.

Figure 8 shows the suggested application schematic for the SDIO bus in JODY-W2 modules.

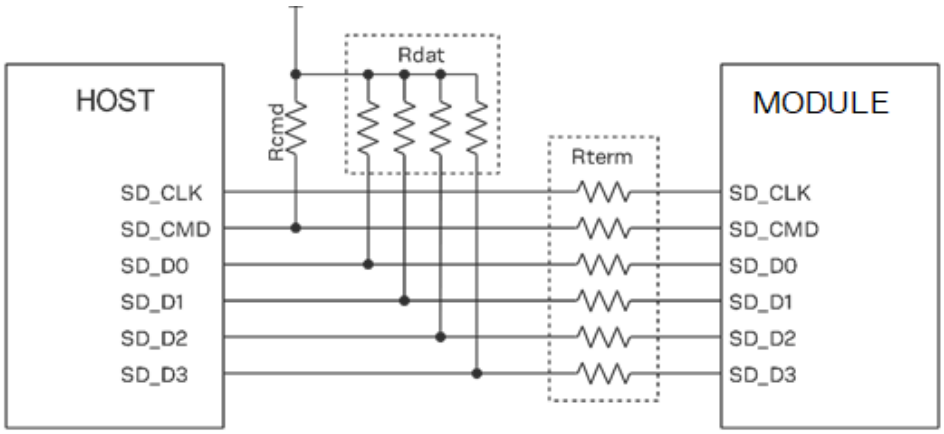


Figure 8: SDIO application schematic

☞ A small value capacitor in the range of few pF should be considered in parallel to **SDIO_CLK** as EMI debug option and signal termination. This capacitor should be placed as close as possible to the JODY-W2 clock input pin and can be assembled only for EMI purpose. The capacitor value adds to total line capacitance and must not exceed total allowed capacitance to avoid violating clock rise and fall timing specifications.

Table 19 summarizes the electrical requirements of the bus.

Signal Group	Parameter	Min.	Typ.	Max.	Unit
CLK, CMD, DAT[0:3]	Single ended impedance, Z_0		50		Ω
CLK, CMD, DAT[0:3]	Impedance control	$Z_0 - 10\%$	Z_0	$Z_0 + 10\%$	Ω
DAT[0:3]	Pull-Up range, Rdat	10	47	100	kΩ
CMD	Pull-Up range, Rcmd	10	10	50	kΩ
CLK, CMD, DAT[0:3]	Series termination (Host side), Rterm[6]	0	22		Ω
CLK, CMD, DAT[0:3]	Bus length[7]			100	mm
CMD, DAT[0:3]	Bus skew length mismatch to CLK	-3		+3	mm
CLK	Center to center CLK to other SDIO signals[8]	4*W			
CMD, DAT[0:3]	Center to center between signals[11]	3*W			

Table 19: SDIO bus requirements

[6] Series termination values larger than typical recommended only for addressing EMI issues.
[7] Routing should minimize the total bus length.
[8] Center to center spacing requirement can be ignored for up to 10 mm of routed length to accommodate BGA escape.

JODY-W2 series supports a 1.8 V SDIO interface only. A level shifter is needed to connect to a 3.3 V host CPU. An implementation of a level shifter is described in the JODY-W2 level shifter application note [12]. Further information about how to connect the SDIO interface on the EVK is described in EVK-JODY-W2 user guide [13].

2.4.2 High-speed UART interface

The high-speed UART interface for the JODY-W2 complies with the HCI UART Transport layer and uses the settings according to Table 20.

UART Settings	
baud rate default	3000000 Baud
Data bits	8
Parity bit	No parity
Stop bit	1 stop bit
Flow Control	RTS/CTS

Table 20: HCI UART Transport layer settings

Flow control with RTS/CTS is used to prevent temporary UART buffer overrun. It should not be used for flow control of HCI as HCI has its own flow control mechanisms for HCI commands, HCI events and HCI data.

- If CTS is 1, then the Host/Host Controller can send.
- If CTS is 0, then the Host/Host Controller is not allowed to send.

☞ It is mandatory to use the hardware flow control. Otherwise, JODY-W2 does not answer.

Baud rates				
1200	38400	460800	1500000	3000000 (default)
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	

Table 21: Possible baud rates for the UART interface

After loading the firmware, the baud rate is set to 3000000 baud. A host application can configure any desired baud shown in Table 21 using the dedicated HCI command:
`HCI_CMD_MARVELL_UART_BAUD`

```
hcitool -i hci0 cmd 0x3F 0x0009 <4 byte value for baudrate>
```

The command is generated completely at the old baud rate. Once the host receives the command at the old baud rate, it can switch to the new baud rate and should wait for 5 ms or more before sending the new command.

2.5 Other interfaces and notes

All pins have internal keeper resistors; leave it open if not used.

2.6 General high-speed layout guidelines

These general design guidelines are considered as best practices and are valid for any bus present in the JODY-W2 modules; the designer should prioritize the layout of higher speed busses. Low frequency signals are generally not critical for layout.

⚠ One exception is represented by High Impedance traces (such as signals driven by weak pull resistors) that may be affected by crosstalk. For those traces, a supplementary isolation of 4w from other busses is recommended.

2.6.1 General considerations for schematic design and PCB floor-planning

- Verify which signal bus requires termination and add series resistor terminations to the schematics.
- Carefully consider the placement of the module with respect to antenna position and host processor; RF trace length should be minimized first, followed by SDIO bus length.
- SDIO bus routing shall be planned to minimize layer-to-layer transition to a minimum.
- Verify with PCB manufacturer allowable stack-ups and controlled impedance dimensioning for antenna traces and busses.
- Verify that the power supply design and power sequence are compliant with JODY-W2 specification described in System function interfaces.

2.6.2 Component placement

- Accessory parts like bypass capacitors should be placed as close as possible to the module to improve filtering capability, prioritizing the placement of the smallest size capacitor close to module pins.
- Take care not to place components close to the antenna area. The designer should carefully follow the recommendations from the antenna manufacturer about the distance of the antenna vs. other parts of the system. The designer should also maximize the distance of the antenna to Hi-frequency busses like DDRs and related components or consider an optional metal shield to reduce interferences that could be picked up by the antenna thus reducing the module's sensitivity.

2.6.3 Layout and manufacturing

- Avoid stubs on high-speed signals. Test points or component pads should be placed over the PCB trace.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length; longer traces will degrade signal performance. Ensure that maximum allowable length for high-speed busses is not exceeded.
- Ensure to track your impedance matched traces. Consult early with your PCB manufacturer for proper stack-up definition.
- RF, analog and digital sections should have dedicated and clearly separated areas on the board.
- No digital routing is allowed in the GND reference plane area of RF traces (ANT pin and Antenna).
- It is strongly recommended to avoid digital routing beneath all layers of RF traces.
- Ground cuts or separation are not allowed below the module.
- Minimize the length of the RF traces, and then minimize the bus length to reduce potential EMI issues from digital busses.
- All traces (including low speed or DC traces) must couple with a reference plane (GND or power), Hi-speed busses should be referenced to the ground plane. In this case, if the designer needs to change the ground reference, an adequate number of GND vias must be added in the area of transition to provide a low impedance path between the two GND layers for the return current.
- Hi-Speed busses are not allowed to change reference plane. If a reference plane change is unavoidable, some capacitors should be added in the area to provide a low impedance return path through the different reference planes.
- Trace routing should keep a distance greater than 3w from the ground plane routing edge.
- Power planes should keep a distance from the PCB edge sufficient to route a ground ring around the PCB, the ground ring must then be connected to other layers through vias.

⚠ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application baseboard below the JODY-W2 series modules. Avoid placing temperature sensitive devices close to the module and provide adequate grounding to transfer the generated heat to the PCB.

2.7 Module footprint and paste mask

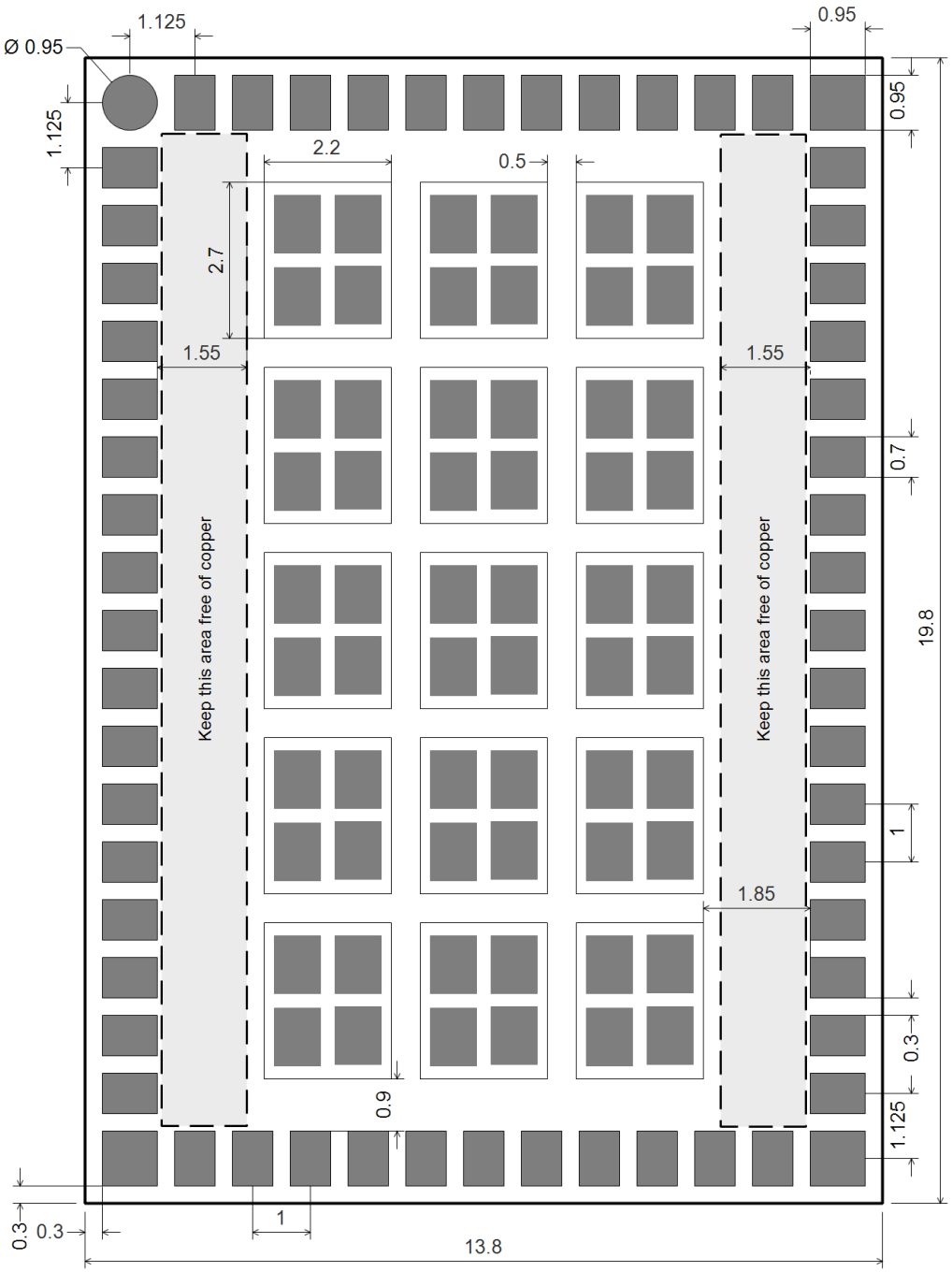


Figure 9: Recommended footprint for JODY-W2 module, top view (dimensions in mm, ±.05 mm)

⚠ Future variants of JODY-W2 can have more pins in the area enclosed with dotted lines. To ensure compatibility, keep this area free of copper.

Figure 9 describes the pin layout for the JODY-W2 series module. The proposed land pattern layout reflects the pin layout of the module. Both Solder Mask Defined (SMD) and Non Solder Mask Defined (NSMD) pins can be used, however the following considerations apply:

- Pins from 1 to 60 should be NSMD
- Inner pads must have a good thermal bonding to PCB ground planes to help spreading the heat generated by the module.
- If NSMD design is chosen for inner pads, thermal reliefs should be considered and 4 or 9 vias per pad must be added for heat sink. Those vias may require copper capping.
- If SMD design is chosen for inner pads, the land pattern can be flooded on a ground plane beneath the module and vias added around the pads for heat sinking.

The suggested stencil layout for the JODY-W2 module is to follow the copper pad layout exactly as described in Figure 9 for the outer pads, while the central pads should implement a special solder paste pattern with the following characteristics:

- Solder paste area should be split in several smaller parts, typically four to nine depending on copper pad area.
- Total solder paste area should cover about 50% to 60% of copper thermal pad area.
- Total solder paste area must not exceed 65% of copper thermal pad area.

Missing to consider solder paste optimization may lead to poor soldering quality in production. Figure 10 shows a suggested stencil opening implementation.

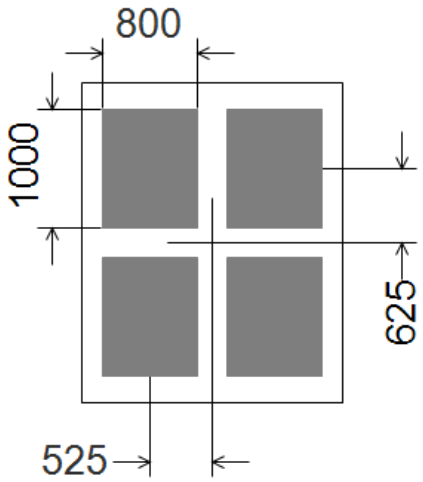


Figure 10: Stencil opening example for inner thermal pads (dimensions in µm)

⚠ The exact mask geometries, distances and stencil thicknesses must be adapted to the specific production process of the customer.

2.8 Thermal guidelines

JODY-W2 series modules have been successfully tested from -40 °C to +85 °C (or -40 °C to +105 °C for JODY-W263-01A) at an ambient temperature inside the enclosure box. The board will generate heat during high loads that must be dissipated to sustain the lifetime of the components.

The improvement of thermal dissipation in the module decreases its internal temperature and consequently increases the long-term reliability of the device for applications operating at high ambient temperatures.

For best performance, consider the following guidelines when designing the layout:

- Vias specification for ground filling: $300/600\mu m$, no thermal reliefs are allowed on vias.
- Ground vias density under the module: $50\ vias/cm^2$, thermal vias can be placed in gaps between module's thermal pads.
- Minimum layer count and copper thickness: $4\ layers$, $35\ \mu m$.
- Minimum board size: $55x70\ mm$.
- Power planes and signal traces should not cross the layers beneath the module to maximize heat flow from the module.

Those recommendations allow the design to achieve a thermal characterization parameter of $\psi_{JB} = 15.0\ °C/W$, where JB refers to the "module's junction to main PCB bottom side".

The following additional hardware techniques can be used to improve the thermal performance of the module in customer's applications:

- Maximize antenna's return loss to reduce reflected RF power to the module.
- Improve the efficiency and the thermal design of any component that generates heat in the application, including power supplies and processor, to spread the generated heat distribution over the application device.
- Properly design the mechanical enclosure of the application device to provide ventilation and good thermal dissipation.
- For continuous operation at high temperatures, high power density applications or reduced PCB size, the designer may consider a heat sink on main PCB's bottom side, connected through electrically insulated / high thermal conductivity adhesive[9].

2.9 ESD guidelines

JODY-W2 module is manufactured through a highly automated process, which complies with IEC61340-5-1 [6] (STM5.2-1999 Class M1 devices) standard. A manufacturing process on customer's manufacturing site that implements a basic ESD control program is considered sufficient to satisfy the necessary precautions[10] for handling the modules. The ESD ratings of JODY-W2 module pins are stated in the JODY-W2 series data sheet [2].

In compliance with the following European regulations, the designer must implement proper measures to protect from ESD events on any pin that may be exposed to the end user:

- ESD testing standard CENELEC EN 61000-4-2 [4]
- Radio equipment standard ETSI EN 301 489-1 [5]

The minimum requirements for conformance to these European regulations are summarized in Table 22.

Application	Category	Immunity level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration of the end product.	Contact Discharge	4 kV
	Air Discharge	8 kV

Table 22: Minimum ESD immunity requirements based on EN 61000-4-2

Compliance with standard protection level as specified in EN 61000-4-2 [5] can be achieved by including proper ESD protections in parallel to the line, close to areas accessible by the end user.

[9] Typically not required.
[10] Minimum ESD protection level for safe handling is specified in JEDEC JEP155 (HBM) and JEP157 (CDM) for ±500 V and ±250 V respectively.

⚠ Special care should be taken if the **ANT0** and **ANT1** pins must be protected by choosing an ESD absorber with adequate parasitic capacitance. For 5 GHz operation, a protection with maximum internal capacitance of 0.1 pF is recommended.

2.10 Design checklist

2.10.1 Schematic checklist

- ☐ JODY-W2 module pins are properly numbered and designated on the schematic (including thermal pins).
- ☐ Power supply design complies with the specification.
- ☐ The power sequence is properly implemented.
- ☐ Adequate bypassing is present in front of each power pin.
- ☐ Each signal group is consistent with its own power rail supply or proper signal translation has been provided.
- ☐ Configuration pins are properly set at bootstrap.
- ☐ SDIO bus includes series resistors and pull-ups.
- ☐ Unused pins are properly terminated.
- ☐ A pi-filter is provided in front of each antenna for final matching.
- ☐ RF co-location additional filters have been considered in the design.

2.10.2 Layout checklist

- ☐ PCB stack-up and controlled impedance traces follow PCB manufacturer's recommendation.
- ☐ All pins are properly connected, and the package follows u-blox recommendations for pin design.
- ☐ Proper clearance has been provided between the RF and digital sections.
- ☐ Proper isolation has been provided between Antennas (RF co-location, diversity, or multi-antenna design).
- ☐ Bypass capacitors are placed close to the module.
- ☐ Low impedance power path has been provided to the module.
- ☐ Controlled impedance traces are properly implemented on the layout (both RF and digital) and follow PCB manufacturer recommendations.
- ☐ 50Ω RF traces and connectors follow the rules described in Antenna interfaces.
- ☐ Antenna design has been reviewed by the antenna manufacturer.
- ☐ The module has proper grounding for low impedance return path and heat sink.
- ☐ Reference plane skipping has been minimized for high frequency busses.
- ☐ All traces and planes are routed inside the area defined by the main ground plane.
- ☐ u-blox has reviewed and approved the PCB[11].

[11] This is applicable only for end-products based on u-blox reference designs.

3 Software

The instructions in this chapter describe how to set up the JODY-W2 series module on a Linux operating system. Including several examples, it also describes how the reference driver packages are compiled and deployed in the target system.

The described configuration is based on the proprietary driver supported on kernel version 3.10.40 that has been integrated onto an Apalis TK1 development board from Toradex. The board connects to the JODY-W2 series module through the SDIO host interface and uses a USB-to-UART adapter to connect to the Bluetooth UART resident in the module.

☞ The Proprietary drivers, developed by NXP and distributed by u-blox, are only made available to customers that have signed a limited use license agreement (LULA) [1] with u-blox. A valid non-disclosure agreement (NDA) is mandatory to get the driver packages directly from NXP.

☞ Open-source drivers for mainstream use are made available free of charge by NXP and are already pre-integrated into the Linux BSPs for the NXP i.MX application processors and the MCUXpresso SDK for selected NXP MCU devices. See also Open-source Linux/Android drivers and MCUXpresso SDK.

3.1 Available software packages

3.1.1 Open-source Linux/Android drivers

JODY-W2 series modules are based on the NXP 88W8987 chipset. The drivers and firmware required to operate JODY-W2 series modules are developed by NXP and are already integrated into the Linux BSP for the NXP i.MX application processors [16].

The documentation for the software releases from NXP contains Wi-Fi and Bluetooth release notes and a list of supported software features. The driver source code is provided free of charge as open source under NXP license terms. Being open source allows the drivers to be integrated or ported to other non-NXP based host platforms. Yocto recipes for the driver and firmware, that can be used to develop custom Linux-based systems, are part of the NXP i.MX Linux BSP.

The latest version of the driver source code and Wi-Fi/Bluetooth firmware are available from the following open-source repositories:

- Wi-Fi driver: https://github.com/nxp-imx/mwifiex
- Firmware: https://github.com/NXP/imx-firmware
- i.MX meta-layer: https://github.com/nxp-imx/meta-imx
  - ./meta-bsp/recipes-connectivity/nxp-wlan-sdk
  - ./meta-bsp/recipes-kernel/kernel-modules/kernel-module-nxp89xx.bb
  - ./meta-bsp/recipes-kernel/linux-firmware/linux-firmware_%.bbappend

☞ Use the repository branches matching to the latest Linux BSP release version. At the time of publication, this is release 6.1.1_1.0.0.

The Wi-Fi driver uses the TCP/IP stack from the Linux kernel for data transmission and the `cfg80211` subsystem in the kernel for configuration and control. The `hci_uart` driver from the Linux kernel and BlueZ host stack are used for the Bluetooth part. For further information about initialization and configuration of the Wi-Fi and Bluetooth features, see also the NXP User Manual UM11490 [17].

3.1.2 MCUXpresso SDK

The MCUXpresso SDK is a comprehensive software enablement package for MCU devices from NXP. It includes production-grade software with optionally integrated real-time operation systems (RTOS), integrated enabling software technologies (stacks and middleware), reference software, and more. The SDK includes the Wi-Fi and Bluetooth drivers and firmware for JODY-W2 series modules for supported NXP MCUs. MCUXpresso Wi-Fi/Bluetooth support for NXP 88W8987 chipset in JODY-W2 is currently available for FreeRTOS™ real-time operation system.

3.1.3 Proprietary drivers

JODY-W2 modules can be operated in SDIO-UART or SDIO-SDIO mode. Each operation mode must use a dedicated host driver.

Two following proprietary driver variants are available:

- SDIO-UART (SD-WLAN-UART-BT-8987-XX): this package is needed for using SDIO for Wi-Fi and UART for Bluetooth.
- SDIO-SDIO (SD-WLAN-SD-BT-8987-XX): this package is needed for using SDIO host interface for both radios.

NXP provides two package variants:

- XX-MGPL: source code with GPLv2 license
- XX-GPL: source code with proprietary license

For further information about license usage, refer to the README file in the driver package. See also Driver package structure.

3.2 Supported kernel versions

Due to constant changes in the kernel subsystem APIs for different kernel releases, the driver must be modified for each major and minor kernel release.

The proprietary driver packages have been verified on the following platforms and kernel versions only:

Platform	SoC	Kernel Version
i.MX 8MQ EVK	i.MX8M (NXP)	5.4.24, 4.14.98
i.MX 6SoloX Sabre board	i.MX6 SoloX (NXP)	5.4.24, 4.1.15
Ixora Apalis TK1 (Toradex AG)	NVIDIA Tegra K1 (NVIDIA)	4.14.90, 3.10.40

Table 23: Tested Linux kernel versions for the JODY-W2 modules reference drivers

The supplied software package supports Linux kernel from 2.6.32 to 5.5.2. If there is no change in the kernel API, it can also support the latest kernel versions. If there are any changes to the kernel APIs you choose to use, make the necessary changes using patches. In case of any discrepancy, contact the respective support team in your region.

The current driver is tested with Linux kernel version 4.14.98 on Android 9 and 5.4 on Android 10 and 11. For detailed instructions and procedures, refer to the application note [11].

3.3 Driver package structure

The NXP driver packages include different components, depending on the supported host interfaces. The content of the packages is described in Table 24.

Component	Content folder	Explanation
Release Notes	N/A	This document describes all the supported features, specific changes made in the release and known issues.
FwImage	FwImage	Binary firmware images. See also Firmware.
SD-app-src.tgz	wlan_src/mapp	Source code for the NXP proprietary applications needed for setting up different modes to operate in Wi-Fi.
SD-src.tgz	wlan_src/mlinux	Source code for the proprietary driver module sd8987.ko. This is the main holder for all the Makefiles and README.
SD-mlan-src.tgz	wlan_src/mlan	Source code for the driver module mlan.ko which implements functionality to interface with Linux network stack.
UART-src.tgz	muart_src	Source code for the proprietary driver Bluetooth HCI_UART driver module hci_uart.ko.
UART-FW-LOADER-src.tgz	uartfwloader_src	Source code for NXP application to download the Bluetooth only firmware over UART while using parallel mode.
SD-BT-src.tgz	mbt_src	Source code for the proprietary driver module bt8987.ko. The driver acts as a link between SDIO interface on host and firmware and binds to BlueZ.
SD-BT-CHAR-src.tgz	mbtc_src	Source code for the proprietary driver module mbt8987.ko, which exposes a character interface for use with other Bluetooth stacks.

Table 24: Components of NXP driver package

3.4 Software architecture

From the software point of view, JODY-W2 series modules contain on-board OTP memory with calibration parameters and MAC addresses. Consequently, the modules require a host-side driver and device firmware to run.

At startup and at every reset or power cycle, the host driver needs to download the firmware binary file to the module. The host driver interfaces the bus drivers with the upper layer protocol stacks of the operating system.

Figure 11 shows the different software components and upper layers required for the operation of the JODY-W2 series module.

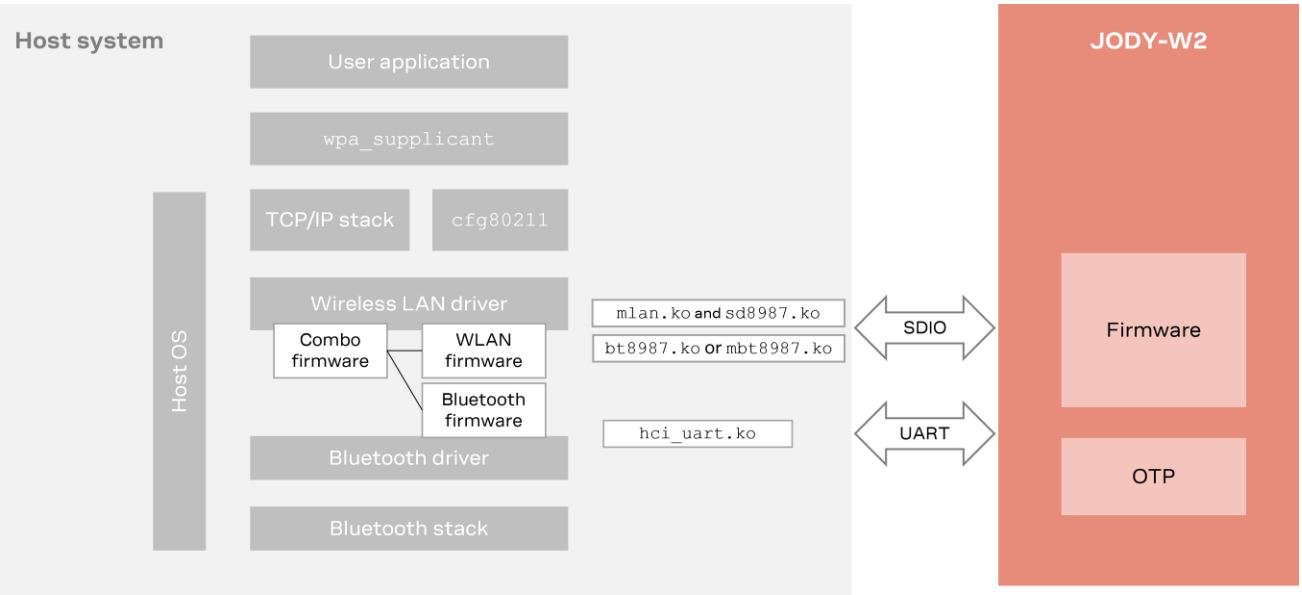


Figure 11: Basic software overview

3.4.1 Wi-Fi driver architecture

JODY-W2 module software includes a dedicated Wi-Fi reference driver that has both Wireless Extension (WEXT) and Netlink-based (nl80211/cfg80211) driver configuration interfaces.

Wi-Fi driver implementation is spread between the kernel modules, `sd8987` and `mlan`, where:

- `sd8987` implements the OS specific bindings. It provides an interface to kernel and protocol stack. It takes care of operations related to sockets, bus interface, IOCTLs, and so on.
- `mlan` is an OS independent module which handles chip-specific functions such as firmware downloading, command handling, data-path handling, power-save, and so on.

Figure 12 shows basic architecture of the Wi-Fi driver.

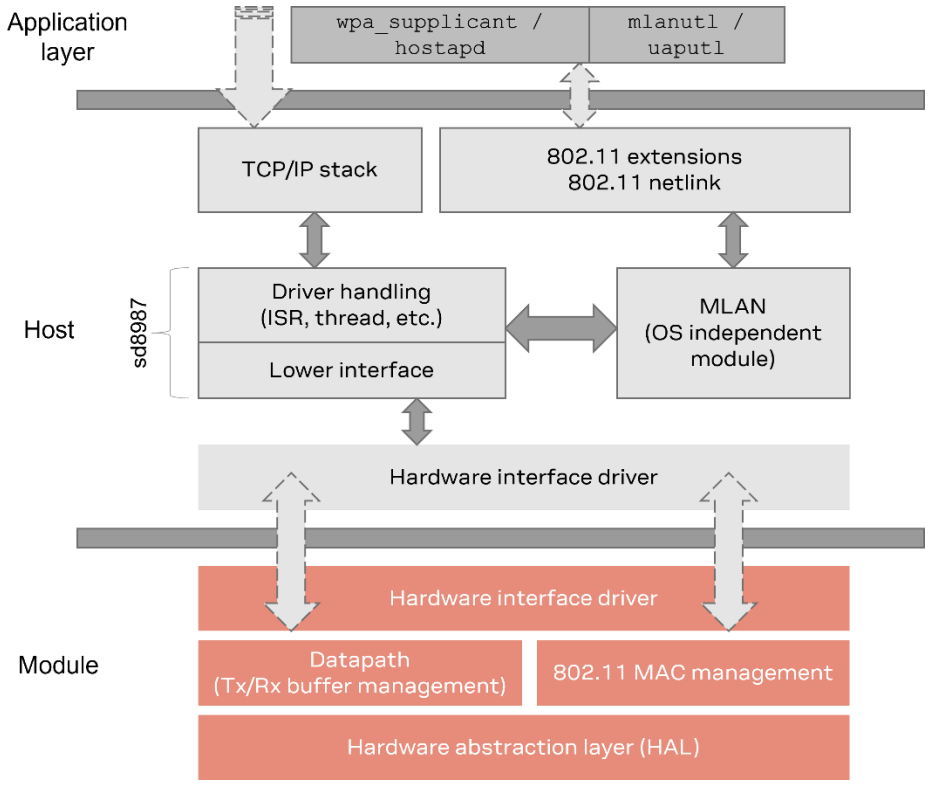


Figure 12: Basic Wi-Fi host driver and firmware architecture

3.4.2 Bluetooth driver architecture

The standard Bluetooth protocol stack in Linux is provided by BlueZ. The reference driver provides a Bluetooth driver for the JODY-W2 series module. It is a client driver that runs on top of the MMC/SDIO bus driver and performs the following:

1. Forwards data and commands between the upper protocol stack layers and the firmware
2. Handles some private commands used in handshake between the driver and firmware only

The host system can access JODY-W2 modules either through the SDIO or UART interface - depending on the host interface chosen, as described in Configuration pins.

The following drivers can be used for the Bluetooth operation:

1. UART interface:
   - Bluetooth driver `hci_uart` is included in the Linux kernel distribution to which NXP adds additional functionality. We recommend use of the proprietary `hci_uart` module over the open-source variant. The `hci_uart` driver should be compiled as a module rather than a feature in the kernel.
2. SDIO interface:
   - Bluetooth driver `bt8987.ko` is used to provide HCI interface via SDIO to access the Bluetooth hardware. The driver is suitable when using the BlueZ stack.
   - Another Bluetooth driver `mbt8987.ko` is available in the SDIO-SDIO package, which is not bound to BlueZ. This driver exports a character device, which can be used by third-party user space stacks.

The architecture of the Bluetooth driver and protocol stack is shown in Figure 13.

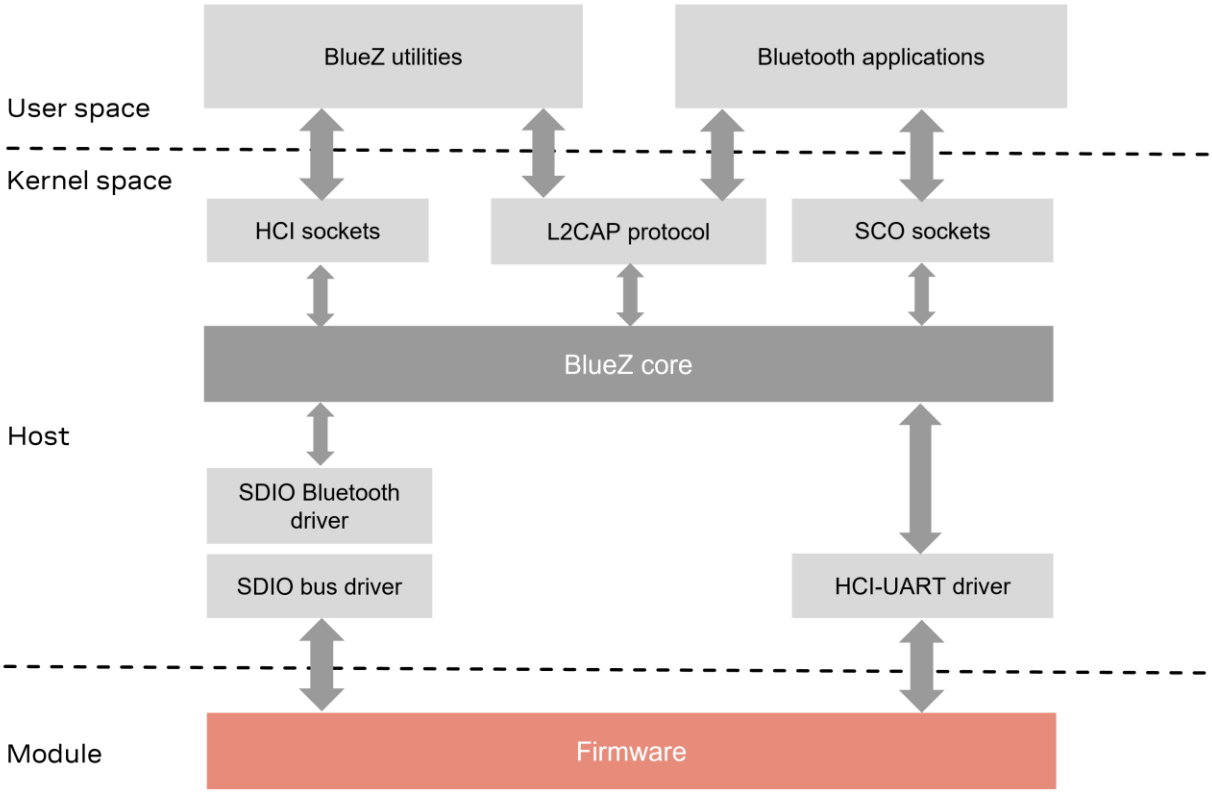


Figure 13: Bluetooth driver and protocol stack

3.5 Compiling the drivers

A README file with details on driver compilation steps, supported features, and commands is provided within all the individual driver packages.

☞ The Yocto/OpenEmbedded recipes provided by u-blox can be used to integrate the software package into Yocto projects. These also make good references to fully understand the process of compiling and deploying the software package. See also Yocto recipes.

3.5.1 Prerequisites

The SDIO driver for JODY-W2 series modules depend on the MMC/SDIO stack supplied with the Linux kernel distribution. Consequently, the correct driver must be enabled in the target kernel configuration of the system.

For configuration management, the driver that supports the cfg80211 wireless configuration API must be selected using the `CONFIG_CFG80211` option.

In order to use Bluetooth implementation in the Linux BlueZ stack, kernel options `CONFIG_BT_HCIUART`, `CONFIG_BT_HCIUART_H4` must be enabled along with other Bluetooth protocols.

Prior to building the driver, the kernel needs to be prepared for the compilation of external kernel modules. To do this, change to the source directory of the kernel and run the following command:

```
$ make modules_prepare
```

⚠ The `make modules_prepare` command does not build `module.symvers` even if `CONFIG_MODVERSIONS` is set. A full kernel build must be executed to make module versioning work.

3.6 Deploying the drivers

The drivers can be deployed at reasonable locations in the target root file system. Using the Yocto recipes provided by u-blox, the utilities and modules typically install as shown below:

```
\
├── etc
│   └── modprobe.d
│       └── jody-w2-driver-sdiouart.conf
├── lib
│   ├── firmware
│   │   └── mrvl
│   │       ├── sd8987_wlan_jody-w2-sdiouart.bin
│   │       ├── sduart8987_combo_jody-w2-sdiouart.bin
│   │       ├── uart8987_ble_jody-w2-sdiouart.bin
│   │       └── uart8987_bt_jody-w2-sdiouart.bin
│   └── modules
│       └── 3.10.40
│           └── updates
│               └── mrvl
│                   └── sd8987
│                       ├── hci_uart_jody-w2-sdiouart.ko
│                       ├── mlan_jody-w2-sdiouart.ko
│                       └── sd8987_jody-w2-sdiouart.ko
└── opt
    └── jody-w2
        └── sdiouart
            ├── mlanutl
            └── uaputl
```

All firmware binaries and kernel modules include a package name suffix, which is shown in the example above as “jody-w2-sdiouart”. The utilities and module files shown in this structure are for the SDIO-UART variant of the driver package. The structure for SDIO-SDIO interface can be similarly extrapolated. Refer to the Yocto recipes to learn more about the install path and names of the files.

3.6.1 Firmware

JODY-W2 series modules can be configured to download the firmware in two different modes:

- Parallel mode: Dedicated interface is used to download the firmware for Wi-Fi and Bluetooth radios separately.
- Serial mode: SDIO interface is used to download the combo firmware, which is applicable to both the radios irrespective of the driver package used either SDIO-UART or SDIO-SDIO.

Table 25 shows the mapping between the different firmware images and their usage for different modes.

Firmware image	Usage for different modes			
	Type of image	Operation mode	Wi-Fi interface	Bluetooth interface
sduart8987_combo.bin	Combo (Wi-Fi + Bluetooth)	Serial	SDIO	UART
sdsd8987_combo.bin	Combo (Wi-Fi + Bluetooth)	Serial	SDIO	SDIO
uart8987_bt.bin	Bluetooth	Parallel	N/A	UART
sd8987_wlan.bin	Wi-Fi	Parallel	SDIO	N/A
sd8987_bt.bin	Bluetooth	Parallel	N/A	SDIO

Table 25: Firmware images and their respective usage

For further information about the commands and logs, see also Using SDIO-UART driver package and Using the SDIO-SDIO driver package.

3.6.2 Configuration utilities

NXP provide the source code for building various applications, which makes it easier to configure the different modes and features of the module.

Application	Functionality
mlanutl	Features and configuration related to station mode in Wi-Fi
uaputl	Features and configuration related to AP mode in Wi-Fi

Table 26: Utilities to configure Wi-Fi modes

3.6.3 Additional software requirements

Although NXP configuration utilities provide the necessary interface to configure features at granular levels, most product vendors prefer open-source applications and stacks. Some additional packages that are recommended for installation on the target system are shown in Table 27.

Package	Comment
bluez	Contains the user space parts of the Linux Bluetooth stack
wpa_supplicant	WPA supplicant. Handles key negotiation, roaming etc. on client side.
iw	CLI configuration utility for wireless devices
hostapd	User space daemon for access point and authentication servers.
crda	User space udev helper to handle regulatory domain

Table 27: Recommended additional software packages

3.7 Configuration of Wi-Fi transmit power limits

JODY-W2 modules contain calibration data for the output power limits in OTP. This calibration data enables the module to achieve maximum transmit power levels that still pass the required EVM and spectral mask limits. The maximum transmit-power levels that can be used in an end-product also depend on:

- Regulatory domain limits
- Restricted band of usage
- Gain of the antenna and antenna trace design

A configuration file on the host system and the utility `mlanutl` is used to reduce the transmit power levels as required.

☞ Transmit power limit configuration files are provided by u-blox for the certified regulatory domains which addresses the reference designs and the approved antennas.

⚠ The correct transmit power limits must be applied to the module after startup of the host system or change of the regulatory domain during runtime.

3.7.1 Wi-Fi power table

The Wi-Fi power table defines the transmit power levels for the Wi-Fi radio. The power levels are based on regulatory compliance, IEEE 802.11 requirements, and product design constraints. The TX power table can be adjusted to achieve the highest transmit power level for each Wi-Fi channel, bandwidth, and modulation within the constraints defined by the certification.

The Wi-Fi power table is defined in a transmit power configuration file, `txpwrlimit_cfg_XX.conf`, where "`XX`" stands for the alpha2 country code. It allows developers to fine tune specific transmit power levels for the Wi-Fi radio, including:

- Band (2G and 5G)
- Channel
- Modulation rate (CCK and OFDM)
- Bandwidth (20, 40, and 80 MHz)

☞ Transmit power configuration files for each completed certification are included in the Yocto meta-layer. Transmit power config files are named as per the name of the certification region, for example `txpwrlimit_cfg_ETSI.conf`. The configuration files are used by the recipe in the meta-layer to derive binary files, which can be automatically loaded by the driver, for each country in the certification region, such as, Germany (DE), France (FR), and so on.

An example of the configuration file for 2 GHz channels is shown below:

```
## 2G Tx power limit CFG
txpwrlimit_2g_cfg_set={
        CmdCode=0x00fb          # do NOT change this line
        Action:2=1              # 1 - SET
        RSVD:2=0                # do NOT change this line

        ChanTRPC.TlvType:2=0x0189
        ChanTRPC.TlvLength:2={
            TLVStartFreq:2=2407
            TLVChanWidth:1=20
            TLVChanNum:1=1
            TLVPwr:20='0,12,1,11,2,11,3,11,4,11,5,11,6,11,7,0,8,0,9,0'
        }
        ChanTRPC.TlvType:2=0x0189
        ChanTRPC.TlvLength:2={
            TLVStartFreq:2=2407
            TLVChanWidth:1=20
            TLVChanNum:1=2
            TLVPwr:20='0,12,1,16,2,16,3,16,4,16,5,16,6,16,7,0,8,0,9,0'
        }
        …
}
```

Description of the parameters is described in Table 28.

Parameter	Description
TLVType	Internal parameter set to 0x189. Do not change this value.
TLVStartFreq	Starting frequency of the band for this channel • 2407, 2414 or 2400 for 2.4 GHz • 5000 for 5 GHz
TLVChanWidth	Channel bandwidth in MHz (for example: 20)
TLVChanNum	Logical 5 MHz channel number (1-255). Channel of the center frequency for HT40 operation in the 2.4 GHz band and primary channel for 40/80 MHz operation in 5 GHz.
TLVPwr:<Length>	Specifies the transmit power limits for specific modulations as a list with the length: <length> of (ModulationGroup,Power) tupels, where ModulationGroup specifies the mapping for the modulation. See also Table 29. Power specifies the Tx power limit in dBm.

Table 28: Parameters in tx power configuration file

To reduce the size of the power table, multiple wireless data rates are grouped into a single rate group as shown in Table 29:

Rate group	Mode	Description
0	11b 20 MHz	CCK (1,2,5.5,11 Mbit/s)
1	11g 20 MHz	OFDM (6,9,12,18 Mbit/s)
2	11g 20 MHz	OFDM (24,36 Mbit/s)
3	11g 20 MHz	OFDM (48,54 Mbit/s)
4	11n/ac 20 MHz	MCS 0,1,2 HT20/VHT20
5	11n/ac 20 MHz	MCS 3,4 HT20/VHT20
6	11n/ac 20 MHz	MCS 5,6,7 HT20/VHT20
7	11n/ac 40 MHz	MCS 0,1,2 HT40/VHT40
8	11n/ac 40 MHz	MCS 3,4 HT40/VHT40
9	11n/ac 40 MHz	MCS 5,6,7 HT40/VHT40
10	11ac 20 MHz	MCS 8 VHT20
11	11ac 40 MHz	MCS 8,9 VHT40
12	11ac 80 MHz	MCS 0, 1, 2 VHT80
13	11ac 80 MHz	MCS 3, 4 VHT80
14	11ac 80 MHz	MCS 5,6,7 VHT80
15	11ac 80 MHz	MCS 8,9 VHT80

Table 29: Rate group information for one spatial stream

The configuration file example above sets the following transmit power limits for channel 1 and 2 in the 2.4 GHz band:

- 12 dBm for 802.11b rates (BPSK, QPSK, CCK)
- 11 dBm for 802.11g OFDM (6, 9, 12, 18 Mbps; 24, 36 and 48, 54 Mbps),
- 11 dBm for 802.11n HT20 (MCS 0 to MCS 7)

☞ For HT40 operation in the 2.4 GHz band (HT40 MCS0-7), the transmit power limits are selected from the channel of the center frequency. For example, the first 40 MHz channel at the center frequency 2422 MHz (20 MHz channels 1+5) uses the transmit power limits from HT40 values in the entry with `TLVChanNum=3`.

A sample of the configuration file for 5 GHz channels is shown below.

```
## 5G Tx power limit CFG
txpwrlimit_5g_cfg_set={
        CmdCode=0x00fb          # do NOT change this line
        Action:2=1              # 1 - SET
        RSVD:2=0                # do NOT change this line

        ChanTRPC.TlvType:2=0x0189
        ChanTRPC.TlvLength:2={
            TLVStartFreq:2=5000
            TLVChanWidth:1=20
            TLVChanNum:1=36
            TLVPwr:30='1,15,2,15,3,15,4,15,5,15,6,15,7,15,8,15,9,15,10,15,11,15,12,14,
13,14,14,14,15,14'
        }
        ChanTRPC.TlvType:2=0x0189
        ChanTRPC.TlvLength:2={
            TLVStartFreq:2=5000
            TLVChanWidth:1=20
            TLVChanNum:1=40
            TLVPwr:30='1,15,2,15,3,15,4,15,5,15,6,15,7,15,8,15,9,15,10,15,11,15,12,14,
13,14,14,14,15,14'
        }
…
}
```

☞ Contrary to the configuration of 2.4 GHz band, the transmit-power-limit configurations for the 5 GHz band are not defined through a channel center frequency but must instead be specified for all related 20 MHz channels. For example, the 40 MHz channel at the center frequency 5190 MHz (20 MHz channels 36+40) uses the transmit power limits from HT40 values in the entry with `TLVChanNum=36`. These limits should be equal to the HT40 values in the entry with `TLVChanNum=40`.

For the exact power limits used in the u-blox reference design for the various certifications, see the Appendix: Wi-Fi Tx output power limits.

3.7.2 Applying the transmit power limit configuration

The configuration file `txpwrlimit_cfg.conf` contains separate sections for setting the transmit power limits for 2.4 and 5 GHz. These can be applied using the `mlanutl` tool, as shown in the following example:

```
mlanutl mlan0 hostcmd txpwrlimit_cfg.conf txpwrlimit_2g_cfg_set
mlanutl mlan0 hostcmd txpwrlimit_cfg.conf txpwrlimit_5g_cfg_set
```

The WLAN driver also looks for a binary file (text file with hex values) on the filesystem, with the transmit power limit configuration, whenever the regulatory domain is changed. The file name of this file should be `txpower_XX.bin`, where "`XX`" is the ISO/IEC 3166 alpha2 country code. The file is expected to reside in the same folder as the firmware. The binary configuration files can be generated from the `txpwrlimit_cfg.conf` files using the `mlanutl` tool:

```
mlanutl mlan0 hostcmd txpwrlimit_cfg.conf generate_raw <txpower_XX.bin>
```

☞ Configurations with syntactic or semantic errors are not necessarily reported by the tool when applied.

3.7.3 Reading the transmit power limit configuration

The current transmit power limit tables can be read from the firmware using the `mlanutl` tool as shown in the following example:

```
mlanutl mlan0 get_txpwrlimit <n> [raw_data_file]
       where <n>
              0:      Get 2.4G txpwrlimit table
              0x10:   Get 5G sub0 txpwrlimit table
              0x11:   Get 5G sub1 txpwrlimit table
              0x12    Get 5G sub2 txpwrlimit table
              0x1f    Get all 5G txpwrlimit table
              0xff    Get both 2G and 5G txpwrlimit table
       <raw_data_file> driver will save fw raw data to this file.
```

3.8 Configuration of Bluetooth power levels

A vendor specific HCI command `HCI_CMD_MARVELL_UPDATE_TX_MAX_PWR_LVL` must be used to set the exact power limit for Bluetooth as shown below:

```
# hcitool -i hci0 3F EE 01 <signed tx power value in dBm >
hcitool -i hci0 cmd 3F EE 01 0A
# After above command HCI reset command is required take effect.
hcitool -i hci0 cmd 03 03
```

☞ A maximum Tx power of up to 10 dBm can be set using the `hcitool` command. The power is capped at 4 dBm for Bluetooth LE advertisement.

3.9 Adaptivity configuration (energy detection)

JODY-W2 modules support the adaptivity requirements (energy detection) from EN 300 328 and EN 301 893 for Wi-Fi. The adaptivity or Energy Detect mechanism must be explicitly enabled after the startup of the module, and correct detection threshold values must be configured. These threshold values depend on the combined gain of the antenna and antenna trace used in the end-product.

☞ u-blox provide a configuration file to enable energy detection and set the detection thresholds for the reference designs.

The following command enables energy detection and configures the detection thresholds according to the settings in the `ed_mac_ctrl_V3_8987.conf` configuration file:

```
mlanutl mlan0 hostcmd config/ed_mac_ctrl_V3_8987.conf ed_mac_ctrl_v3
```

The values `ed_ctrl_2g.offset` and `ed_ctrl_5g.offset` used in the excerpt below have been determined in the Reference schematic. Changes to the antenna path of that reference design, e.g., introducing a higher attenuation on the antenna path, have to be reflected into the energy detection configuration file. Therefore, the offsets `ed_ctrl_2g.offset` and `ed_ctrl_5g.offset` can be increased to compensate the additional attenuation of the antenna path. Where increasing the value of the offset would result in a more sensitive behavior. Increasing the offset value by 1 would lower the sensitivity threshold for energy detection by 1 dB. An integrator is encouraged to optimize the sensitivity threshold for energy detection.

```
#       File : ed_mac_ctrl_V3_8987.conf
#
#   ed_mac_ctrl_v3 is used for 88W8987
#   ./mlanutl mlan0 hostcmd config/ed_mac_ctrl_V3_8987.conf ed_mac_ctrl_v3
#
## Set Energy Detect Threshold for EU Adaptivity test
ed_mac_ctrl_v3={
    CmdCode=0x0130                  #Command code, DO NOT change this line
    ed_ctrl_2g.enable:2=0x1         # 0       - disable EU adaptivity for 2.4GHz band
                                    # 1       - enable EU adaptivity for 2.4GHz band
    ed_ctrl_2g.offset:2=0x6         # 0       - Default Energy Detect threshold
                                    #offset value range: 0x80 to 0x7F
    ed_ctrl_5g.enable:2=0x1         # 0       - disable EU adaptivity for 5GHz band
                                    # 1       - enable EU adaptivity for 5GHz band
    ed_ctrl_5g.offset:2=0x6         # 0       - Default Energy Detect threshold
                                    #offset value range: 0x80 to 0x7F
    ed_ctrl_txq_lock:4=0xFF         #DO NOT Change this line
}
```

3.10 Yocto recipes

Yocto meta layer is provided by u-blox for all the modules. This layer can be used to build the image for most of the host platforms that run Linux kernels. It contains various files for building the software components, loading, and configuring the module.

File type	Description
Build recipe	Include all the instructions to extract, compile and install the drivers and firmware in the root file system of the image built for the host system.
Patch	Used for drivers distributed through u-blox for some bugs locally seen or recommended by the vendor.
Calibration	Provided by u-blox, to be used while loading the driver. These files store the tuning parameters needed for RF parts present in the module, such as, the crystal etc.
Power configuration	RF power specific files for the different bands, rates and countries are stored in tx_power.conf provided by u-blox. These are built as a binary files and can be downloaded when the location changes.
Modprobe	Required for the SDIO-UART, SDIO-SDIO and mfg mode drivers.
Manufacturing package recipes	Include the different recipes to build the manufacturing driver and firmware. These can be used in production and RF-related tests.
Labtool recipes	Used by this proprietary tool to run specific tests and configure the hardware and RF parameters. This test and configuration tool uses different firmware and driver modes.

Further information about Yocto layers is provided in the README file present in the recipe.

3.11 Runtime usage

With focus on operating the module for different use-cases, such as station, access-point, this section describes how to load specific drivers in different modes and configurations.

In SDIO-UART and SDIO-SDIO configuration, the firmware can be downloaded in either serial or parallel mode. Even though the download part changes significantly, the Wi-Fi and Bluetooth operation in different use cases remain the same.

3.11.1 Using reserved MAC addresses

JODY-W2 series modules have four unique MAC addresses that are reserved specifically for each module variant. Two of these addresses are separately dedicated for use with Bluetooth radio and Wi-Fi and are stored in the OTP during production. The other two are reserved for other local interfaces.

The Wi-Fi driver assigns unique MAC addresses to the local interfaces, sequentially. The address given to each interface is derived from the primary MAC address.

Example

`D4:CA:6E:00:1B:16` – Bluetooth interface

`D4:CA:6E:00:1B:17` – Wi-Fi station interface (mlan0)

`D4:CA:6E:00:1B:18` – Reserved for secondary module interfaces

`D4:CA:6E:00:1B:19` – Reserved for secondary module interfaces

☞ The use of reserved MAC addresses is recommended to avoid possible collisions with the MAC addresses of other modules.

You can change the MAC address of the module by configuring the `init_cfg.conf` file when loading the driver. Note that the driver expects the `init_cfg.conf` file to be present in the directory relative to `/lib/firmware/`.

In the following example, the MAC addresses of the Wi-Fi interfaces have been changed in the `init_cfg.conf` file. The changes have been implemented to meet the application requirements so that each interface is assigned with a unique MAC address to avoid conflicts. The addresses are assigned to the primary (`uap0`) and secondary (`uap1`) interfaces.

```
File: /lib/firmware/mrvl/init_cfg.conf
# MAC address (interface: address)
mac_addr=uap0: D4:CA:6E:00:1B:18
mac_addr=uap1: D4:CA:6E:00:1B:19
insmod mlan.ko && insmod sd8987.ko fw_name=mrvl/sdsd8987_combo_jody-w2-sdio.bin
cfg80211_wext=0xf cal_data_cfg=none init_cfg=mrvl/init_cfg.conf max_uap_bss=2
# ifconfig -a | grep HWaddr
mlan0     Link encap:Ethernet  HWaddr D4:CA:6E:00:1B:17
uap0      Link encap:Ethernet  HWaddr D4:CA:6E:00:1B:18
uap1      Link encap:Ethernet  HWaddr D4:CA:6E:00:1B:19
```

☞ To configure a second AP interface (`uap1`), you need to set the parameter `max_uap_bss=2` when loading the driver.

3.11.2 Device detection

When JODY-W2 series modules are are connected to the host system through SDIO, confirmation that the SDIO card has been detected is reported in the kernel log:

```
mmc1: new ultra high speed SDR104 SDIO card at address 0001
```

3.11.3 Using SDIO-UART driver package

JODY-W2 modules provide two options for downloading the firmware, as described in Firmware. The commands included in the following examples show how the different driver and firmware combinations are used. The downloading method is based on firmware version and the given argument for loading the driver.

3.11.3.1 Serial mode

In the default serial mode, combo firmware is used. This firmware operates on the Wi-Fi and Bluetooth parts of the chip.

```
# insmod mlan.ko
# insmod sd8987.ko fw_name=mrvl/sduart8987_combo_jody-w2-sdiouart.bin cfg80211_wext=0xf
cal_data_cfg=none
root@:/# lsmod
Module                  Size    Used by
sd8xxx                  449099  3
mlan                    369709  1 sd8xxx
cfg80211                355367  1 sd8xxx
```

By default, kernel module `sd8987` downloads the firmware `mrvl/sduart8987_combo.bin`. The driver expects the firmware to be relative to the path[12] `/lib/firmware`. The log of a successful firmware download is shown below.

```
[   72.034179] mmc1: new ultra high speed SDR104 SDIO card at address 0001
[  333.390065] mlan: loading out-of-tree module taints kernel.
[  333.431751] wlan: Loading MWLAN driver
[  333.436334] vendor=0x02DF device=0x9149 class=0 function=1
[  333.443326] SDIO: max_segs=128 max_seg_size=65535
[  333.448263] rx_work=1 cpu_num=4
[  333.453058] wlan: Enable TX SG mode
[  333.456558] wlan: Enable RX SG mode
[  333.468777] Request firmware: mrvl/sduart8987_combo_jody-w2-sdiouart.bin
[  333.988129] Wlan: FW download over, firmwarelen=629824 downloaded 629824
[  334.897778] WLAN FW is active
[  334.922457] fw_cap_info=0x187cff03, dev_cap_mask=0xffffffff
[  334.928073] max_p2p_conn = 8, max_sta_conn = 8
[  334.940920] creating custom regulatory domain failed
[  334.981289] wlan: version = SD8987-16.68.10.p33-C4X15C651-GPL-(FP68)
[  334.990293] wlan: Driver loaded successfully
```

⚠ To avoid collisions between the SDIO-SDIO and SDIO-UART drivers, we advise against loading more than one NXP reference driver of the same kind simultaneously.

The kernel modules can be unloaded using the below command:

```
# rmmod sd8xxx mlan
[415240.024054] wlan: Unloading MWLAN driver
[415240.032803] wlan: Driver unloaded
```

☞ While using the dual Wi-Fi interfaces on JODY-W2 module, such as access point and station at the same time, different MAC addresses for each logical network interface should be used. See also Using reserved MAC addresses.

[12] In the latest driver packages released by NXP, the default path is changed to /lib/firmware/nxp/. Use the path variable based on the driver package. Refer to the README file in the driver for instructions.

After loading the Wi-Fi driver with combo firmware, we do not need to specify the Bluetooth firmware while loading the driver. The UART host interface of the JODY-W2 series module must be configured for Bluetooth. See also Configuration pins.

```
# insmod ./hci_uart.ko
[  435.469227] HCI UART driver ver 2.2-M2614100
[  435.477280] HCI H4 protocol initialized
[  435.502009] HCI BCSP protocol initialized
[  435.511552] HCILL protocol initialized
```

☞ The `hci_uart.ko` kernel module is distributed with the kernel sources, which means that BT_HCIUART feature might already be included in the kernel. If this is the case, it is not possible to load the module provided by NXP. The kernel configuration should include `CONFIG_BT_HCIUART=m` and must not include `CONFIG_BT_HCIUART=y` so that it allows us to load the proprietary module provided by NXP.

3.11.3.2 Parallel mode

In parallel mode, two different firmware binary files are used together with the respective driver. Set the driver parameter `fw_serial=0` to configure the download operation in parallel mode, as shown below.

```
# insmod mlan.ko
# insmod sd8987.ko fw_name=mrvl/sd8987_wlan_jody-w2-sdiouart.bin cfg80211_wext=0xf
cal_data_cfg=none fw_serial=0
```

To download the Bluetooth firmware over UART, we need `fw_loader` built from `uartfwloader_src` present in the `SDIO-UART` driver package. Sample to download along with all the parameters is shown below.

```
# fw_loader /dev/ttyUSB0 115200 0 /lib/firmware/mrvl/uart8987_bt_jody-w2-sdiouart.bin
3000000
Protocol: Marvell Proprietary
FW Loader Version: M304
ComPort : /dev/ttyUSB0
BaudRate: 115200
FlowControl: 0
Filename: /lib/firmware/mrvl/uart8987_bt_jody-w2-sdiouart.bin
Second BaudRate: 3000000
File downloaded:   204864:  204864
Download Complete
time:8060
CTS is low
# insmod hci_uart.ko
```

☞ Note the sequence. The firmware is downloaded first and is then followed by driver.

☞ The example uses `/dev/ttyUSB0` as the serial device port. Replace it with the port where the JODY-W2 series UART interface is connected to the host system.

3.11.4 Using SDIO-SDIO driver package

While using SDIO-SDIO package the same bus is shared between both radios. It also has both modes of usage.

3.11.4.1 Serial mode

In serial mode, a combo firmware is used. By default, the kernel module `sd8987` downloads the firmware `mrvl/sdsd8987_combo.bin`. Here are the set of commands used.

```
# insmod mlan.ko
# insmod sd8987.ko fw_name=mrvl/sdsd8987_combo_jody-w2-sdio.bin cfg80211_wext=0xf
cal_data_cfg=none
```

For Bluetooth, we can just load the module.

```
# insmod bt8987.ko
```

When combo FW is loaded either by Wi-Fi or Bluetooth, the driver loaded second detects the FW and does not try to download it again. There is no specific order in which drivers are loaded, so technically the Bluetooth driver can be loaded first with the combo FW, followed by Wi-Fi driver.

3.11.4.2 Parallel mode

Here we use two different firmware binaries along with the respective driver. Here we need to set `fw_serial=0`, to configure the download operation in parallel mode. The excerpt below shows the command for it.

```
# insmod mlan.ko
# insmod sd8987.ko fw_name=mrvl/sd8987_wlan_jody-w2-sdio.bin cfg80211_wext=0xf
cal_data_cfg=none fw_serial=0
```

To operate Bluetooth in parallel mode using dedicated firmware, we need to set `bt_fw_serial=0` which will enable this mode. Remember to use the Bluetooth only firmware.

```
# insmod bt8987.ko bt_fw_serial=0 fw_name=mrvl/sd8987_bt_jody-w2-sdio.bin
[   33.066092] bt8xxx: loading out-of-tree module taints kernel.
[   33.073293] BT: Loading driver
[   33.178538] BT Request firmware: mrvl/sd8987_bt_jody-w2-sdio.bin
[   33.507969] BT: FW download over, size 210952 bytes
[   33.713345] BT FW is active(2)
[   33.730704] BT: Driver loaded successfully
```

3.11.5 Verifying the firmware version

The version of the loaded driver can be verified using the following command:

```
# mlanutl mlan0 version
Version string received: SD8987-16.68.10.p33-C4X15C651-GPL-(FP68)
```

3.11.6 Verifying the interfaces

The available Wi-Fi interfaces can be seen using `ifconfig` command.

Interface	Usage
mlan0	Default interface used for station mode functionality. Can be configured using mlanutl.
uap0	Virtual interface with AP functionality, it can be configured using uaputl.
wfd0	Virtual interface to use P2P functionality. It can operate in both group owner as well as client mode.

```
ifconfig -a
mlan0     Link encap:Ethernet  HWaddr D4:CA:6E:00:1B:17
          UP BROADCAST MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)
uap0      Link encap:Ethernet  HWaddr D4:CA:6E:00:1C:17
          UP BROADCAST MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)
wfd0      Link encap:Ethernet  HWaddr D6:CA:6E:00:1B:17
          UP BROADCAST MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)
```

☞ Driver internally sets the Locally Administered Address bit of the first octet of the MAC address assigned to P2P interface as seen in the below excerpt.

3.11.7 Access point

This information provided in this section assumes that the JODY-W2 series module has been connected to the host and the Wi-Fi drivers are loaded. Not all the driver packages have firmware which supports internal supplicant and authenticator. The package must include the tools `mlanutl` and `uaputl` for station and AP respectively. See the README file in the driver package to check this.

3.11.7.1 Using internal authenticator

In the following scenario, an access point is created using the example configuration tool provided by NXP called `uaputl`. NXP firmware has internal authenticator functionalities that are used in this case.

☞ The embedded authenticator is not supported in all firmware releases. Using hostapd is the recommended way to configure the access point.

The access point is configured with an SSID value "`jody-w2`" for 80 MHz bandwidth and passphrase "`12345678`" for WPA2 based encryption. The description of the individual commands is provided in the `README_uap` and `README_mlan` files.

To set up the SSID and the encryption mechanisms:

```
./uaputl.exe -i uap0 sys_cfg_80211d state 1 country DE
./uaputl.exe -i uap0 sys_cfg_rates 0x8c 0x98 0xb0 0x12 0x24 0x48 0x60 0x6c
./uaputl.exe -i uap0 sys_cfg_channel 36 2
./uaputl.exe -i uap0 httxcfg 0x16f
./uaputl.exe -i uap0 sys_cfg_11n 1 0x16f 3 0x09E1E008 0xff
./uaputl.exe -i uap0 vhtcfg 2 3 1 0x33c07130 0xfffe 0xfffe
./uaputl.exe -i uap0 sys_cfg_protocol 32
./uaputl.exe -i uap0 sys_cfg_cipher 8 8
./uaputl.exe -i uap0 sys_cfg_wpa_passphrase 12345678
./uaputl.exe -i uap0 sys_cfg_ssid jody-w2
./uaputl.exe -i uap0 bss_start
```

To assign an IP to the interface:

```
ifconfig uap0 192.168.1.1
```

Additionally, we can run a DHCP server on the interface to automatically assign IP addresses to the connected clients.

```
File: udhcpd.conf
interface uap0
start 192.168.1.10
end 192.168.1.200
option subnet 255.255.255.0
```

Command to start the DHCP server:

```
udhcpd udhcpd.conf
```

☞ By providing the -f option in the command, the server will run in the foreground with logs.

3.11.7.2 Using hostapd

`Hostapd` is an open-source configuration manager used to bring up the access point. Sources can be found in the location: `https://w1.fi/hostapd/`.

Here is a sample command used to create access point:

```
./hostapd ./hostapd.conf -B
```

☞ If the command is used with `-dddt` option, `hostapd` generates detailed logs.

Here `hostapd.conf` is used as a configuration file that has all the information related to the channel, security etc. A sample of file which can be used is given below.

The access point is configured with an SSID value "`jody-w2`" with the passphrase `12345678` for WPA2 based encryption. It operates in channel 36 with 80 MHz bandwidth.

```
File: hostapd.conf

interface=uap0
driver=nl80211
ssid=jody-w2

# RF
hw_mode=a
channel=36
country_code=DE

# 11N
ieee80211n=1
ht_capab=[HT40+][SHORT-GI-20][SHORT-GI-40]

# 11AC
ieee80211ac=1
vht_capab=[SHORT-GI-80]
vht_oper_chwidth=1
vht_oper_centr_freq_seg0_idx=42

# Security
wpa=2
wpa_passphrase=12345678
wpa_key_mgmt=WPA-PSK
wpa_pairwise=TKIP
rsn_pairwise=CCMP
```

3.11.8 Station mode

3.11.8.1 Using internal supplicant

You can connect to an AP using NXP configuration tools.

```
# ./mlanutl mlan0 passphrase "1;ssid=<ssid>;passphrase=<sharedkey>"
# ./mlanutl mlan0 assocessid <ssid>
# ./mlanutl mlan0 reassoctrl 1
# udhcpc -i mlan0
For example,
# ./mlanutl mlan0 passphrase "1;ssid=ubx-co-AP5G;passphrase=12345678"
# ./mlanutl mlan0 assocessid ubx-co-AP5G
# ./mlanutl mlan0 reassoctrl 1
# udhcpc -i mlan0
```

☞ The embedded supplicant is not supported in all firmware releases. Using wpa_supplicant is the recommended way to configure the station mode.

3.11.8.2 Using wpa_supplicant

`Wpa_supplicant` is an open-source configuration manager used to connect to an access point which uses different security encryption methods. Sources can be found in the location: https://w1.fi/wpa_supplicant/.

The following commands are used to connect to an access point. Initially prepare the configuration file with some primitive settings:

```
# cat > /etc/wpa_supplicant.conf << EOF
ctrl_interface=/var/run/wpa_supplicant
ctrl_interface_group=0
update_config=1
EOF
```

To set wireless network settings such as SSID (ubx-co-AP5G) and the passphrase (12345678):

```
# wpa_passphrase <ssid> <passphrase> >> /etc/wpa_supplicant.conf
For example,
# wpa_passphrase ubx-co-AP5G 12345678 >> /etc/wpa_supplicant.conf
```

To run `wpa_supplicant` daemon:

```
# wpa_supplicant -B -D nl80211 -i mlan0 -c /etc/wpa_supplicant.conf
```

☞ If the command is used with `-dddt` option, `wpa_supplicant` generates detailed logs.

To acquire an IP address:

```
# udhcpc -i mlan0
```

3.11.9 Bluetooth usage

Once the Bluetooth drivers are loaded, it is necessary to bind a serial interface to the HCI driver. For this, the `hciattach` tool from the BlueZ package can be used. The following excerpt shows an example of an attach through the /dev/ttyUSB0 serial device. In the following example, Bluetooth is connected to the host using USB cable connected via FTDI.

```
# hciattach /dev/ttyUSB0 any 3000000 flow
[  442.667056] ps_init_work...
[  442.675963] ps_init_timer...
[  442.684716] ps_init...
[  442.816845] Bluetooth: BNEP (Ethernet Emulation) ver 1.3
[  442.825928] Bluetooth: BNEP socket layer initialized
[  443.234456] Bluetooth: RFCOMM TTY layer initialized
[  443.245865] Bluetooth: RFCOMM socket layer initialized
[  443.254362] Bluetooth: RFCOMM ver 1.11
Device setup complete
```

☞ It is not necessary to attach while using SDIO interface for Bluetooth.

Then, an HCI interface (here hci0) is available for further transactions.

```
# hciconfig -a hci0 up
hci0:   Type: Primary  Bus: UART
        BD Address: D4:CA:6E:00:1B:16 ACL MTU: 1021:7  SCO MTU: 120:6
        UP RUNNING PSCAN
        RX bytes:918 acl:0 sco:0 events:62 errors:0
        TX bytes:1115 acl:0 sco:0 commands:62 errors:0
        Features: 0xff 0xfe 0x8f 0xfe 0xdb 0xff 0x7b 0x87
        Packet type: DM1 DM3 DM5 DH1 DH3 DH5 HV1 HV2 HV3
        Link policy: RSWITCH HOLD SNIFF
        Link mode: SLAVE ACCEPT
        Name: 'apalis-tk1'
        Class: 0x200000
        Service Classes: Audio
        Device Class: Miscellaneous,
        HCI Version: 5.0 (0x9)  Revision: 0x8300
        LMP Version: 5.0 (0x9)  Subversion: 0x10bc
```

Here is an excerpt which shows the command to scan, results are displayed along with it.

```
# hcitool -ihci0 scan
Scanning ...
        8C:83:E1:77:22:55       Galaxy S9
        B4:69:21:62:32:6F       DE-BLN-LT-020
        30:F7:72:11:D6:6C       KD-55X8505C
        64:A2:F9:36:97:B5       ubx-ae
```

L2CAP echo requests can be used to ping the remote devices.

```
# l2ping 64:A2:F9:36:97:B5
Ping: 64:A2:F9:36:97:B5 from D4:CA:6E:00:1B:16 (data size 44) ...
44 bytes from 64:A2:F9:36:97:B5 id 0 time 8.16ms
44 bytes from 64:A2:F9:36:97:B5 id 1 time 53.00ms
44 bytes from 64:A2:F9:36:97:B5 id 2 time 35.99ms
44 bytes from 64:A2:F9:36:97:B5 id 3 time 83.90ms
4 sent, 4 received, 0% loss
```

3.11.10 Sleep mode configuration

Quite often modules are used in sleep mode to conserve power and improve the efficiency based on the application. Use the following procedure to enable deep sleep on JODY-W2 modules.

1. Download the driver by enabling power save methods.
    a. SDIO driver for Wi-Fi and Bluetooth.

```
# insmod mlan.ko
# insmod sd8987.ko fw_name=mrvl/sdsd8987_combo_jody-w2-sdio.bin
cfg80211_wext=0xf cal_data_cfg=none drv_mode=1 ps_mode=1 auto_ds=1
# insmod ./bt8987.ko psmode=1 deep_sleep=1
```

    b. For Bluetooth connected over UART

```
# insmod ./hci_uart.ko ps_mode=1
# Bind the device node to the HCI interface
# hciattach /dev/ttyUSB0 any 3000000 flow
```

2. Set Bluetooth and Bluetooth LE sleep modes using HCI commands

```
# hciconfig -a hci0 up
# hcitool -i hci0 cmd 3F 23 02      # enable BT power save
# hcitool -i hci0 cmd 3F 8B 01      # enable BLE power save
```

☞ For deep-sleep power consumption measurements, disable network managing utilities like `hostapd`, `wpa_supplicant`, and `network-manager`.

3.12 Driver debugging

Driver debugging is provided through the kernel print function `printk` and the `proc` file system. The driver states are recorded and can be retrieved through the proc file system during runtime. The following files containing the debug information are provided (the actual location is dependent on the Linux kernel version):

- `/proc/mwlan/config or /proc/net/mwlan/config`
- `/proc/mwlan/mlanX/info or /proc/net/mwlan/mlanX/info`
- `/proc/mwlan/mlanX/debug or /proc/net/mwlan/mlanX/debug`

☞ mlanX is the name of the device node created at runtime. Other possibilities are uapX and wfdX for the access point and Wi-Fi Direct interfaces respectively.

The debug messages are also printed to the kernel ring buffer through printk calls. These messages can be accessed using the `/proc/kmsg` interface or by the `dmesg` command. Alternatively, this can also be handled by more advanced logging facilities.

3.12.1 Compile-time debug options

The extent to which the debug messages are available to be printed at runtime is controlled by the `CONFIG_DEBUG` variable in the driver `makefile`. The `CONFIG_DEBUG` variable can have the following values:

- n: Debug messages are disabled and not compiled into the driver module
- 1: All kinds of debug messages can be configured except for `MENTRY`, `MWARN` and `MINFO`. By default, `MMSG`, `MFATAL` and `MERROR` are enabled.
- 2: All kinds of debug messages can be configured

3.12.2 Runtime debug options

Once debugging is enabled in the `makefile`, debug messages can be selectively enabled or disabled at runtime by setting or clearing the corresponding bits of the `drvdbg` parameter:

```
bit 0:  MMSG          PRINTM(MMSG,...)
bit 1:  MFATAL        PRINTM(MFATAL,...)
bit 2:  MERROR        PRINTM(MERROR,...)
bit 3:  MDATA         PRINTM(MDATA,...)
bit 4:  MCMND         PRINTM(MCMND,...)
bit 5:  MEVENT        PRINTM(MEVENT,...)
bit 6:  MINTR         PRINTM(MINTR,...)
bit 7:  MIOCTL        PRINTM(MIOCTL,...)
...
bit 16: MDAT_D        PRINTM(MDAT_D,...), DBG_HEXDUMP(MDAT_D,...)
bit 17: MCMD_D        PRINTM(MCMD_D,...), DBG_HEXDUMP(MCMD_D,...)
bit 18: MEVT_D        PRINTM(MEVT_D,...), DBG_HEXDUMP(MEVT_D,...)
bit 19: MFW_D         PRINTM(MFW_D,...),  DBG_HEXDUMP(MFW_D,...)
bit 20: MIF_D         PRINTM(MIF_D,...),  DBG_HEXDUMP(MIF_D,...)
...
bit 28: MENTRY        PRINTM(MENTRY,...), ENTER(), LEAVE()
bit 29: MWARN         PRINTM(MWARN,...)
bit 30: MINFO         PRINTM(MINFO,...)
```

The value of drvdbg can be given as a module parameter when the driver is loaded, by writing to the proc file system's `debug` file or by setting it through the `iwpriv` or `mlanutl` tool.

```
iwpriv mlan0 drvdbg                          # Get the current driver debug mask
iwpriv mlan0 drvdbg 0                        # Disable all debug messages
echo "drvdbg=0x7" > /proc/mwlan/mlan0/debug  # enable MMSG, MFATAL and MERROR
mlanutl mlan0 drvdbg -1                      # Enable all debug messages
```

4 Handling and soldering

⚠ JODY-W2 series modules are Electrostatic Sensitive Devices that demand the observance of special handling precautions against electrostatic damage. Failure to observe these precautions can result in severe damage to the product.

4.1 ESD handling precautions

⚠ As the risk of electrostatic discharge in the RF transceivers and patch antennas of the module is of particular concern, standard ESD safety practices are prerequisite. See also Figure 14.

Consider also:

- When connecting test equipment or any other electronics to the module (as a standalone or PCB-mounted device), the first point of contact must always be to local GND.
- Before mounting an antenna patch, connect the device to ground.
- When handling the RF pin, do not touch any charged capacitors. Be especially careful when handling materials like patch antennas (~10 pF), coaxial cables (~50-80 pF/m), soldering irons, or any other materials that can develop charges.
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk of the exposed antenna being touched in an unprotected ESD work area, be sure to implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the RF pin on the receiver, be sure to use an ESD-safe soldering iron (tip).

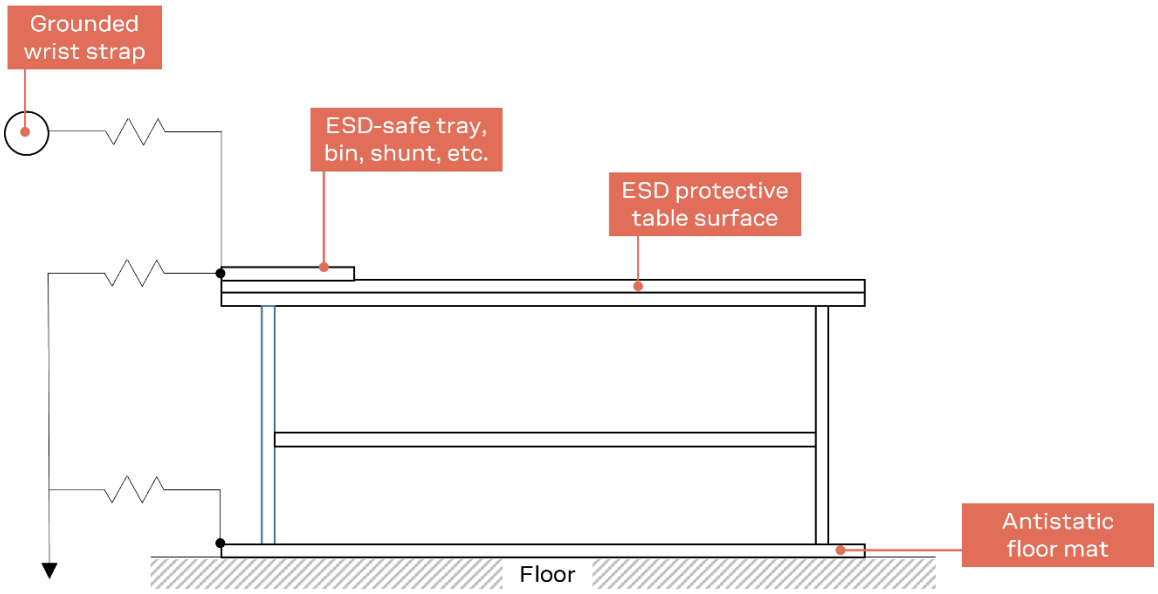


Figure 14: Standard workstation setup for safe handling of ESD-sensitive devices

4.2 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to reels, tapes or trays, moisture sensitivity levels (MSL), shipment and storage, as well as drying for preconditioning, refer to the respective JODY-W2 series data sheet [2] and Packaging information reference guide [3].

4.3 Soldering

☞ No natural rubbers, hygroscopic materials or materials containing asbestos are employed.

4.3.1 Reflow soldering process

JODY-W2 series modules are surface mounted devices supplied in a Land Grid Array (LGA) package with gold-plated solder lands. The modules are manufactured in a lead-free process with lead-free soldering paste.

The thickness of solder resist between the top side of the host PCB and the bottom side of the JODY-W2 series module must be considered for the soldering process.

JODY-W2 modules are compatible with the industrial reflow profile for common SAC type RoHS solders. No-clean soldering paste is strongly recommended. The reflow profile is dependent on the thermal mass over the entire area of the fully populated host PCB, the heat transfer efficiency of the oven, and the type of solder paste that is used. The optimal soldering profile that is used must be trimmed for each case depending on the specific soldering process and PCB layout.

The target parameter values shown in Table 30 are only general guidelines for a Pb-free process. The given values are tentative and subject to change. For further information, see also the JEDEC J-STD-020E standard [7].

Process parameter		Unit	Target
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_S (from 25°C)	s	150
	t_S (Pre-heat)	s	110
Peak	T_L	°C	217
	t_L (time above T_L)	s	90
	T_P (absolute max)	°C	260
	t_P (time above T_P -5°C)	s	30
Cooling	Ramp-down from T_L	K/s	6
General	$T_{to\ peak}$	s	300
	Allowed soldering cycles	-	1

Table 30: Recommended reflow profile

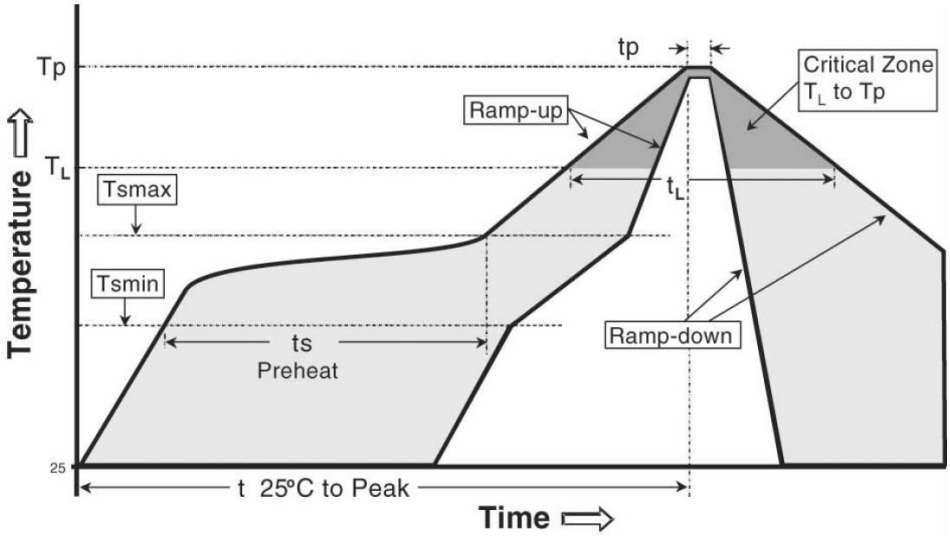


Figure 15: Reflow profile

☞ A lower value of T_P and slower ramp down rate (2 – 3 °C/sec) is preferred.

4.3.2 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pins. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housing, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module and the crystal oscillators in particular.
- For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering process.

4.3.3 Other notes

- Only a single reflow soldering process is allowed for boards with a module populated on them.
- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices may require wave soldering to solder the THT components. Only a single wave soldering process is allowed for boards populated with the modules.
- Miniature Wave Selective Solder process is preferred over traditional wave soldering process.
- Hand soldering is not recommended.
- Rework is not recommended.
- Conformal coating may affect the performance of the module, it is important to prevent the liquid from flowing into the module. The RF shields do not provide protection for the module from coating liquids with low viscosity, so care is needed when the coating is applied. Conformal coating of the module will void the warranty.
- Grounding metal covers: Attempts to improve grounding by soldering ground cables, wick, or other forms of metal strips directly onto the EMI covers is done at the customer's own risk and will void the module warranty. The numerous ground pins are adequate to provide optimal immunity to interferences.
- The modules contain components that are sensitive to Ultrasonic Waves. Use of any ultrasonic processes, like cleaning and welding, might damage the module. Use of ultrasonic processes on an end product integrating this module will void the warranty.

5 Regulatory compliance

5.1 General requirements

JODY-W2 modules comply with the regulatory demands of Federal Communications Commission (FCC), Innovation, Science and Economic Development Canada (ISED)[13] and the CE mark[14]. This section contains instructions on the process needed for an integrator when including the JODY-W2 into an end-product.

- Any deviation from the process described may cause the JODY-W2 module not to comply with the regulatory authorizations of the module and thus void the user's authority to operate the equipment.
- Any changes to hardware, hosts or co-location configuration may require new radiated emission and SAR evaluation and/or testing.
- The regulatory compliance of JODY-W2 does not exempt the end-product from being evaluated against applicable regulatory demands; for example, FCC Part 15B criteria for unintentional radiators [9].
- The end-product manufacturer must follow all the engineering and operating guidelines as specified by the grantee (u-blox).
- The JODY-W2 is for OEM integrators only.
- Only authorized antenna(s) may be used. Refer to JODY-W2 data sheet [2] for the list of authorized antennas. In the end-product, the JODY-W2 module must be installed in such a way that only authorized antennas can be used.
- The end product must use the specified antenna trace reference design, as described in the JODY-W2 antenna reference design application note [15].
- Any notification to the end user about how to install or remove the integrated radio module is NOT allowed.

⚠ If these conditions cannot be met or any of the operating instructions are violated, the u-blox regulatory authorization will be considered invalid. Under these circumstances, the integrator is responsible to re-evaluate the end-product including the JODY-W2 module and obtain their own regulatory authorization, or u-blox may be able to support updates of the u-blox regulatory authorization. See also Antenna requirements.

5.2 European Union regulatory compliance

JODY-W2 modules comply with the essential requirements and other relevant provisions of Radio Equipment Directive (RED) 2014/53/EU.

For information about the regulatory compliance of JODY-W2 modules against requirements and provisions in the European Union, see the JODY-W2 Declaration of Conformity [21].

5.2.1 CE End-product regulatory compliance

5.2.1.1 Safety standard

In order to fulfill the safety standard EN 60950-1 [8], the JODY-W2 module must be supplied with a Class-2 Limited Power Source.

[13] Formerly known as IC (Industry Canada).
[14] Approvals are still pending.

5.2.1.2 CE Equipment classes

In accordance with Article 1 of Commission Decision 2000/299/EC[15], JODY-W2 is defined as either Class-1 or Class-2 radio equipment, the end-product integrating JODY-W2 inherits the equipment class of the module.

☞ Guidance on end product marking, according to the RED can be found at: http://ec.europa.eu/

⚠ The EIRP of the JODY-W2 module must not exceed the limits of the regulatory domain that the module operates in. Depending on the host platform's implementation and antenna gain, integrators have to limit the maximum output power of the module through the host software. See Approved antennas for the list of approved antennas and Wi-Fi transmit output power limits for the corresponding maximum transmit power levels.

5.2.2 Compliance with the RoHS directive

JODY-W2 modules comply with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

5.3 Great Britain regulatory compliance

For information about the regulatory compliance of JODY-W2 modules against requirements and provisions in Great Britain, see also the JODY-W2 UKCA Declaration of Conformity [20].

5.3.1 UK Conformity Assessed (UKCA)

☞ The United Kingdom is made up of the Great Britain (including England, Scotland, and Wales) and Northern Ireland. Northern Ireland continues to accept the CE marking. The following notice is applicable to Great Britain only.

JODY-W2 modules have been evaluated against the essential requirements of the Radio Equipment Regulations 2017 (SI 2017 No. 1206, as amended by SI 2019 No. 696).

For guidance on end product marking in accordance with UKCA, see https://www.gov.uk/guidance/using-the-ukca-marking.

5.4 United States/Canada end-product regulatory compliance

u-blox represents that the modular transmitter fulfills the FCC/ISED regulations when operating in authorized modes on any host product given that the integrator follows the instructions as described in this document. Accordingly, the host product manufacturer acknowledges that all host products referring to the FCC ID or ISED certification number of the modular transmitter and placed on the market by the host product manufacturer need to fulfil all of the requirements mentioned below. Non-compliance with these requirements may result in revocation of the FCC approval and removal of the host products from the market. These requirements correspond to questions featured in the FCC guidance for software security requirements for U-NII devices, FCC OET KDB 594280 D02 [19].

⚠ The modular transmitter approval of JODY-W2, or any other radio module, does not exempt the end product from being evaluated against applicable regulatory demands.

[15] 2000/299/EC: Commission Decision of 6 April 2000 establishing the initial classification of radio equipment and telecommunications terminal equipment and associated identifiers.

The evaluation of the end product shall be performed with the JODY-W2 module installed and operating in a way that reflects the intended end product use case. The upper frequency measurement range of the end product evaluation is the 10th harmonic of 5.8 GHz as described in KDB 996369 D04.

The following requirements apply to all products that integrate a radio module:

- Subpart B - UNINTENTIONAL RADIATORS
  To verify that the composite device of host and module comply with the requirements of FCC part 15B, the integrator shall perform sufficient measurements using ANSI 63.4-2014.
- Subpart C - INTENTIONAL RADIATORS
  To validate that the fundamental and out of band emissions of the transmitter part of the composite device complies with the requirements of FCC part 15C, it is required that the integrator carries out sufficient verification measurements using ANSI 63.10-2013.

When the above requirements are fulfilled the end product manufacturer can use the authorization procedures, shown in Table 1 of 47 CFR Part 15.101, before marketing the end product. This means that the customer has to market the end product under a *Suppliers Declaration of Conformity (SDoC)*. Alternatively, the product must be certified by accredited test lab.

The description of the FCC regulatory requirements in this document comprise a subset of applicable publications maintained by the FCC Office of Engineering and Technology (OET) Knowledge Database (KDB). We recommend that integrators read the following list of KDB reference documents:

- KDB 178919 D01 Permissive Change Policy
- KDB 447498 D01 General RF Exposure Guidance
- KDB 594280 D01 Configuration Control
- KDB 594280 D02 U-NII Device Security
- KDB 784748 D01 Labelling Part 15 18 Guidelines
- KDB 996369 D01 Module certification Guide
- KDB 996369 D02 Module Q&A
- KDB 996369 D04 Module Integration Guide

5.4.1 United States compliance statement (FCC)

Table 31 shows the FCC IDs allocated to JODY-W2 modules.

Model[16]	FCC ID
JODY-W263-00A, JODY-W263-01A, JODY-W263-00B, JODY-W263-10B	XPYJODYW263

Table 31: FCC IDs for different variants of JODY-W2 modules

JODY-W2 modules have modular approval and comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

3. This device may not cause harmful interference, and
4. This device must accept any interference received, including interference that may cause undesired operation.

⚠ Any changes or modifications NOT explicitly APPROVED by u-blox could cause the JODY-W2 module to cease to comply with FCC rules part 15 thus void the user's authority to operate the equipment.

[16] The model name is identical to the ordering code. For details, see the JODY-W2 data sheet [2].

The internal / external antenna(s) used for this module must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

For FCC end poduct labeling requirements, see End product labeling requirements.

5.4.2 Canada compliance statement (ISED)

JODY-W2 modules are certified for use in accordance with the Canada Innovation, Science and Economic Development Canada (ISED) Radio Standards Specification (RSS) RSS-247 Issue 2 and RSS-Gen. Table 32 shows the ISED certification IDs allocated to JODY-W2 modules.

Model	ISED certification ID
JODY-W263-00A, JODY-W263-01A, JODY-W263-00B, JODY-W263-10B	8595A-JODYW263

Table 32: ISED IDs for different variants of JODY-W2 modules

JODY-W2 complies with ISED (Innovation, Science and Economic Development Canada)[17] license-exempt RSSs. Operation is subject to the following two conditions:

5. This device may not cause interference, and
6. This device must accept any interference, including interference that may cause undesired operation of the device.

☞ Any notification to the end user of installation or removal instructions about the integrated radio module is NOT allowed. Unauthorized modification could void authority to use this equipment.

This equipment complies with ISED RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator and your body.

This radio transmitter IC: 8595A-JODYW263 has been approved by ISED to operate with the antenna types listed in Approved antennas with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

☞ Operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

☞ Operation in the 5600-5650 MHz band is not allowed in Canada. High-power radars are allocated as primary users (i.e., priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

Le présent appareil est conforme aux CNR d'ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Cet équipement est conforme aux limites d'exposition de rayonnement d'ISED RSS-102 déterminées pour un environnement non contrôlé. Cet équipement devrait être installé et actionné avec la distance minimum 20 cm entre le radiateur et votre corps.

[17] Formerly known as IC (Industry Canada).

Cet émetteur radio, IC: 8595A-JODYW263 été approuvé par ISED pour fonctionner avec les types d'antenne énumérés dans la section Approved antennas avec le gain maximum autorisé et l'impédance nécessaire pour chaque type d'antenne indiqué. Les types d'antenne ne figurant pas dans cette liste et ayant un gain supérieur au gain maximum indiqué pour ce type-là sont strictement interdits d'utilisation avec cet appareil.

☞ Le dispositif de fonctionnement dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur pour réduire le risque d'interférences nuisibles à la co-canal systèmes mobiles par satellite

☞ Opération dans la bande 5600-5650 MHz n'est pas autorisée au Canada. Haute puissance radars sont désignés comme utilisateurs principaux (c.-àutilisateurs prioritaires) des bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer des interférences et / ou des dommages à dispositifs LAN-EL.

The internal / external antenna(s) used for this module must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

For ISED end poduct labeling requirements, see End product labeling requirements.

☞ The approval type for all JODY-W2 variants is a single modular approval. Due to ISED Modular Approval Requirements (Source: RSP-100 Issue 10), any application which includes the module must be approved by the module manufacturer (u-blox). The application manufacturer must provide design data for the review procedure.

5.4.3 Referring to the u-blox FCC/ISED certification ID

If the conditions in General requirements, FCC/ISED End-product regulatory compliance and all Antenna requirements are met, the u-blox modular FCC/ISED regulatory authorization is valid and the end-product may refer to the u-blox FCC ID and ISED certification number. U-blox may be able to support updates to the u-blox regulatory authorization; for example, adding new antennas to the u-blox authorization. See also Antenna requirements.

⚠ To use the u-blox FCC / ISED grant and refer to the u-blox FCC ID / ISED certification ID, the integrator must confirm to u-blox that all requirements associated with the Configuration control and software security of end-products are fulfilled.

5.4.4 Obtaining own FCC/ISED certification ID

Integrators who do not want to refer to the u-blox FCC/ISED certification ID, or who do not fulfil all requirements to do so may instead obtain their own certification. With their own certification, the integrator has full control of the grant to make changes.

Integrators who want to base their own certification on the u-blox certification can do so via a process called "Change in ID" (FCC) / "Multiple listing" (ISED). With this, the integrator becomes the grantee of a copy of the u-blox FCC/ISED certification. U-blox will support with an approval letter that shall be filed as a Cover Letter exhibit with the application.

☞ For modules where the FCC ID / ISED certification ID is printed on the label, the integrator must replace the module's label with a new label containing the new FCC/ISED ID. For a description of the labeling requirements, refer to the JODY-W2 series data sheet [2].

☞ It is the responsibility of the integrator to comply with any upcoming regulatory requirements.

5.4.5 Antenna requirements

In addition to the general requirement to use only authorized antennas, the u-blox grant also requires a separation distance of at least 20 cm from the antenna(s) to all persons. The antenna(s) must not be co-located with any other antenna or transmitter (simultaneous transmission) as well. If this cannot be met, a Permissive Change as described below must be made to the grant.

☞ In order to support verification activities that may be required by certification laboratories, customers applying for Class-II Permissive changes must implement the setup described in Software and the Radio Test Guide for NXP based modules [14].

5.4.5.1 Separation distance

If the required separation distance of 20 cm cannot be fulfilled, a SAR evaluation must be performed. This consists of additional calculations and/or measurements. The result must be added to the grant file as a Class II Permissive Change.

5.4.5.2 Co-location (simultaneous transmission)

If the module is to be co-located with another transmitter, additional measurements for simultaneous transmission are required. The results must be added to the grant file as a Class II Permissive Change.

5.4.5.3 Adding a new antenna for authorization

If the authorized antennas and/or antenna trace design cannot be used, the new antenna and/or antenna trace designs must be added to the grant file. This is done by a Class I Permissive Change or a Class II Permissive Change, depending on the specific antenna and antenna trace design.

- Antennas of the same type and with less or same gain as an already approved antenna can be added under a Class I Permissive Change.
- Antenna trace designs deviating from the u-blox reference design and new antenna types are added under a Class II Permissive Change.
- For 5 GHz modules, the combined minimum gain of antenna trace and antenna must be greater than 0 dBi to comply with DFS testing requirements.

⚠ Integrators with the intention to refer to the u-blox FCC ID / ISED certification ID must send an email to the support team email address for your area, as listed in the Contact section to discuss the Permissive Change Process. Class II Permissive Changes will be subject to NRE costs.

5.4.6 Configuration control and software security of end-products

☞ “Modular transmitter” hereafter refers to JODY-W263 (FCC ID XPYJODYW263).

As the end-product must comply with the requirements addressed by the OET KDB 594280 [18], the host product integrating JODY-W2 must comply with the following requirements:

- Upon request from u-blox, the host product manufacturer will provide all of the necessary information and documentation to demonstrate how the requirements listed below are met.
- The host product manufacturer will not modify the modular transmitter hardware.

- The configuration of the modular transmitter when installed into the host product must be within the authorization of the modular transmitter at all times and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host product. The Wi-Fi Tx output power limits must be followed. In particular, the modular transmitter installed in the host product will not have the capability to operate on the operating channels/frequencies referred to in the section(s) below, namely one or several of the following channels: 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz). The channels 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz) are allowed to be used only for modules that are certified for the usage ("modular transmitter"). Customers must verify that the module in use is certified as supporting DFS client/master functionality.
- The host product uses only authorized firmware images provided by u-blox and/or by the manufacturer of the RF chipset used inside the modular transmitter.
- The configuration of the modular transmitter must always follow the requirements specified in Operating frequencies and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host product.
- The modular transmitter must when installed into the host product have a regional setting that is compliant with authorized US modes and the host product is protected from being modified by third parties to configure unauthorized modes of operation for the modular transmitter, including the country code.
- The host product into which the modular transmitter is installed does not provide any interface for the installer to enter configuration parameters into the end product that exceeds those authorized.
- The host product into which the modular transmitter is installed does not provide any interface to third parties to upload any unauthorized firmware images into the modular transmitter and prevents third parties from making unauthorized changes to all or parts of the modular transmitter device driver software and configuration.

☞ The OET KDB 594280 D01 [18] lists the topics that must be addressed to ensure that the end-product specific host meets the Configuration Control requirements.

☞ The OET KDB 594280 D02 [19] lists the topics that must be addressed to ensure that the end-product specific host meets the Software Security Requirements for U-NII Devices.

5.4.7 Operating frequencies

JODY-W2 802.11b/g/n operation outside the 2412–2462 MHz band is prohibited in the US and Canada and 802.11a/n/ac operation in the 5600–5650 MHz band is prohibited in Canada. Configuration of the module to operate on channels 12–13 and 120–128 must be prevented accordingly. The allowed channels are described in Table 33.

Channel number	Channel center frequency [MHz] [18]	Allowed channels	Remarks
1 – 11	2412 – 2462	Yes	
12 – 13	2467 – 2472	No	
36 – 48	5180 – 5240	Yes	Canada (ISED): Devices are restricted to indoor operation only and the end product must be labelled accordingly.
52 – 64	5260 – 5320	Yes	
100 – 116	5500 – 5580	Yes	
120 – 128	5600 – 5640	No	USA (FCC): Client device operation allowed under KDB 905462
132 – 144	5660 – 5700	Yes	
149 – 165	5745 – 5825	Yes	

Table 33: Allowed channel usage under FCC/ISED regulation

☞ 15.407 (j) Operator Filing Requirement:
Before deploying an aggregate total of more than one thousand outdoor access points within the 5.15–5.25 GHz band, parties must submit a letter to the Commission acknowledging that, should harmful interference to licensed services in this band occur, they will be required to take corrective action. Corrective actions may include reducing power, turning off devices, changing frequency bands, and/or further reducing power radiated in the vertical direction. This material shall be submitted to Laboratory Division, Office of Engineering and Technology, Federal Communications Commission, 7435 Oakland Mills Road, Columbia, MD 21046. Attn: U-NII Coordination, or via Web site at https://www.fcc.gov/labhelp with the subject line: “U-NII-1 Filing”.

5.4.8 End product labeling requirements

For an end-product using the JODY-W2, there must be a label containing, at least, the following information:

This device contains
FCC ID: (XYZ)(UPN)
IC: (CN)-(UPN)

(XYZ) represents the FCC “Grantee Code”, this code may consist of Arabic numerals, capital letters, or other characters, the format for this code will be specified by the Commission’s Office of Engineering and Technology[19]. (CN) is the Company Number registered at ISED. (UPN) is the Unique Product Number decided by the grant owner.

The label must be affixed on an exterior surface of the end product such that it will be visible upon inspection in compliance with the modular labeling requirements of OET KDB 784748. The host user manual must also contain clear instructions on how end users can find and/or access the FCC ID of the end product.

The label on the JODY-W2 module containing the original FCC ID acquired by u-blox can be replaced with a new label stating the end-product’s FCC/ISED ID in compliance with the modular labeling requirements of OET KDB 784748.

FCC end product labeling

The outside of final products containing the JODY-W2 module must display in a user accessible area a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains Transmitter Module FCC ID: XPYJODYW263” or “Contains FCC ID: XPYJODYW263”.

[18] Under ISED regulations, operation in the band 5150–5250 MHz is for indoor use only and the end product must be labelled accordingly.
[19] 47 CFR 2.926

In accordance with 47 CFR § 15.19, the end product shall bear the following statement in a conspicuous location on the device:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: This device may not cause harmful interference, and This device must accept any interference received, including interference that may cause undesired operation.

ISED end product labeling

The ISED certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host device must be labeled to display the ISED certification number for the module, preceded by the words “Contains transmitter module”, or the word “Contains”, or similar wording expressing the same meaning, as follows: “Contains transmitter module IC: 8595A-JODYW263”.

L’étiquette d’homologation d’ISED d’un module donné doit être posée sur l’appareil hôte à un endroit bien en vue en tout temps. En l’absence d’étiquette, l’appareil hôte doit porter une étiquette sur laquelle figure le numéro d’homologation du module d’ISED, précédé des mots « Contient un module d’émission », ou du mot « Contient », ou d’une formulation similaire allant dans le même sens et qui va comme suit : « Contient le module d’émission IC: 8595A-JODYW263».

The end product shall bear the following statement in both English and French in a conspicuous location on the device:

Operation is subject to the following two conditions: this device may not cause interference, and this device must accept any interference, including interference that may cause undesired operation of the device.
Son utilisation est soumise aux deux conditions suivantes: Cet appareil ne doit pas causer d’interférences et il doit accepter toutes interférences reçues, y compris celles susceptibles d’avoir des effets indésirables sur son fonctionnement.

Labels of end products capable to operate within the band 5150–5250 MHz shall also include:

for indoor use only
Pour usage intérieur seulement

When the device is so small or for such use that it is not practicable to place the statements above on it, the information shall be placed in a prominent location in the instruction manual or pamphlet supplied to the user or, alternatively, shall be placed on the container in which the device is marketed. However, the FCC/ISED ID label must be displayed on the device as described above.

In case, where the final product will be installed in locations where the end-consumer is unable to see the FCC/ISED ID and/or this statement, the FCC/ISED ID and the statement shall also be included in the end-product manual.

5.5 NCC Taiwan compliance

5.5.1 Taiwan NCC Warning Statement

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。
低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。應避免影響附近雷達系統之操作。
系統廠商應於平台上標示「本產品內含射頻模組： JODY-W2 字樣。

Statement translation:

- Without permission granted by the NCC, any company, enterprise, or user is not allowed to change frequency, enhance transmitting power, or alter original characteristic as well as performance to an approved low power radio-frequency device.
- The low power radio-frequency devices shall not influence aircraft security and interfere legal communications; If any interference is found or suspected, the user shall immediately cease operating the equipment until the interference has been prevented. The said legal communications means radio communications is operated in compliance with the Telecommunications Act. The low power radio-frequency devices must be susceptible with the interference from legal communications or ISM radio wave radiated devices.

Table 34 shows the NCC certification IDs allocated to JODY-W2 modules.

Model	NCC ID
JODY-W263-01A	CCAJ22Y100F0T0
JODY-W263-00A	CCAJ22Y100F1T2
JODY-W263-00B	CCAJ22Y100F2T1
JODY-W263-10B	CCAJ22Y100F3T3

Table 34: NCC certification IDs for different variants of JODY-W2 modules

5.5.2 Labeling requirements for end products

End products based on JODY-W2 series modules and targeted for distribution in Taiwan must carry labels with the textual and graphical elements shown below.

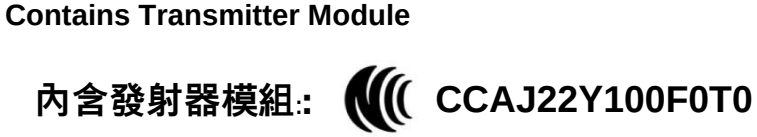


Figure 16: JODY-W263-01A

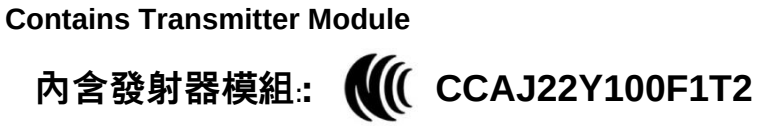


Figure 17: JODY-W263-00A

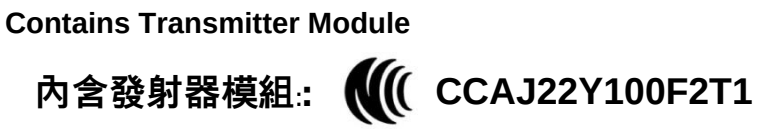


Figure 18: JODY-W263-00B

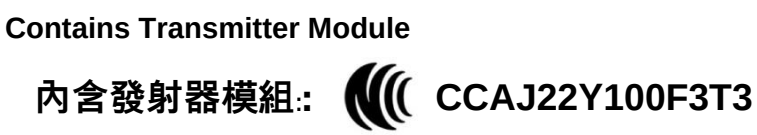


Figure 19: JODY-W263-10B

Other wording can be used, but only if the meaning of original messaging remains unchanged. The label must be physically attached to the product and made clearly visible for inspection.

5.6 Japan radio equipment compliance

5.6.1 Compliance statement

JODY-W2 series modules comply with the Japanese Technical Regulation Conformity Certification of Specified Radio Equipment (ordinance of MPT N°. 37, 1981), Article 2, Paragraph 1:

- Item 19 "2.4 GHz band wide band low power data communication system"
- Item 19-3 “Low power data communications system in the 5.2/5.3 GHz band”
- Item 19-3-2 “Low power data communications system in the 5.6 GHz band”

The JODY-W2 module is restricted on the Japanese market to be used indoors only if the product is operating in the 5.2/5.3 GHz band.

Table 35 shows the Giteki certification IDs allocated to JODY-W2 modules.

Model	Giteki ID
JODY-W263-00A, JODY-W263-01A, JODY-W263-00B	MIC ID: R 003-210312, MIC ID: T D210214003

Table 35: Giteki IDs for different variants of JODY-W2 modules

5.6.2 End product labelling requirement

End products based on JODY-W2 series modules and targeted for distribution in Japan must be affixed with a label with the “Giteki” marking, as shown in Figure 20. The “Indoor use only” information translated into Japanese below is mandatory if the product is operating in the 5.2/5.3 GHz band. The marking must be visible for inspection.

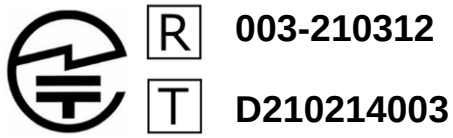


Figure 20: Giteki R and T marks with the JODY-W2 MIC certification numbers

5.7 KCC South Korea compliance

JODY-W2 series modules are certified by the Korea Communications Commission (KCC).

Table 36 shows the KCC certification IDs allocated to JODY-W2 modules.

Model	KCC ID
JODY-W263-00A, JODY-W263-01A, JODY-W263-00B, JODY-W263-10B	R-C-ULX-JODY-W263-01A

Table 36: KCC certification IDs for different variants of JODY-W2 modules

End products based on JODY-W2 series modules and targeted for distribution in South Korea must carry labels containing the KCC logo and certification number, as shown in Figure 21. This information must also be included in the product user manuals.



Figure 21: KCC marks with the JODY-W2 KCC certification numbers

☞ The height of the KCC logo must be at least 5 mm.

5.8 Australia and New Zealand regulatory compliance



JODY-W2 series modules are compliant with the Australian/New Zealand Industry Standard “AS/NZS 4268:2012/AMDT 1:2013 Radio equipment and systems – Short range devices – Limits and methods of standard measurement”. The standard is developed and maintained by the Australian Communications and Media Authority (ACMA).

JODY-W2 module test reports can be used to partly demonstrate that the application product meets the necessary performance requirements for using the Regulatory Compliance Mark (RCM). To satisfy the overall Australian and/or New Zealand compliance requirements on the end product, the integrator must create a compliance folder that contains all relevant compliance test reports.

For more information about Australian compliance, visit the Australian Communications and Media Authority web site http://www.acma.gov.au/.

For more information about New Zealand compliance, visit the New Zealand Radio Spectrum Management Group web site www.rsm.govt.nz.

5.9 Approved antennas

Refer to the JODY-W2 antenna reference design application note [15] for the specifications that must be fulfilled in the end product that uses radio type approval of the JODY-W2 module. The JODY-W2 antenna reference design application note provides PCB layout details and electrical specifications.

For Bluetooth and Wi-Fi operation in the 2.4 GHz band and Wi-Fi operation in the 5 GHz band, JODY-W2 has been tested and approved for use with the antennas listed in Table 37.

Manufacturer	Part number	Antenna type	Peak gain [dBi] / band		Validated regulatory domain
			2.4 GHz	5 GHz	
Linx	ANT-DB1-RAF-RPS [22]	Dual-band dipole antenna	2.5	4.6	FCC/ISED, ETSI, ACMA, NCC, KCC, Giteki
Linx	ANT-2.4-CW-RCT-RP [23]	Single-band dipole antenna	2.2	-	FCC/ISED, ETSI, ACMA, NCC, KCC, Giteki

Table 37: List of approved antennas

⚠ For compliance with FCC §15.407(a), the EIRP is not allowed to exceed 125 mW (21 dBm) at any elevation angle above 30° (measured from the horizon) when operated as an outdoor access point in U-NII-1 band, 5.150-5.250 GHz.

6 Product testing

6.1 u-blox in-line production testing

As part of our focus on high quality products, u-blox maintain stringent quality controls throughout the production process. This means that all units in our manufacturing facilities are fully tested and that any identified defects are carefully analyzed to improve future production quality.

The Automatic test equipment (ATE) deployed in u-blox production lines logs all production and measurement data – from which a detailed test report for each unit can be generated. Figure 22 shows the ATE typically used during u-blox production.

u-blox in-line production testing includes:

- Digital self-tests (firmware download, MAC address programming)
- Measurement of voltages and currents
- Functional tests (host interface communication)
- Digital I/O tests
- Measurement and calibration of RF characteristics in all supported bands, including RSSI calibration, frequency tuning of reference clock, calibration of transmitter power levels, etc.
- Verification of Wi-Fi and Bluetooth RF characteristics after calibration, like modulation accuracy, power levels, and spectrum, are checked to ensure that all characteristics are within tolerance when the calibration parameters are applied.



Figure 22: Automatic test equipment for module test

6.2 OEM manufacturer production test

As all u-blox products undergo thorough in-series production testing prior to delivery, OEM manufacturers do not need to repeat any firmware tests or measurements that might otherwise be necessary to confirm RF performance. Testing over analog and digital interfaces is also unnecessary during an OEM production test.

OEM manufacturer testing should ideally focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on application board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

In addition to this testing, OEMs can also perform other dedicated tests to check the device. For example, the measurement of module current consumption in a specified operating state can identify a short circuit if the test result deviates that from that taken against a “Golden Device”.

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and perform basic RF performance testing. Special manufacturing firmware can also be used to perform more advanced RF performance tests.

6.2.1 “Go/No go” tests for integrated devices

A “Go/No go” test compares the signal quality of the Device under Test (DUT) with that of “Golden Device” in a location with a known signal quality. This test can be performed after establishing a connection with an external device.

A very simple test can be performed by just scanning for a known Bluetooth low energy device and checking that the signal level (Received Signal Strength Indicator (RSSI) is acceptable.

☞ Tests of this kind may be useful as a “go/no go” test but are not appropriate for RF performance measurements.

Go/No go tests are suitable for checking communication between the host controller and the power supply. The tests can also confirm that all components on the DUT are well soldered.

A basic RF functional test of the device that includes the antenna can be performed with standard Bluetooth low energy devices configured as remote stations. In this scenario, the device containing JODY-W2 and the antennas should be arranged in a fixed position inside an RF shield box. The shielding prevents interference from other possible radio devices to ensure stable test results.

Appendix

A Reference schematic

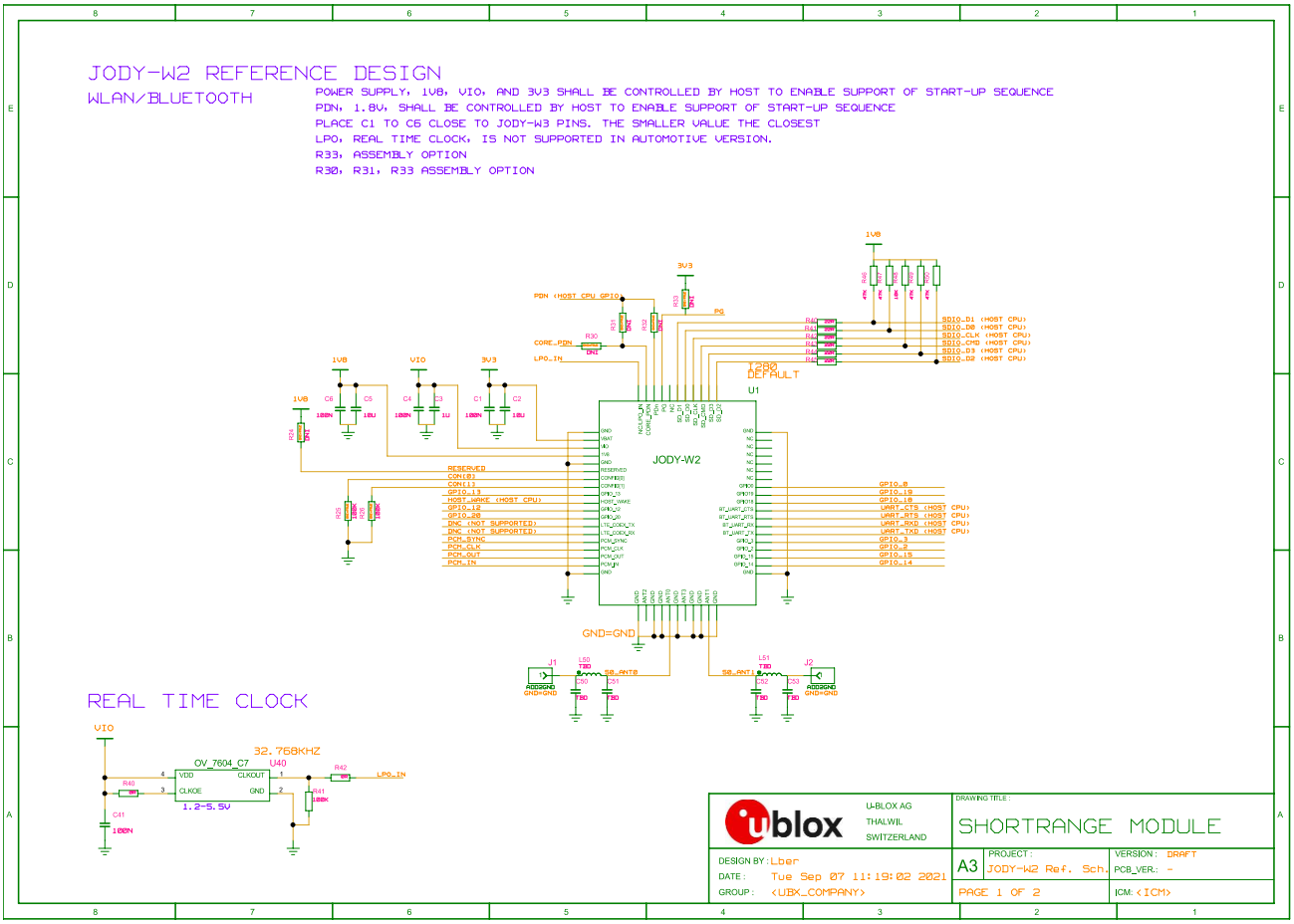


Figure 23: Reference design for JODY-W2

B Appendix: Wi-Fi Tx output power limits

B.1. FCC/ISED regulatory domain

B.1.1. Wi-Fi output power for 2.4 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
1 – 11	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	12 dBm
1	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	11 dBm
2 – 10	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	16 dBm
11	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	11 dBm
1	OFDM	20 MHz	HT20 MCS0-MCS7	11 dBm
2 – 10	OFDM	20 MHz	HT20 MCS0-MCS7	16 dBm
11	OFDM	20 MHz	HT20 MCS0-MCS7	11 dBm
3	OFDM	40 MHz	HT40 MCS0-MCS7	10 dBm
4	OFDM	40 MHz	HT40 MCS0-MCS7	11 dBm
5, 9	OFDM	40 MHz	HT40 MCS0-MCS7	12 dBm
6 – 8	OFDM	40 MHz	HT40 MCS0-MCS7	13 dBm

Table 38: FCC Wi-Fi power table for operation in the 2.4 GHz band

B.1.2. Wi-Fi output power for 5 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
36 – 64	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	15 dBm
36 – 64	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
36 – 64	OFDM	20 MHz	VHT20 MCS0-MCS8	15 dBm
38 – 62	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
38 – 62	OFDM	40 MHz	VHT40 MCS0-MCS9	15 dBm
42, 58	OFDM	80 MHz	VHT80 MCS0-MCS9	14 dBm

Table 39: FCC Wi-Fi power table for operation in the 5 GHz U-NII-1 and U-NII-2A bands

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
100 – 144	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	15 dBm
100 – 144	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
100 – 144	OFDM	20 MHz	VHT20 MCS0-MCS8	15 dBm
102	OFDM	40 MHz	HT40 MCS0-MCS7	14 dBm
102	OFDM	40 MHz	VHT40 MCS0-MCS9	14 dBm
110 – 142	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
110 – 142	OFDM	40 MHz	VHT40 MCS0-MCS9	15 dBm
106 – 138	OFDM	80 MHz	VHT80 MCS0-MCS9	14 dBm

Table 40: FCC Wi-Fi power table for operation in the 5 GHz U-NII-2e band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
149 – 165	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	15 dBm
149 – 165	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
149 – 165	OFDM	20 MHz	VHT20 MCS0-MCS8	15 dBm
151, 159	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
151, 159	OFDM	40 MHz	VHT40 MCS0-MCS9	15 dBm
155	OFDM	80 MHz	VHT80 MCS0-MCS9	14 dBm

Table 41: FCC Wi-Fi power table for operation in the 5 GHz U-NII-3 band

B.2. ETSI regulatory domain

B.2.1. Wi-Fi output power for 2.4 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
1 – 13	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	18 dBm
1 – 13	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	17 dBm
1 – 13	OFDM	20 MHz	HT20 MCS0-MCS7	17 dBm
3 – 9	OFDM	40 MHz	HT40 MCS0-MCS4	18 dBm
3 – 9	OFDM	40 MHz	HT40 MCS5-MCS7	17 dBm

Table 42: ETSI Wi-Fi power table for operation in the 2.4 GHz band

B.2.2. Wi-Fi output power for 5 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
36 – 64	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	15 dBm
36 – 64	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
36 – 64	OFDM	20 MHz	VHT20 MCS0-MCS8	15 dBm
38 – 62	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
38 – 62	OFDM	40 MHz	VHT40 MCS0-MCS7	15 dBm
38 – 62	OFDM	40 MHz	VHT40 MCS8-MCS9	14 dBm
42, 58	OFDM	80 MHz	VHT80 MCS0-MCS7	15 dBm
42, 58	OFDM	80 MHz	VHT80 MCS8-MCS9	14 dBm

Table 43: ETSI Wi-Fi power table for operation in the 5 GHz U-NII-1 and U-NII-2A bands

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
100 – 140	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	15 dBm
100 – 140	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
100 – 140	OFDM	20 MHz	VHT20 MCS0-MCS8	15 dBm
102 – 134	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
102 – 134	OFDM	40 MHz	VHT40 MCS0-MCS7	15 dBm
102 – 134	OFDM	40 MHz	VHT40 MCS8-MCS9	14 dBm
106, 122	OFDM	80 MHz	VHT80 MCS0-MCS7	15 dBm
106, 122	OFDM	80 MHz	VHT80 MCS8-MCS9	14 dBm

Table 44: ETSI Wi-Fi power table for operation in the 5 GHz U-NII-2e band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
149 – 165	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	13 dBm
149 – 165	OFDM	20 MHz	HT20 MCS0-MCS7	13 dBm
149 – 165	OFDM	20 MHz	VHT20 MCS0-MCS8	13 dBm
151, 159	OFDM	40 MHz	HT40 MCS0-MCS7	13 dBm
151, 159	OFDM	40 MHz	VHT40 MCS0-MCS9	13 dBm
155	OFDM	80 MHz	VHT80 MCS0-MCS9	13 dBm

Table 45: ETSI Wi-Fi power table for operation in the 5 GHz U-NII-3 band

B.3. Japan regulatory domain (Giteki)

B.3.1. Wi-Fi output power for 2.4 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
1 – 13	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	17 dBm
1 – 13	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	18 dBm
1 – 13	OFDM	20 MHz	HT20 MCS0-MCS7	18 dBm
3 – 9	OFDM	40 MHz	HT40 MCS0-MCS7	18 dBm

Table 46: Japan Wi-Fi power table for operation in the 2.4 GHz band

B.3.2. Wi-Fi output power for 5 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
36 – 64	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	15 dBm
36 – 64	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
36 – 64	OFDM	20 MHz	VHT20 MCS0-MCS8	15 dBm
38 – 62	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
38 – 62	OFDM	40 MHz	VHT40 MCS0-MCS7	15 dBm
38 – 62	OFDM	40 MHz	VHT40 MCS8-MCS9	14 dBm
42, 58	OFDM	80 MHz	VHT80 MCS0-MCS7	15 dBm
42, 58	OFDM	80 MHz	VHT80 MCS8-MCS9	14 dBm

Table 47: Japan Wi-Fi power table for operation in the 5 GHz U-NII-1 and U-NII-2A bands

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
100 – 144	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	15 dBm
100 – 144	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
100 – 144	OFDM	20 MHz	VHT20 MCS0-MCS8	15 dBm
102 – 142	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
102 – 142	OFDM	40 MHz	VHT40 MCS0-MCS7	15 dBm
102 – 142	OFDM	40 MHz	VHT40 MCS8-MCS9	14 dBm
106 – 138	OFDM	80 MHz	VHT80 MCS0-MCS7	15 dBm
106 – 138	OFDM	80 MHz	VHT80 MCS8-MCS9	14 dBm

Table 48: Japan Wi-Fi power table for operation in the 5 GHz U-NII-2e band

B.4. Korea regulatory domain (KCC)

B.4.1. Wi-Fi output power for 2.4 GHz band

Mode	Channel(s)	Maximum power setting
802.11b, CCK/DSSS	1 – 13	17 dBm
802.11g, OFDM	1 – 13	17 dBm
802.11n, HT20	1 – 13	17 dBm
802.11n, HT40	3 – 9	17 dBm

Table 49: Korea Wi-Fi power table for operation in the 2.4 GHz band

B.4.2. Wi-Fi output power for 5 GHz band

Mode	Channel(s)	Maximum power setting
802.11a, OFDM	36 – 44, 52 – 64, 100 – 144, 149 – 165	15 dBm
	48	13 dBm
802.11n, HT20	36 – 44, 52 – 64, 100 – 144, 149 – 165	15 dBm
	48	13 dBm
802.11ac, VHT20	36 – 44, 52 – 64, 100 – 144, 149 – 165	15 dBm
	48	13 dBm
802.11n, HT40	38 – 62, 102 – 142, 151, 159	15 dBm
802.11ac, VHT40, MCS0-7	38 – 62, 102 – 142, 151, 159	15 dBm
802.11ac, VHT40, MCS8-9	38 – 62, 102 – 142, 151, 159	14 dBm
802.11ac, VHT80, MCS0-7	42, 58, 106 – 138, 155	15 dBm
802.11ac, VHT80, MCS8-9	42, 58, 106 – 138, 155	14 dBm

Table 50: Korea Wi-Fi power table for operation in the 5 GHz bands

B.5. Taiwan regulatory domain (NCC)

B.5.1. Wi-Fi output power for 2.4 GHz band

Mode	Channel(s)	Maximum power setting
802.11b, CCK/DSSS	1	17 dBm
	2 – 11	19 dBm
802.11g, OFDM	1, 11	15 dBm
	2 – 10	18 dBm
802.11n, HT20	1	13 dBm
	2 – 10	18 dBm
	11	14 dBm
802.11n, HT40	3, 9	13 dBm
	4 – 8	16 dBm

Table 51: Taiwan Wi-Fi power table for operation in the 2.4 GHz band

B.5.2. Wi-Fi output power for 5 GHz band

Mode	Channel(s)	Maximum power setting
802.11a, OFDM	36 – 64, 100 – 140, 149 – 165	15 dBm
802.11n, HT20	36 – 64, 100 – 140, 149 – 165	15 dBm
802.11ac, VHT20	36 – 64, 100 – 140, 149 – 165	15 dBm
802.11n, HT40	46, 54, 102 – 134, 151, 159	15 dBm
	38, 62	13 dBm
802.11ac, VHT40, MCS0-7	46, 54, 102 – 134, 151, 159	15 dBm
802.11ac, VHT40, MCS8-9	46, 54, 102 – 134, 151, 159	14 dBm
802.11ac, VHT40	38, 62	13 dBm
802.11ac, VHT80	42	5 dBm
802.11ac, VHT80	58	9 dBm
802.11ac, VHT80	106	12 dBm
802.11ac, VHT80, MCS0-7	122, 155	15 dBm
802.11ac, VHT80, MCS8-9	122, 155	14 dBm

Table 52: Taiwan Wi-Fi power table for operation in the 5 GHz bands

C Glossary

Abbreviation	Definition
AEC	Automotive Electronics Council
AP	Access point
API	Application programming interface
ATE	Automatic test equipment
BT	Bluetooth
CDM	Charged device model
CE	European Conformity
CTS	Clear to send
DC	Direct current
DDR	Double data rate
DFS	Dynamic frequency selection
DHCP	Dynamic host ----configuration interface
EDR	Enhanced data rate
EEPROM	Electrically erasable programmable read-only memory
EIRP	Equivalent isotropic radiated power
ESD	Electrostatic discharge
FCC	Federal Communications Commission
FW	Firmware
GND	Ground
GPIO	General purpose input/output
HBM	Human body model
HS	High speed
HCI	Host controller interface
ISED	Innovation, Science and Economic Development Canada
I²C	Inter-Integrated Circuit
KDB	Knowledge database
LAN	Local area network
LDO	Low drop out
LED	Light-emitting diode
LPO	Low power oscillator
LTE	Long Term Evolution
MAC	Medium access control
MMC	Multimedia card
MWS	Mobile Wireless Standards
NRE	Non-recurring engineering
NSMD	Non solder mask defined
OEM	Original equipment manufacturer
OET	Office of Engineering and Technology
OS	Operating system
PCB	Printed circuit board
PCI	Peripheral component interconnect
PCIe	PCI Express
PCM	Pulse-code modulation
PHY	Physical layer (of the OSI model)

Abbreviation	Definition
PMU	Power management unit
RF	Radio frequency
RSDB	Real simultaneous dual band
RST	Request to send
SDIO	Secure digital input output
SMD	Solder mask defined
SMPS	Switching mode power supply
SMT	Surface-Mount Technology
SSID	Service set identifier
STA	Station
TBD	To be decided
THT	Through-hole technology
UART	Universal asynchronous receiver-transmitter
VCC	IC power-supply pin
VIO	Input offset voltage
VSDB	Virtual simultaneous dual band
VSWR	Voltage standing wave ratio
WFD	Wi-Fi Direct
WLAN	Wireless local area network
WPA	Wi-Fi Protected access
WAPI	WLAN Authentication and Privacy Infrastructure
SAE	Simultaneous Authentication of Equals

Table 53: Explanation of the abbreviations and terms used

Related documents

[1] u-blox Limited Use License Agreement (LULA-M)
[2] JODY-W2 series data sheet, UBX-18017567
[3] Packaging information reference guide, UBX-14001652
[4] IEC EN 61000-4-2 – Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
[5] ETSI EN 301 489-1 – Electromagnetic compatibility and Radio spectrum Matters (ERM); Electro Magnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
[6] IEC61340-5-1 – Protection of electronic devices from electrostatic phenomena – General requirements
[7] JEDEC J-STD-020E – Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices
[8] ETSI EN 60950-1:2006 – Information technology equipment – Safety – Part 1: General requirements
[9] FCC Regulatory Information, Title 47 – Telecommunication
[10] JESD51 – Overview of methodology for thermal testing of single semiconductor devices
[11] Android integration, application note, UBX-19035432
[12] JODY-W2 level shifter integration, application note, UBX-19034257
[13] EVK-JODY-W2, user guide, UBX-19027118
[14] Radio test guide for NXP based modules, application note, UBX-15014433
[15] JODY-W2 antenna reference design, application note, UBX-20053581
[16] Embedded Linux for i.MX Applications Processors
[17] NXP UM11490, Feature Configuration Guide for NXP-based Wireless Modules on i.MX 8M Quad EVK
[18] FCC guidance 594280 D01 Configuration Control v02 r01
[19] FCC guidance 594280 D02 U-NII Device Security v01r03
[20] JODY-W2 UKCA Declaration of Conformity, UBX-22030268
[21] JODY-W2 EU declaration of conformity, UBX-20053576
[22] ANT-DB1-RAF-XXX Data Sheet, Linx, https://linxtechnologies.com/wp/wp-content/uploads/ant-db1-raf-fff.pdf
[23] ANT-2.4-CW-RCT-XX Data Sheet, Linx, https://linxtechnologies.com/wp/wp-content/uploads/ant-2.4-cw-rct-cc.pdf

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Revision history

Revision	Date	Name	Comments
R01	10-Apr-2019	lber, aheg, mzes	Initial release.
R02	02-May-2019	kgom	Changed product status for JODY-W263-01A-00 to Prototype.
R03	21-May-2019	lber	Updated JODY-W2 module pin definition.
R04	03-Sep-2019	aheg	Added information about loading calibration data.
R05	05-May-2020	lber, aheg, mzes	Verification and update of the document with respect to different hardware and software features.
R06	25-Jun-2020	aheg	Fixed the command to download Bluetooth firmware using fw_loader with 3 MHz baud rate. Resolved some minor discrepancies between the datasheet and integration manual.
R07	7-Dec-2020	lber	Added references [12] and [13]. Removed antenna pins 2 and 3 from Figure 2 and updated Figure 7 to reflect latest antenna layout. Added antenna reference design to related documents.
R08	11-Dec-2020	mzes	Corrected product name and chipset references in document information and section 1.1.1.
R09	29-Jan-2021	aheg, lber	Revised Wi-Fi power states in Table 3, added power-up sequence diagram in section 1.3.1, configuration of Wi-Fi transmit power limits in section 3.7, and Rate group information for one spatial stream in Table 29. Included sleep mode configuration commands in section 3.11.10.
R10	26-Aug-2021	lber	Updated reference design schematic in Figure 15.
R11	25-Jan-2022	lber, mzes	Internal PU/PD added in Table 8 in Configuration pins. Updated Bluetooth to version 5.2. Added open-source and MCUXpresso in Available software packages. Updated Handling and soldering and Product testing chapters.
R12	06-May-2022	mzes	Updated regulatory output power limits for 2.4 GHz, 40 MHz in Table 38 and Table 42 according to certification reports.
R13	05-Oct-2022	sebs, mzes, lber	Added JODY-W263-10B variant. Updated Configuration control and software security of end-products. Added Wi-Fi Tx output power limits for Japan (Giteki), Korea (KCC), and Taiwan (NCC) regulatory domains. Updated host wake-up signals in Table 6. Clarified the Power-up sequence. Added thermal characterization parameter in Thermal guidelines. Updated contact information.
R14	05-Jun-2023	mzes	Updated Open-source Linux/Android drivers. Moved ESD specification for HBM and CDM to the data sheet. Added NCC Wi-Fi Tx output power limits for 5 GHz, VHT80. Updated RF transmission line design recommendations and contact information. Restructured Regulatory compliance section with rationalized content moved from the data sheet.

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