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JODY-W1 series

Host-based modules with Wi-Fi and dual-mode Bluetooth

System integration manual

Abstract

This integration manual describes JODY-W1 series modules with 2x2 MIMO 802.11n/ac and dual-mode Bluetooth® 5. JODY-W1 is ideal for in-vehicle-infotainment and telematics applications with simultaneous use cases requiring high data rates, such as in-car hotspots, Wi-Fi display applications such as Apple CarPlay, or video streaming across multiple clients. Connection to a host processor is through PCIe, SDIO, or high speed UART interfaces. It comes in an SMD form-factor, providing a complete solution for easy integration into the application.

UBX-16012621 - R19
C1-Public

Document information

Title	**JODY-W1 series**
Subtitle	Host-based modules with Wi-Fi and dual-mode Bluetooth
Document type	System integration manual
Document number	UBX-16012621
Revision and date	R19 27-Feb-2023
Disclosure Restriction	C1-Public

Document status description	
Draft	For functional testing. Revised and supplementary data will be published later.
Objective Specification	Target values. Revised and supplementary data will be published later.
Advance Information	Data based on early testing. Revised and supplementary data will be published later.
Early Production Information	Data from product verification. Revised and supplementary data may be published later.
Production Information	Document contains the final product specification.

This document applies to the following products:

Product name	**Document status**
JODY-W163-A	Initial production
JODY-W164-A	Initial production
JODY-W167-A	Initial production
JODY-W174-A	Engineering sample

For information about the related hardware, software, and status of listed product types, refer to the respective data sheet [2].

Contents

1 System description

1.1 Overview and applications

The JODY-W1 series is a range of compact modules based on the AEC-Q100-compliant Infineon CYW88359/CYW89359 (JODY-W16x) and CYW88459/CYW89459 (JODY-W17x) chipsets. The modules enable Wi-Fi, Bluetooth®, and Bluetooth low energy communication, and is thus ideal for in-vehicle-infotainment and telematics applications with simultaneous use cases requiring high data rates, such as in-car hotspots, Wi-Fi display applications such as Apple CarPlay, or video streaming across multiple clients. JODY-W1 modules can be operated in the following modes:

- Wi-Fi 2x2 MIMO 802.11n/ac in 2.4 GHz or 5 GHz
- Wi-Fi 1x1 802.11ac in 2.4 / 5 GHz real simultaneous dual band (RSDB)
- Dual-mode Bluetooth v5, including audio, can be operated simultaneously with both Wi-Fi modes

JODY-W1 undergoes extended automotive qualification according to ISO 16750-4 and is manufactured in line with ISO/TS 16949. Connection to a host processor is through PCIe, SDIO, or High-Speed UART interfaces. The JODY-W1 series modules are radio type approved for Europe, USA and Canada. Refer to the JODY-W1 series data sheet [2] for the complete list of approvals.

JODY-W1 series modules are suitable for a large number of automotive and industrial applications. Some example applications are shown in the list below.

Automotive applications

- In-car Access-Point for internet access
- Usage of in-car applications, such as Apple CarPlay, Miracast, etc.
- Rear-seat display
- Rapid sync-n-go applications and fast content download to the vehicle
- Hands-free equipment (Bluetooth)

Industrial applications

- Manufacturing floor automation, wireless control terminals and point-to-point backhaul
- Machine control
- Medical in-hospital applications
- Security and surveillance
- Outdoor content distribution
- Robust wireless connectivity in a broad range of industrial applications

1.1.1 Module architecture

Table 1 shows the available antenna and host interface configurations for JODY-W1 series module variants.

Product variant	LTE filter	Antenna configuration			Host interface
		ANT0	ANT1	ANT2	
JODY-W163-04A	-	2.4 GHz Bluetooth	2.4/5 GHz Wi-Fi (RSDB operation supported)	-	SDIO
JODY-W164-27A	•				
JODY-W163-13A	•	5 GHz Wi-Fi and 2.4 GHz Bluetooth (5 GHz 2x2 MIMO operation supported in single band mode)	2.4/5 GHz Wi-Fi (RSDB operation supported)	-	SDIO
JODY-W164-15A	•	2.4 GHz Bluetooth	2.4/5 GHz Wi-Fi (RSDB operation supported)	-	PCIe
JODY-W174-15A	•				
JODY-W164-03A	-	5 GHz Wi-Fi and 2.4 GHz Bluetooth (5 GHz 2x2 MIMO operation supported in single band mode)	2.4/5 GHz Wi-Fi (RSDB operation supported)	-	PCIe
JODY-W164-13A	•				
JODY-W174-03A	-				
JODY-W174-13A	•				
JODY-W174-12A	•				
JODY-W167-00A	-	2.4/5 GHz Wi-Fi (2x2 MIMO operation supported in single band mode)	2.4/5 GHz Wi-Fi (2x2 MIMO operation supported in single band mode)	2.4 GHz Bluetooth	PCIe
JODY-W167-03A	-				
	-				

Table 1: Supported configurations of the JODY-W1 module series

☞ Some JODY-W1 series modules use an LTE coexistence band-pass filter for BPF_1 (TDK B8343). All other band-pass filters are normal multilayer ceramic band-pass filters. Module variants equipped with an LTE coexistence filter, as shown in Table 2, are recommended when co-located with LTE devices operating in LTE bands 7, 38, 40, or 41.

The module host interface configuration is programmed in OTP memory during production.

Block diagrams of the JODY-W1 series modules are shown in Figure 1 and Figure 2.

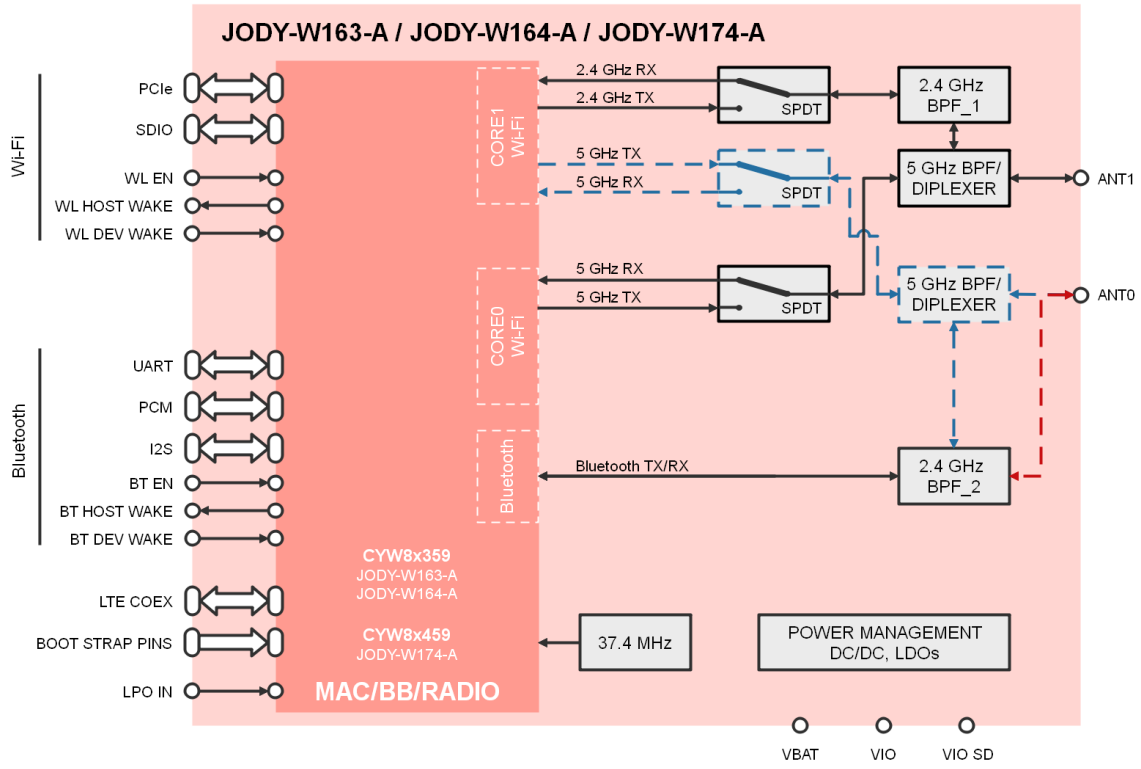

Figure 1: Block diagram of JODY-W163-A, JODY-W164-A, and JODY-W174-A

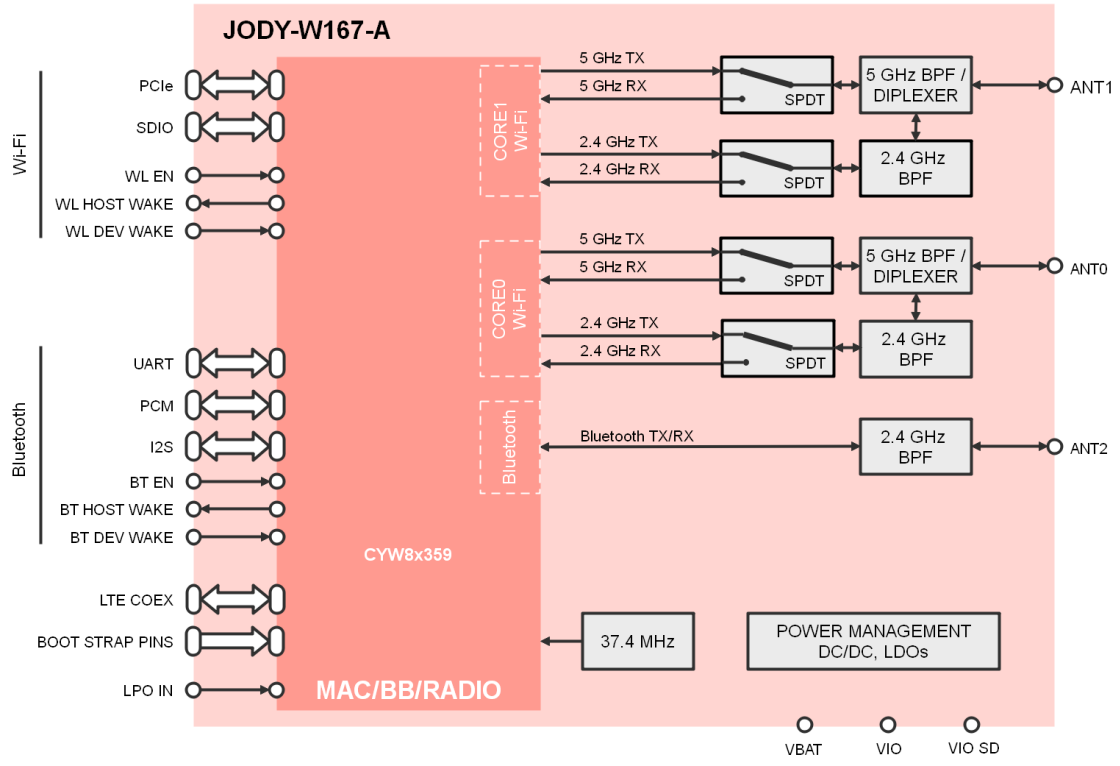

Figure 2: Block diagram of JODY-W167-A

1.1.2 Radio interfaces

JODY-W1 series modules support Wi-Fi 5 802.11a/b/g/n/ac and Bluetooth operations:

- JODY-W163/-W164/-W174 provide two antenna ports, one for dual band Wi-Fi (2.4 GHz and 5 GHz) and one for Bluetooth, shared with 5 GHz Wi-Fi on some variants. See also Table 1.
- JODY-W167 provides three antenna ports, two for dual band Wi-Fi (2.4 GHz and 5 GHz) and one dedicated for Bluetooth.

1.1.3 Power management

JODY-W1 series modules have different power management states. Guidelines for Wi-Fi and Bluetooth operations in different power states are defined in Table 2.

General Status	Power State	Description
Power-Off	Not Powered	**VBAT** and **VIO/VIO_SD** supply not present or below operating range: module is switched off. **VIO** supply can be on in order to reduce leakage current from other devices connected to the I/O's.
Power Down	Power Down	The module is effectively powered off by shutting down all internal regulators. This is done by de-asserting WL_EN and BT_EN. The chip is brought out of this mode by external logic re-enabling the internal regulators. The WL_EN and BT_EN pins can also be used for separate system reset.
Normal Operation	Deep Sleep	Most analog and digital domains of the chip and most of the regulators are powered off. All main clocks are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. Upon a wake-up event triggered by the PMU timers, an external interrupt, or a host resume through the SDIO bus, logic states in the digital core are restored to their pre-deep-sleep settings to avoid lengthy HW re-initialization. In deep sleep mode, the main source of power consumption is leakage current.
	Active	All blocks are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.

Table 2: Description for Wi-Fi power states

1.2 Pin configuration and function

1.2.1 Pin attributes

1. **Function:** Pin function.
2. **Pin name:** The name of the package pin or terminal.
3. **Pin number:** Package pin numbers associated with each signals.
4. **Power:** The voltage domain that powers the pin
5. **Type:** Signal type description:

I = Input	PD = Internal Pull-Down	PWR = Power
I/O = Input and Output	RF = Radio interface	PU = Internal Pull-Up
DS = Differential	O = Output	H = High-Impedance pin
GND = Ground	OD = Open drain	

6. **Signal name:** The signal name for that pin in the mode being used.
7. **Remarks:** Pin description and notes.

1.2.2 Pin list

Figure 3 and Table 3 list the pin-out of the JODY-W1 module, with pins grouped by function.

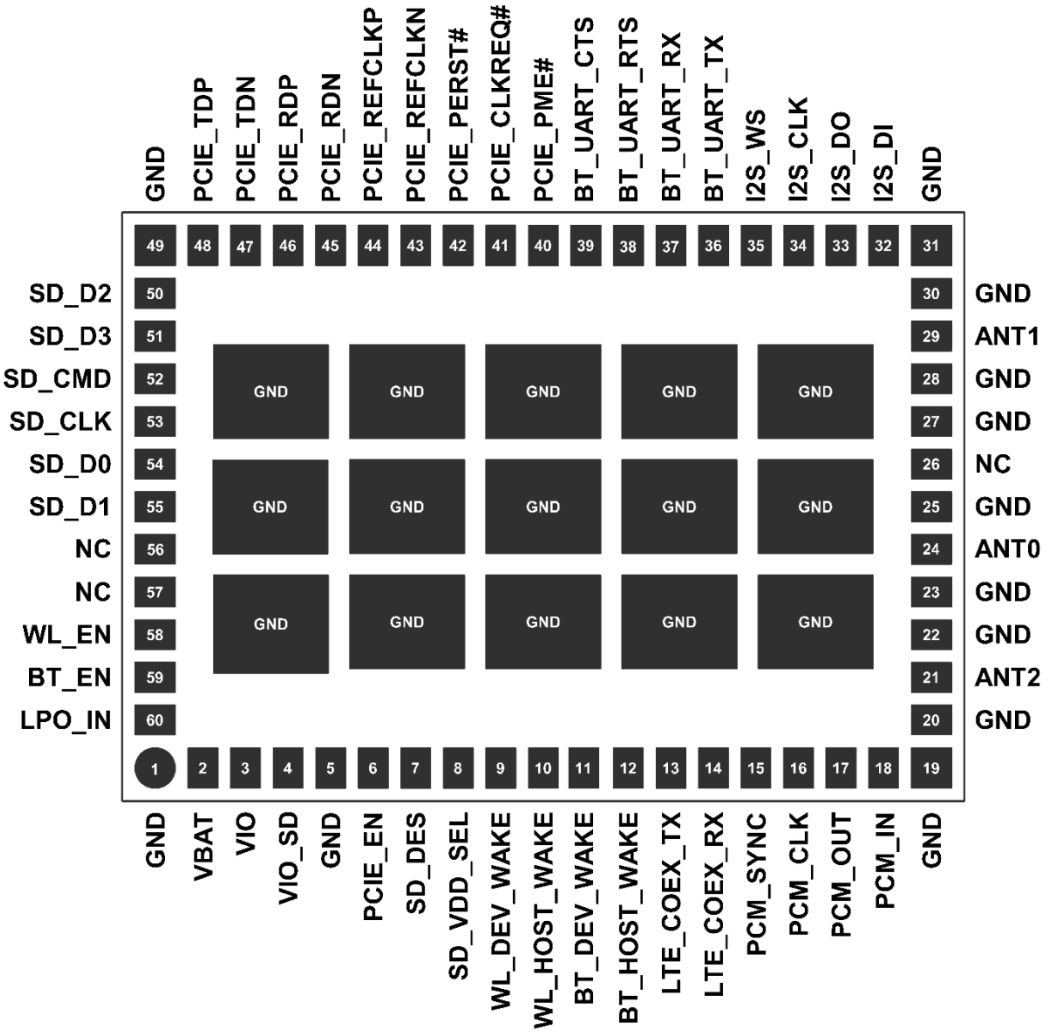

Figure 3: JODY-W1 pin assignment (top view)

Function	Pin name	Pin no.	Power	Type	Signal name	Remarks	Active	Power down
Power	VBAT	2	VBAT	PWR	Module supply input	Voltage supply range: 3.2 V – 4.8 V	VBAT	VBAT
	VIO	3	VIO	PWR	VIO supply	Nominal supply range: 1.8 V or 3.3 V	VIO	VIO
	VIO_SD	4	VIO_SD	PWR	VIO supply for SDIO	Nominal supply range: 1.8 V or 3.3 V. Also used for PCIe out-of-band signals.	VIO_SD	VIO_SD
	GND	1, 5, 19, 20, 22, 23, 25, 27, 28, 30, 31, 49	GND	GND			GND	GND
	Exposed Pins	-	GND	GND		Connect to Ground	GND	GND
Digital	SD_CLK	53	VIO_SD	I	SDIO Clock	SDIO Clock input	I	Tristate
	SD_CMD	52	VIO_SD	I/O	SDIO Command	SDIO command line	I/O	Tristate
	SD_D0	54	VIO_SD	I/O	SDIO data 0	SDIO data line bit [0]	I/O	Tristate
	SD_D1	55	VIO_SD	I/O	SDIO data 1	SDIO data line bit [1]	I/O	Tristate
	SD_D2	50	VIO_SD	I/O	SDIO data 2	SDIO data line bit [2]	I/O	Tristate
	SD_D3	51	VIO_SD	I/O	SDIO data 3	SDIO data line bit [3]	I/O	Tristate
	PCIE_REFCLKN	43	-	I	PCIe 100 MHz clock differential input	AC coupling capacitors 100 pF included in the module	I	Disabled
	PCIE_REFCLKP	44	-	I			I	Disabled
	PCIE_RDN	45	-	I	PCIe receiver differential input	DC coupled inputs. Place 100 nF AC coupling capacitors close to the host TDN/TDP differential output.	I	Disabled
	PCIE_RDP	46	-	I			I	Disabled
	PCIE_TDN	47	-	O	PCIe transmitter differential output	AC coupling capacitors100 nF included in the module. Connect to the host RDN/RDP differential input directly.	O	Tristate
	PCIE_TDP	48	-	O			O	Tristate
	BT_UART_TX	36	VIO	O	UART TX	BT UART, connect to Host RX	O	Tristate
	BT_UART_RX	37	VIO	I	UART RX	BT UART, connect to Host TX	I	Tristate
	BT_UART_RTS	38	VIO	O	UART RTS	BT UART, connect to Host CTSn	O	Tristate
	BT_UART_CTS	39	VIO	I	UART CTS	BT UART, connect to Host RTSn	I	Tristate
	PCM_CLK	16	VIO	I/O	PCM clock	Input if slave, Output if master Alternate function: I2S clock	I/O	Tristate
	PCM_SYNC	15	VIO	I/O	PCM Frame Sync	Input if slave, Output if master Alternate function: I2S Word Select	I/O	Tristate
	PCM_IN	18	VIO	I	PCM data in	Alternate function: I2S data in	I	Tristate
	PCM_OUT	17	VIO	O	PCM data out	Alternate function: I2S data out	O	Tristate
	I2S_CLK	34	VIO	I/O	I2S clock	Reserved for additional I2S interface. Do not connect. The I2S interface shares the pins with the PCM interface. Use the PCM pins to connect	I/O	Tristate
	I2S_WS	35	VIO	I/O	I2S Word Sel.		I/O	Tristate
	I2S_DI	32	VIO	I	I2S data in		I	Tristate
	I2S_DO	33	VIO	O	I2S data out		O	Tristate

Function	Pin name	Pin no.	Power	Type	Signal name	Remarks	Active	Power down
						an I2S interface for Bluetooth audio.		
	LTE_COEX_TX	13	VIO	O	UART TX	LTE coexistence UART[1]	O	Tristate
	LTE_COEX_RX	14	VIO	I	UART RX	LTE coexistence UART[1]	I	Disabled
Control	PCIE_EN	6	VIO	I	Configuration pin	See Table 7 for bootstrap configuration	I	Disabled
	SD_DES	7	VIO	I	Configuration pin	See Table 7 for bootstrap configuration	I	Disabled
	SD_VDD_SEL	8	VIO	I	Configuration pin	See Table 7 for bootstrap configuration	I	Disabled
	WL_DEV_WAKE	9	VIO	I	Wi-Fi device wake-up signal input	Asserted: Wi-Fi device must wake-up or remain awake Deasserted: Wi-Fi device may sleep when the sleep criteria is met.	I	Tristate
	WL_HOST_WAKE	10	VIO	O	Wi-Fi Host wake-up signal output	Asserted: Host device must wake-up or remain awake Deasserted: Host device may sleep when the sleep criteria is met	O	Tristate
	BT_DEV_WAKE	11	VIO	I	Bluetooth device wake-up signal	Asserted: Bluetooth device must wake-up or remain awake Deasserted: Bluetooth device may sleep when sleep criteria are met.	I	Tristate
	BT_HOST_WAKE	12	VIO	O	Bluetooth Host wake-up signal	Asserted: Host device must wake-up or remain awake Deasserted: Host device may sleep when sleep criteria are met	O	Tristate
	PCIE_PME#	40	VIO_SD	OD	PCIe control signal	PCIe power management event output	OD	OD
	PCIE_CLKREQ#	41	VIO_SD	OD	PCIe control signal	PCIe clock request signal	OD	OD
	PCIE_PERST#	42	VIO_SD	I	PCIe control signal	PCIe System reset	I	Disable
	WL_EN	58	VIO	I/PD	Wi-Fi power enable		I/PD	I/PD
	BT_EN	59	VIO	I/PD	BT power enable		I/PD	I/PD
	LPO_IN	60	-	I	Sleep clock input	32.768 kHz clock input, fail safe pin.	I	I
Radio	ANT0	24	VBAT	RF	Antenna signal	See also Module architecture	RF	RF
	ANT1	29	VBAT	RF	Antenna signal	See also Module architecture	RF	RF
	ANT2	21	VBAT	RF	Antenna signal	See also Module architecture	RF	RF
Other	NC	26, 56, 57	-	-	Reserved	Do not connect	NC	NC

Table 3: JODY-W1 pinout grouped by function

Logical pin states are the same for active mode and sleep mode.

Do not apply any voltage to the digital, control, and radio signal groups while in Not Powered mode to avoid damaging the module.

[1] Not supported in current firmware releases

1.3 Supply interfaces

1.3.1 Main supply inputs

JODY-W1 series modules must be supplied through the **VBAT/VIO/VIO_SD** pins. All supply voltages used inside the modules are generated from the VBAT rail through internal DC/DC converters.

The current drawn by the JODY-W1 series through the **VBAT** pin can vary by several orders of magnitude depending on the operation mode and state. In connected mode, high-current consumption is expected at a maximum RF power level during Wi-Fi transmission. With the power saving configuration enabled, low current consumption is expected in the low power idle mode.

Supply voltages and other electrical requirements are shown in the JODY-W1 series data sheet [2].

Rail	Allowable ripple (peak to peak)[2] over DC supply			Current consumption, peak	
	10-100 kHz	100 kHz-1 MHz	>1 MHz		
VBAT (3.3 V)	65 mV_{pk-pk}	25 mV_{pk-pk}	10 mV_{pk-pk}	Wi-Fi: BT:	1050 mA 60 mA
VIO + VIO_SD	65 mV_{pk-pk}	25 mV_{pk-pk}	10 mV_{pk-pk}	400 µA	

Table 4: Summary of voltage supply requirements

The JODY-W1 series modules can be powered by one of the following DC supplies:

- Switching Mode Power Supply (SMPS)
- Low Drop Out (LDO) regulator

The SMPS is the ideal choice when the available primary supply source has higher value than the operating supply voltage of the JODY-W1 series modules. The use of SMPS provides the best power efficiency for the overall application and minimizes current drawn from the main supply source.

⚠ While selecting the SMPS, ensure that the AC voltage ripple at switching frequency does not violate the requirements as specified in Table 4. Layout shall be implemented to minimize the impact of high frequency ringing. See also Guidelines for VCC supply circuit design using a switching regulator.

The use of an LDO linear regulator is convenient for a primary supply with a relatively low voltage where the typical 85-90% efficiency of the switching regulator leads to minimal current saving. Linear regulators are not recommended for high voltage step-down as they will dissipate a considerable amount of energy.

Independent of the selected DC power supply, it is crucial that it can handle the high peak current generated by the module. It is recommended to provide at least 20% margin overstated peak current when designing the power supply for this module.

[2] Ripple measured on the power connectors of u-blox EVK.

1.3.2 Power-up sequence

Figure 4 shows the recommended power sequence of the module. When **WL_EN** and **BT_EN** pins are driven by the host, it is required to apply at least 60 µs delay (two 32.768 clock cycles) with respect to **VBAT/VIO/VIO_SD** ramp-up.

⚠ Partial power down of the module is not allowed.

Parameter	Min.	Typ.	Max.	Unit	Remarks
t_dly	0	-	-	ms	VIO or VIO_SD should NOT be present before VBAT is high.
T_ramp-up	40	-	-	µs	All Power rails should not rise 10%-90% faster than 40 µs.
t_PD	60	-	-	µs	Power down signals release delay.
T_init	150	-	-	ms	Waiting time before initiating SDIO/PCIe access.

Table 5: Power sequence timings

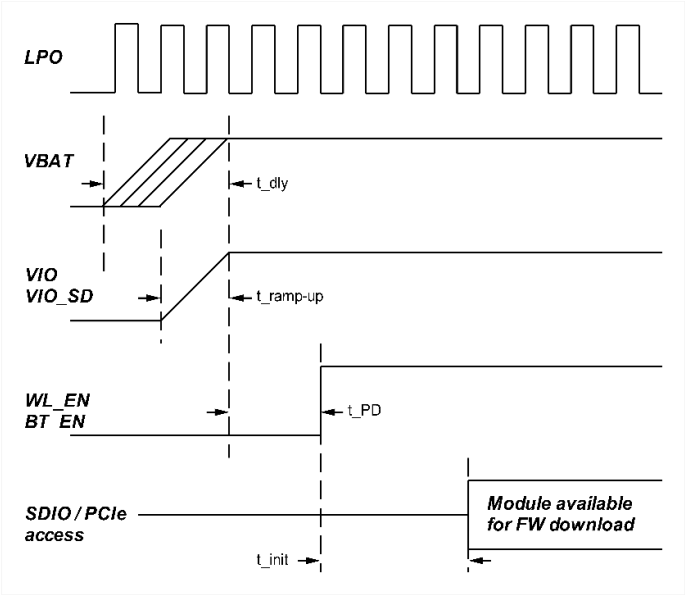

Figure 4: Power sequence of JODY-W1 module

The **WL_EN** and **BT_EN** signals should be kept low during startup (internal pull-down) and driven high when the power is stable or later when the module must be turned on. Those signals are powered by **VIO** voltage domain.

☞ Power down mode can be entered only by **WL_EN** and **BT_EN** deassertion by the host.

☞ The 32.768 kHz clock signal can be applied to the **LPO** pin before **VBAT** ramp-up.

1.4 System function interfaces

1.4.1 Module Power-on

The power-on sequence of a JODY-W1 series module can be initiated by applying the respective voltage to **VBAT/VIO/VIO_SD** supply pins and asserting the two **EN** signals (logic level 1). Firmware download is required each time **WL_EN** or **BT_EN** are asserted. External reset is not needed for proper operation due to internal power-up reset logic though it can be used by the host controller through the **WL_EN / BT_EN** in case of an abnormal module behavior.

1.4.2 Module Power-off

The JODY-W1 modules can enter **Power Down** mode by de-asserting WL_EN and BT_EN signals. After de-assertion, power on VBAT/VIO/VIO_SD can be removed to enter **Power Off** mode.

1.4.3 Wake-up signals

JODY-W1 modules provide several wake-up signals to handle low power modes for both Wi-Fi and Bluetooth as described in Table 6:

- **WL_DEV_WAKE** (Wi-Fi only): Host-to-module wake-up signal from Deep Sleep mode (input)
- **WL_HOST_WAKE** (Wi-Fi only): Module-to-host wake-up signal that can be used to exit Host from Deep Sleep modes and out-of-band SDIO interrupt signaling (output)
- **BT_DEV_WAKE** (Bluetooth only): Host-to-Module wake-up signal from Deep Sleep mode (input)
- **BT_HOST_WAKE** (Bluetooth only): Module-to-host wake-up signal that can be used to exit Host from Deep Sleep modes (output)

The wakeup signals are powered by **VIO** voltage domain. For information about how to configure the Bluetooth sleep mode, see also PCM/I2S audio interface configuration.

Name	I/O	Description
WL_DEV_WAKE	I	Host-to-Module Wake-Up signal, Wi-Fi interface
WL_HOST_WAKE	O	Module-to-Host Wake-Up signal, Wi-Fi interface
BT_DEV_WAKE	I	Host-to-Module Wake-Up signal, Bluetooth interface
BT_HOST_WAKE	O	Module-to-Host Wake-Up signal, Bluetooth interface

Table 6: Wake-up signal definition

1.4.4 Host interface configuration

A JODY-W1 series module uses the **PCIE_EN/SD_DES/SD_VDD_SEL** pins as host interface configuration input to set the desired operation mode following a Power on sequence. To configure the pins for a certain module operation mode, you need to provide a 10 kΩ pull down resistor to the ground. No external circuitry is required to set a configuration pin to high logical level.

Bootstrap configuration options are listed in Table 7 and are used to determine the configuration of communication busses and host-side drivers.

- **PCIe** mode: Commands and data regarding the Wi-Fi traffic will be transferred through the PCI express bus to the module.
- **SDIO** mode: Commands and data regarding the Wi-Fi traffic will be transferred through the SDIO bus to the module. The SDIO operates at the voltage selected by the strap option.
- Other configurations are reserved.

The configuration signals are powered by the **VIO** voltage domain.

PCIE_EN (pin 6)	SD_DES (pin 7)	SD_VDD_SEL (pin 8)	VIO_SD supply (pin 4)	Wi-Fi interface
1	1	1	3.3 V or 1.8 V[3]	PCIe
0	0	1	1.8 V	1.8V SDIO
0	0	0	3.3 V	3.3V SDIO

Table 7: Bootstrap configuration options

⚠ The available host interface depends on the product variant. See Table 1 for the host interfaces supported for different JODY-W1 module variants.

[3] The PCIe control pins of the PCIe bus are powered by the VIO_SD voltage domain.

⚠ When SDIO modes are selected, the host interface signal voltage must match the voltage provided on the VIO_SD domain during both card identification process and data transfer mode.

1.5 Data communication interfaces

JODY-W1 series modules use PCI express v3.0, SDIO 3.0 and high-speed UART as host interfaces. The Wi-Fi traffic will always be communicated via the PCI express or the SDIO host interface while the Bluetooth traffic via the UART interface only.

1.5.1 PCIe 3.0 interface

JODY-W1 modules include a PCIe v3.0-compliant interface running at Gen1 speeds and allow a host controller using the PCIe bus protocol to access the Wi-Fi function. Table 8 describes the PCIe interface signals.

Name	I/O	Description	Remarks
PCIE_REFCLKN	I	100MHz clock negative input	AC coupling capacitors 100 pF included to the module
PCIE_REFCLKP	I	100MHz clock positive input	
PCIE_RDN	I	Receiver negative input	Module has no AC coupling capacitors (DC coupled inputs). Place 100 nF AC coupling capacitors close to the Host TDN/TDP output.
PCIE_RDP	I	Receiver positive input	
PCIE_TDN	O	Transmitter negative output	AC coupling capacitors 100 nF included to the module. Connect to Host RDN/RDP inputs directly.
PCIE_TDP	O	Transmitter positive output	
PCIE_PME#	OD	Power management event output	Control pin, open drain. 10 KΩ pull-up must be provided on the Host side.
PCIE_CLKREQ#	OD	Clock request	Control pin, open drain. 10 KΩ pull-up must be provided on the Host side.
PCIE_PERST#	I	Interface reset	Control pin.

Table 8: PCI express signal definition

The PCIe control pins of the PCIe bus are powered by the **VIO_SD** voltage domain.

1.5.2 SDIO 3.0 interface

JODY-W1 series modules include an SDIO device interface compatible with the industry standard SDIO 3.0 specification (UHS-I, up to 104 Mbyte/s) and allows a host controller using the SDIO bus protocol to access the Wi-Fi function. The modules also support legacy modes like default speed and High-Speed modes.

⚠ SDIO supported modes may not be able to support the full throughput capability of the module. If maximum performance is needed, it is recommended to use the PCI express interface.

The module acts as a device on the SDIO bus. Table 9 summarizes the supported bus speed modes.

Bus speed mode	Max. bus speed [MB/s]	Max. clock frequency [MHz]	Signal voltage (VIO_SD) [V]
SDR104	104	208	1.8
SDR50	50	100	1.8
DDR50	50	50	1.8
SDR25	25	50	1.8
SDR12	12.5	25	1.8
High Speed	25	50	3.3
Default Speed	12.5	25	3.3

Table 9: SDIO supported rates for JODY-W1

Pull-up resistors are required for all SDIO data and command lines. These pull-up resistors can be provided either externally on the host PCB or internally in the host application processor. Depending on the routing of the SDIO lines on the host, termination resistors in series to the lines might also be needed. See also Data communication interfaces.

Name	I/O	Description	Remarks
SD_CLK	I	SDIO Clock input	
SD_CMD	I/O	SDIO Command line	External PU required
SD_D0	I/O	SDIO Data line bit [0]	External PU required
SD_D1	I/O	SDIO Data line bit [1]	External PU required
SD_D2	I/O	SDIO Data line bit [2]	External PU required
SD_D3	I/O	SDIO Data line bit [3]	External PU required

Table 10: SDIO signal definition

The SDIO host interface pins of the module are powered by the **VIO_SD** voltage domain.

1.5.3 High Speed UART interface

The JODY-W1 series modules support a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface with the following features:

- Two 1040-byte FIFO for transmit and receive to support BT EDR
- Bluetooth UART HCI transport specification: H4
- 2 pins for transmit and receive operations
- 2 flow control pins (RTS/CTS)
- Interrupt triggers for low-power, high throughput operation
- Supports standard baud rates and high throughput up to 4 Mbps. The default baud rate after reset is 115.2 kbaud.

An example of common baud rates supported by the UART interface is listed in Table 12. For proper operation, baud rate error must be kept within ±2%.

Name	I/O	Description	Remarks
BT_UART_TX	O	UART TX signal	Connect to Host RX
BT_UART_RX	I	UART RX signal	Connect to Host TX
BT_UART_RTS	O	UART RTS signal	Connect to Host CTS
BT_UART_CTS	I	UART CTS signal	Connect to Host RTS

Table 11: UART signal description

Desired Rate [kbaud]	Actual Rate [kbaud]	Error [%]
4000.0	4000.0	0.00
3692.0	3692.308	0.01
3000.0	3000.0	0.00
2000.0	2000.0	0.00
1500.0	1500.0	0.00
1444.444	1454.544	0.70
921.6	923.077	0.16
460.8	461.538	0.16
230.4	230.796	0.17
115.2	115.385	0.16
57.6	57.692	0.16
38.4	38.4	0.00

Desired Rate [kbaud]	Actual Rate [kbaud]	Error [%]
28.8	28.846	0.16
19.2	19.2	0.00
14.4	14.423	0.16
9.6	9.6	0.00

Table 12: Example of common baud rates

High Speed UART signals are powered by the **VIO** voltage domain.

1.5.4 PCM/I2S – Audio interfaces

JODY-W1 series modules provide two bi-directional 4-wire digital audio interfaces that can be used for digital voice/audio communication[4] with external digital audio devices like an audio codec. The PCM interface supports:

- Master or slave mode with up to 1024 kHz clock rate.
- 8 kHz or 16 kHz sample rate.
- PCM sample width size of 8 bit or 16 bit.
- Short frame and long frame synchronization.
- Burst mode at up to 24 MHz to reduce host processor load.

The I2S interface supports:

- Master (1.536 MHz or 2.4 MHz) or slave (any frequency up to 3.072 MHz is supported) mode.
- Channel word length: 16bit.

Name	I/O	Description	Remarks
PCM_CLK	I/O	PCM clock	Output if Master, Input if Slave Alternate function: I2S clock
PCM_SYNC	I/O	PCM frame sync	Output if Master, Input if Slave Alternate function: I2S word select
PCM_IN	I	PCM data out	Alternate function: I2S data out
PCM_OUT	O	PCM data in	Alternate function: I2S data in
I2S_CLK	I/O	I2S clock	Reserved for additional I2S interface. Do not connect. The I2S interface shares the pins with the PCM interface. Use the PCM pins to connect an I2S interface for Bluetooth audio
I2S_WS	I/O	I2S word select	
I2S_DI	I	I2S data in	
I2S_DO	O	I2S data out	

Table 13: PCM digital audio signal description

☞ The PCM pins of JODY-W1 series modules can be configured to either PCM or I2S operation mode through HCI commands. See also PCM/I2S audio interface configuration.

The PCM and I2S signals are powered by the **VIO** voltage domain.

[4] The two physical interfaces are mutually exclusive and cannot work simultaneously.

1.5.5 LTE Coexistence UART

The module supports an auxiliary UART for coexistence with other mobile radio technologies. [5]

Name	I/O	Description	Remarks
LTE_COEX_TX	O	WCI-2 UART TX signal	Connect to MWS device RX
LTE_COEX_RX	I	WCI-2 UART RX signal	Connect to MWS device TX

Table 14 : Auxiliary UART signal description

The signals shown in Table 14 are powered by the **VIO** voltage domain.

1.5.6 Low Power Oscillator

It is mandatory to connect an external low-frequency clock to the LPO_IN pin. This clock is used for low-power mode timing and a few other functions. The external LPO must meet the requirements listed in Table 16.

Name	I/O	Description	Remarks
LPO_IN	I	32.768 kHz clock input	Failsafe pin

Table 15: External 32.768 kHz sleep clock signal description

The LPO_IN pin is a failsafe input, clock signal that can be applied to the pin when the module is not powered provided that the requirements in Table 16 are fulfilled.

Parameter	LPO clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 – 70	%
Input signal accuracy	200 – 3300	mV, pkpk
Signal type	Square-wave or Sine-wave	-
Input impedance[6]	> 100	kΩ
	< 5	pF
Clock jitter (during startup)	< 10,000	ppm

Table 16: External 32.768 kHz sleep clock specification

1.6 Antenna interfaces

1.6.1 Wi-Fi and Bluetooth antennas

JODY-W1 modules provide different antenna configurations based on the selected product variant:

- JODY-W163/-W164/-W174 provide two pins for dual-band Wi-Fi and Bluetooth shared connectivity (**ANT0** and **ANT1**), where RSDB operation is supported on a single antenna pin (**ANT1**).
- JODY-W167 provides three pins for dual-band Wi-Fi operation (**ANT0** and **ANT1**) and dedicated Bluetooth connectivity (**ANT2**).

[5] Not supported in current firmware.
[6] When power is applied or switched off.

The following recommendations apply while developing an antenna interface for the JODY-W1 series module:

- Where possible, consider integrating the u-blox reference design in the end product to minimize the effort on the certification process. See JODY-W1 antenna reference design [12] for a full list of available reference designs.
- The **ANT0**, **ANT1** and **ANT2** pins have a nominal characteristic impedance of 50 Ω and must be connected to the external antennas through a 50 Ω transmission line to allow proper RF transmission and reception.
- Good isolation must be provided between the various antennas in the system. Special care should be taken to maximize isolation between antennas operating in the same or nearby bands.

For information about how to properly design circuits compliant with these requirements, see also Antenna interfaces.

1.6.2 Approved antenna designs

JODY-W1 series modules come with a pre-certified design that can be used to save costs and time during the certification process. To minimize this effort, the customer is required to implement antenna layout according to u-blox reference designs. Reference design source files can be provided on request by u-blox.

The designer integrating a u-blox reference design into an end-product is solely responsible for the Unintentional Emissions levels produced by the end-product. See also Regulatory compliance.

For Wi-Fi and Bluetooth operation, the module has been tested and approved for use with the antennas listed in the JODY-W1 series data sheet [2]. The module may be integrated with other antennas and in this case the designer should refer to the Regulatory compliance information that describes the certification options available to customers. For more information, also see the JODY-W1 antenna reference design [12].

1.7 Other remarks

1.7.1 Unused pins

JODY-W1 modules have pins reserved for future use (**NC**) that must be left unconnected on the application board.

2 Design-in

2.1 Overview

For an optimal integration of JODY-W1 series modules in the final application board, it is recommended to follow the design guidelines stated in this chapter. Every application circuit must be properly designed to ensure the correct functionality of the related interface, however a number of points require high attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

- Module antenna connection: **ANT0**, **ANT1** and **ANT2** pins.
  Antenna circuit affects the RF compliance of the device integrating JODY-W1 modules with applicable certification schemes. Follow the recommendations for schematic and layout design described in Antenna interfaces.
- Module supply: **VBAT**, **VIO/VIO_SD**, and **GND** pins.
  The supply circuit affects the RF compliance of the device integrating JODY-W1 modules with applicable certification schemes. Follow the recommendations described in Supply interfaces.
- High speed interfaces: **PCIe differential** pins and **SDIO** pins.
  High speed interfaces can be a source of radiated noise and can affect the compliance with regulatory standards for radiated emissions. Follow the General high speed layout guidelines and recommendations described in PCI express.
- System functions: pins indicated as **Control** pins in Table 3.
  Accurate design is required to ensure that the voltage level is well defined during module boot. Follow the schematic and layout, follow the General high speed layout guidelines.
- Other pins: High speed **UART**, **PCM**, **specific signals** and **NC** pins.
  Accurate design is required to ensure proper functionality. Follow the General high speed layout guidelines and General high speed layout guidelines for schematic and layout design.

⚠ It is recommended to check for radiated spurious emissions according ETSI EN 301 893 and ETSI EN 300 440 early during the design-in-process of the module. For implementation guidelines, see also Layout considerations to reduce spurious emissions.

2.2 Antenna interfaces

JODY-W1 modules provide three RF interfaces for connecting the external antennas. See Table 1 for the connectivity options available at each antenna port.

All the **ANTx** ports have a nominal characteristic impedance of 50 Ω and must be connected to the related antenna through a 50 Ω transmission line to allow proper impedance matching along the RF path. A bad termination of the antenna ports may result in poor performance of the module.

The isolation between the antennas should be maximized, the requirements specified in Table 17 and Table 18 should be followed to ensure good performance.

⚠ According to FCC regulations, the transmission line from the module's antenna pin to the antenna or antenna connector on the host PCB is considered part of the approved antenna design. To learn more about the customer options for simplifying the certification process, see also FCC/ISED End-product regulatory compliance.

2.2.1 RF transmission line design

RF transmission lines such as the ones from the **ANT0**, **ANT1** and **ANT2** pins up to the related antenna connectors must be designed so that the characteristic impedance is as close as possible to 50 Ω (max. ±10%).

Figure 5 shows the design options for implementing a transmission line, namely:

- Microstrip – track separated with dielectric material and coupled to a single ground plane.
- Coplanar microstrip – track separated with dielectric material and coupled to both the ground plane and side conductor.
- Strip – track separated by dielectric material and sandwiched between two parallel ground planes.

The parameters shown in the cross-sectional area of each trace design include:

- Width (W) – shows the width of the copper layer on the top layer
- Distance (S) – shows the distance between the top copper layer and the two adjacent GND planes.
- Dielectric substrate thickness (H) – shows the distance between the GND reference on the bottom plane and the copper layer on the top layer.
- Thickness of the copper layer (T) – can also be represented by "Base Copper Weight", which is commonly used as the parameter for PCB stack-up.
- Dielectric constant (ε_r) defines the ratio between the electric permeability of the material against the electric permeability of free space

☞ The width of a 50 Ω microstrip depends on mainly "ε_r" and "H", which must be calculated for each PCB layer stack-up.

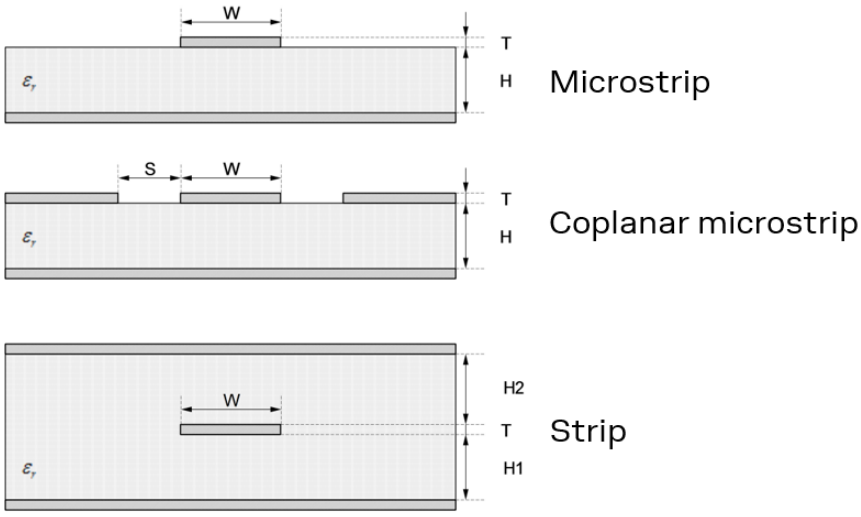

Figure 5: Transmission line trace design

To properly design a 50 Ω transmission line, the following remarks should be considered:

- The designer should provide enough clearance from surrounding traces and ground in the same layer; in general, a trace to ground clearance of at least two times the trace width should be considered, and the transmission line should be" guarded" by ground plane area on each side.
- The characteristic impedance can be calculated as first iteration using tools provided by the layout software. It is advisable to ask the PCB manufacturer to provide the final values that are usually calculated using dedicated software and available stack-ups from production. It could also be possible to request an impedance coupon on panel's side to measure the real impedance of the traces.

- FR-4 dielectric material, although its high losses at high frequencies can be considered in RF designs providing that:
  - RF trace length must be minimized to reduce dielectric losses.
  - If traces longer than few centimeters are needed, it is recommended to use a coaxial connector and cable to reduce losses.
  - Stack-up should allow for wide 50 Ω traces and at least 200 µm trace width is recommended to assure good impedance control over the PCB manufacturing process.
  - FR-4 material exhibits poor thickness stability and thus less control of impedance over the trace length. Contact the PCB manufacturer for specific tolerance of controlled impedance traces.
- For PCBs using components bigger than 0402 and dielectric thickness below 200 µm, it is recommended to add a keep-out (that is, clearance, a void area) on the ground reference layer below any pin present on the RF transmission lines to reduce parasitic capacitance to ground.
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: route RF lines in 45 ° angle.
- Add GND stitching vias around transmission lines as shown in Figure 6.
- Include a solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer. Include an adequate number of vias on the adjacent metal layer, as shown in Figure 5.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit to avoid crosstalk between RF traces and Hi-impedance or analog signals.
- Avoid stubs on the transmission lines, any component on the transmission line should be placed with the connected pin over the trace. Also avoid any unnecessary component on RF traces.

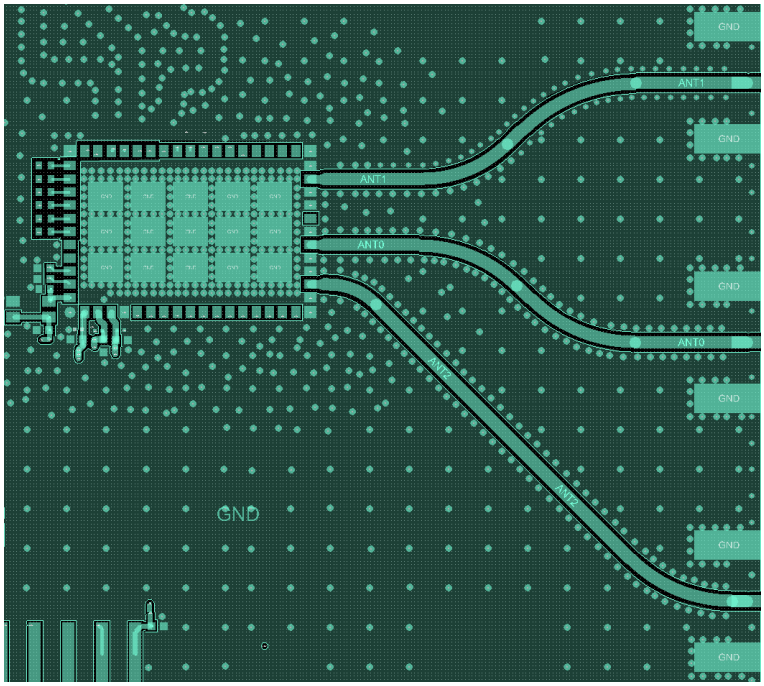

Figure 6: Example of RF trace and ground design

2.2.2 Antenna design

Designers must take care of the antennas from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating JODY-W1 module with all the applicable required certification schemes heavily depends on antennas radiating performance.

- External antennas such as linear monopole:
  - External antennas basically do not imply physical restriction to the design of the PCB where the module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected with minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces radiation performance and sensitivity.
  - A high quality 50 Ω coaxial connector provides proper PCB-to-RF-cable transition.
- Integrated antennas such as patch-like antennas:
  - Internal integrated antennas imply physical restriction to the PCB design:
    Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane related to the antenna element must be considered.
    The RF isolation between antennas in the system has to be as high as possible and the correlation between the 3D radiation patterns of the two antennas has to be as low as possible. In general, an RF separation of at least a quarter wavelength between the two antennas is required to achieve a minimum isolation and low pattern correlation; increased separation should be considered if possible, to maximize the performance and fulfil the requirements in Table 18.
    Find below a numerical example to estimate the physical restrictions on a PCB:
    Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.125 cm
  - Radiation performance depends on the whole product and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.

Table 17 summarizes the requirements for the antenna RF interface while Table 18 specifies additional requirements for dual antenna design implementation.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of Antenna pins.
Frequency Range	2400 – 2500 MHz 5150 – 5850 MHz	For 802.11b/g/n and Bluetooth. For 802.11a/n/ac.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the primary antenna RF connection matches the 50 Ω characteristic impedance of antenna pins. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of antenna pins over the operating frequency range, to maximize the amount of power transferred to the antenna.

Item	Requirements	Remarks
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits.
Maximum Gain		The maximum antenna gain must not exceed the value specified in type approval documentation to comply with regulatory agencies radiation exposure limits.

Table 17: Summary of antenna interface requirements

Item	Requirements	Remarks
Isolation (in-band)	S_{21} > 30 dB recommended	The antenna-to-antenna isolation is the S_{21} parameter between the two antennas in the band of operation. Lower isolation might be acceptable depending on use-case scenario and performance requirements.
Isolation (out-of-band)	S_{21} > 35 dB recommended S_{21} > 30 dB acceptable	Out-of-band isolation is evaluated in the band of the aggressor to ensure that the transmitting signal from the other radio is sufficiently attenuated by the receiving antenna to avoid saturation and intermodulation effect at the receiver's port.
Envelope Correlation Coefficient (ECC)	ECC < 0.1 recommended ECC < 0.5 acceptable	The ECC parameter correlates the far field parameters between antennas in the same system. A low ECC parameter is fundamental to improve performance in MIMO-based systems.

Table 18: Summary of MIMO and Wi-Fi/Bluetooth coexistence requirements

⚠ A good isolation is critical to achieve optimal performance in Wi-Fi/Bluetooth coexistence mode while operating in the same 2.4 GHz band and in MIMO configuration for both the 2.4 GHz and 5 GHz band.

In both the cases, while selecting external or internal antennas, observe the following recommendations:

- Select antennas that provide an optimal return loss (or VSWR) figure over all the operating frequencies.
- Select antennas that provide an optimal efficiency figure over all the operating frequencies.
- Select antennas that provide an appropriate gain not to exceed the regulatory limits specified in some countries such as by FCC in the United States. See also Regulatory compliance.
- Select antennas that can provide low Envelope Correlation Coefficient in the same band.

2.2.2.1 RF Connector Design

If an external antenna is required, the designer should consider using a proper RF connector. It is the responsibility of the designer to verify the compatibility between plugs and receptacles used in the design.

Table 19 suggests some RF connector plugs that can be used by the designers to connect RF coaxial cables based on the declaration of the respective manufacturers. The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitable mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	

Table 19: U.FL compatible plug connector

Typically, the RF plug is available as a cable assembly. Different types of cable assembly are available; the user should select the cable assembly best suited to the application. The key characteristics are:

- RF plug type: select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Typically, 0.8 mm to 1.37 mm. Select thicker cables to minimize insertion loss
- Cable length: Standard length is typically 100 mm or 200 mm; custom lengths may be available on request. Select shorter cables to minimize insertion loss.
- RF connector on the other side of the cable: for example another U.FL (for board-to-board connection) or SMA (for panel mounting)

Consider that SMT connectors are typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect U.FL connector to a more robust connector such as SMA fixed on panel.

☞ A de-facto standard for SMA connectors implies the usage of reverse polarity connectors (RP-SMA) on end user accessible Wi-Fi and Bluetooth interfaces to increase the difficulty to replace the antenna with higher gain versions and exceed regulatory limits.

The following recommendations apply for proper layout of the connector:

- Strictly follow the connector manufacturer's recommended layout. Some examples are provided below:
  - SMA Pin-Through-Hole connectors require GND keep-out (that is, clearance, a void area) on all the layers around the central pin up to annular pins of the four GND posts.
  - U.FL surface mounted connectors require no conductive traces (that is, clearance, a void area) in the area below the connector between the GND land pins.
- In case of connector's RF pin size wider than the microstrip, remove the GND layer beneath the RF connector to minimize the stray capacitance thus keeping the RF line 50 Ω. For example, the active pin of UF.L connector must have a GND keep-out (also called "void area") at least on the first inner layer to reduce parasitic capacitance to ground.

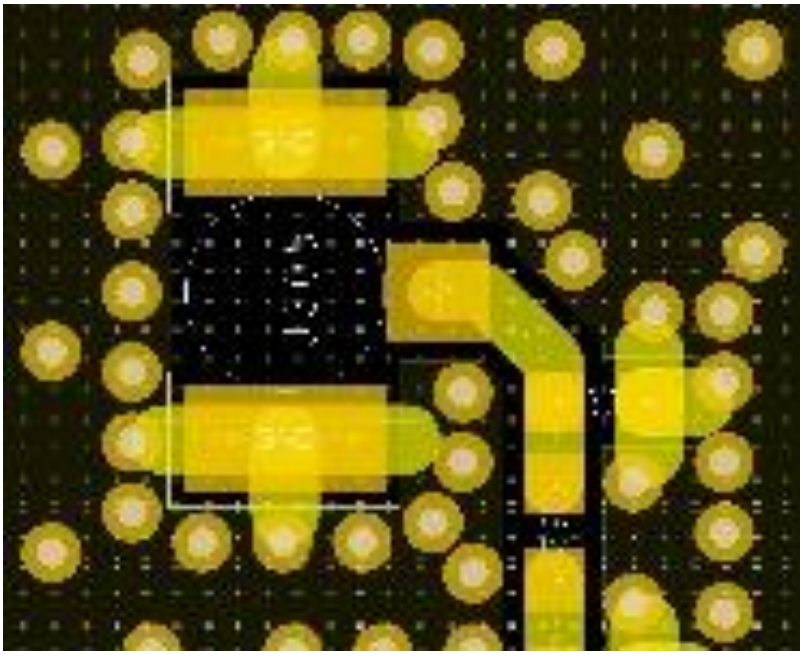

Figure 7: Example of U.FL connector layout

2.2.2.2 Integrated Antenna Design

If integrated antennas are used, the transmission line is terminated by the antennas themselves. Follow the guidelines mentioned below:

- The antenna design process should start together with the mechanical design of the product. PCB mock-ups are useful in estimating overall efficiency and radiation path of the intended design during early development stages.
- Use antennas designed by an antenna manufacturer providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the related integrated antenna requirements. The ground plane of the application PCB may be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated, however overall antenna efficiency may benefit from larger ground planes. Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts such as metal objects or ferrite sheets as they may absorb part of the radiated power, shift the resonant frequency of the antenna or affect the antenna radiation pattern.
- It is highly recommended to strictly follow the specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning/matching to reach the target performance. It is recommended to plan measurement and validation activities with the antenna manufacturer before releasing the end-product to manufacturing.
- The receiver section may be affected by noise sources like hi-speed digital busses. Avoid placing the antenna close to busses as DDR or consider taking specific countermeasures like metal shields or ferrite sheets to reduce the interference.
- Take care of interaction between co-located RF systems like LTE sidebands on 2.4 GHz band. Transmitted power may interact or disturb the performance of JODY-W1 modules where specific LTE filter is not included.

2.3 Supply interfaces

2.3.1 Module supply design

Though the GND pins are internally connected, it is recommended to connect all the available ground pins to solid ground on the application board as a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance. JODY-W1 modules must be sourced through **VBAT** and **VIO/VIO_SD** pins with proper DC power supplies that comply with the requirements summarized in Table 4.

Good connection of the JODY-W1 series module power supply pins with DC supply source is required for accurate RF performance and schematic guidelines are summarized below:

- All power supply pins must be connected to an appropriate DC source.
- Any series component with Equivalent Series Resistance (ESR) greater than a few mΩ should be avoided. Only exceptions to this rule are ferrite beads used for DC filtering, however those parts should be used carefully to avoid instability of the DC/DC supply powering the module and are in general not required.
- A minimum bulk capacitance of 10 µF on VBAT rail is required close to the module to help filter current spikes from the RF section. The preferred choice is a ceramic capacitor with X7R or X5R dielectric due to low ESR/ESL. Special care should be taken in the selection of X5R/X7R dielectrics due to capacitance derating vs DC bias voltage.

- Additional bypass capacitors in the range of 100 nF to 1 µF on all supply pins are required for high frequency filtering. The preferred choice is a ceramic capacitor with X7R or X5R dielectric due to low ESR/ESL. Smaller size bypass capacitors should be chosen for the manufacturing process to minimize ESL.

2.3.1.1 Guidelines for VCC supply circuit design using a switching regulator

It is recommended to use a Switching Mode Power Supply (SMPS) when the difference from the available supply rail to the **VBAT** rail allows significant power savings. For example, conversion of a 12 V or greater voltage supply to the nominal 3.3 V value for the **VBAT** supply.

The characteristics of the SMPS connected to the **VBAT** pin should meet the following prerequisites to comply with the module requirements summarized in Table 4.

- **Power capability:** The switching regulator together with any additional filter in front of the module must be capable of providing a voltage value within the specified operating range. The regulator must also be capable of delivering the specified peak current.
- **Low output ripple**: The switching regulator must be capable of providing a peak-to-peak Voltage ripple within the specified limits. This requirement applies both to voltage ripple generated by SMPS operating frequency and to high frequency noise generated by power switching.
- **PWM/PFM mode operation**: It is preferable to select regulators with fixed Pulse Width Modulation (PWM) mode. Pulse Frequency Modulation (PFM) mode typically exhibits higher ripple and may affect RF performance. If power consumption is not a concern, PFM/PWM mode transitions should be avoided in favor of fixed PWM operation to reduce the peak-to-peak noise on voltage rails. Switching regulators with mixed PWM/PFM mode can be used provided that the PFM/PWM modes and transition between modes complies with the requirements.

2.3.1.2 Guidelines for supply circuit design using a Low Drop-Out (LDO) linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VBAT** or **VIO/VIO_SD** value is relatively low. The linear regulators provide acceptable efficiency when transforming a supply of less than 5 V to a voltage value within the normal operating range of the module. A linear regulator can be also considered to power the **VIO/VIO_SD** section due to the low current requirements, especially if cascaded from a SMPS-generated low voltage rail.

The characteristics of the Low Drop-Out (LDO) linear regulator used to power the voltage rails must meet the following prerequisites to comply with the requirements summarized in Table 4.

- **Power capabilities**: The LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VBAT** or **VIO/VIO_SD** pins within the specified operating range and must be capable of withstanding and delivering the maximum specified peak current while in Connected mode.
- **Power dissipation**: The power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range. The worst-case junction temperature can be estimated as shown below:

  $$T_{j,est} = (V_{in} - V_{out}) * I_{avg} * \theta_{ja} + T_a$$

  Where: θ_{ja} is the junction-to-ambient thermal resistance of the LDO's package[7], I_{avg} is the current consumption of the given voltage rail in continuous TX/RX mode and T_a is the maximum operating temperature of the end product inside the housing.

[7] Thermal dissipation capability reported on datasheets is usually tested on a reference board with adequate copper area (ref. to JESD51 [9]). Junction temperature on a typical PCB may be higher than the estimated value due to the limited space to dissipate the heat. Thermal reliefs on pads also affect the capability of a device to dissipate the heat.

2.4 Data communication interfaces

2.4.1 PCI express

The PCI express bus of JODY-W1 series modules support PCIe v3.0 connectivity at transfer rates up to 2.5 Gbaud. PCIe differential clock and data pairs accommodate a controlled impedance bus. The parameters needed for the track impedance calculation are shown in Figure 8.

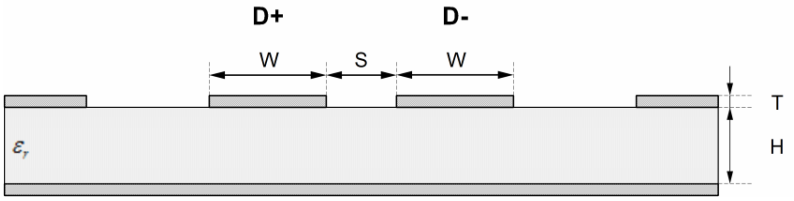

Figure 8: Differential pair, generic-controlled, impedance parameters

To ensure the bus signal integrity and avoid EMI issues, PCIe data lines must follow the recommendations stated in Table 20.

Signal group	Parameter	Min.	Typ.	Max.	Unit
PCIe differential data	Single Ended impedance, Z_{SE}	60			Ω
	Differential impedance, Z_{diff}		100		Ω
	Common mode impedance, Z_{CM}		50		Ω
	Impedance control, Z_{SE}, Z_{diff}, Z_{CM}	$Z_0 - 20\%$	Z_0	$Z_0 + 20\%$	
	PCB signal attenuation margin			13,2	dB
	Bus skew length mismatch on same differential pair			0,1	mm
	Bus skew length mismatch between differential pairs	Not required			-
	Isolation to other pairs and PCB signals	5*W			

Table 20: PCI express bus requirements

2.4.2 SDIO 3.0

The SDIO 3.0 bus can support a clock frequency up to 208 MHz and thus requires special care to ensure that the signal integrity requirements are met and EMI issues are minimized. The signals should be routed with a single ended impedance of 50 Ω.

It is recommended that all signals in the bus are routed with the same length. The total bus length should be minimal, and signals should have appropriate grounding in the surrounding layers.

The layout of the SDIO bus should be completed so that crosstalk with other parts of the circuit is kept to a minimum. This ensures that the isolation between the signals, clock, and surrounding busses/traces is adequate.

Figure 9 shows the suggested application schematic for the SDIO bus in JODY-W1 modules, while Table 21 summarizes the electrical requirements of the bus.

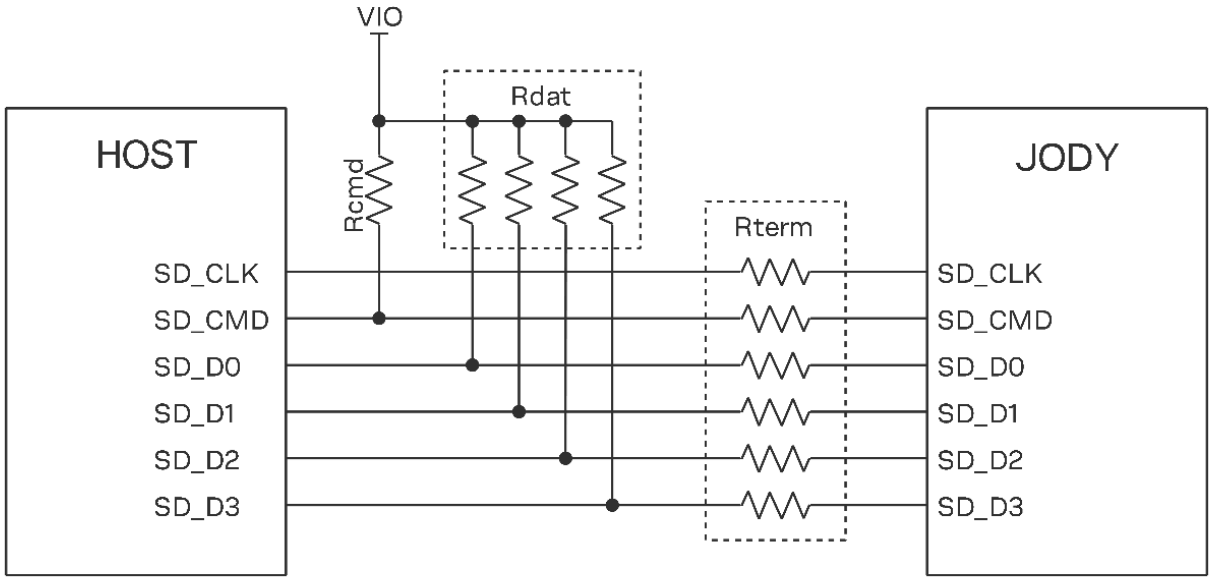

Figure 9: SDIO application schematic

☞ Pull-up resistors can be provided either externally on the host PCB or internally in the host application processor. Depending on the routing of the SDIO lines on the host, termination resistors in series to the lines might also be needed.

Signal Group	Parameter	Min.	Typ.	Max.	Unit
CLK, CMD, DAT[0:3]	Single ended impedance, Z_0		50		Ω
CLK, CMD, DAT[0:3]	Impedance control	$Z_0 - 10\%$	Z_0	$Z_0 + 10\%$	Ω
DAT[0:3]	Pull-Up range, Rdat	10	47	100	kΩ
CMD	Pull-Up range, Rcmd	10	10	50	kΩ
CLK, CMD, DAT[0:3]	Series termination (Host side), Rterm[8]	0	0		Ω
CLK, CMD, DAT[0:3]	Bus length[9]			100	mm
CMD, DAT[0:3]	Bus skew length mismatch to CLK	-3		+3	mm
CLK	Center to center CLK to other SDIO signals[10]	4*W			
CMD, DAT[0:3]	Center to center between signals[9]	3*W			

Table 21: SDIO bus requirements

[8] Series termination values larger than typical recommended only for addressing EMI issues.
[9] Routing should minimize the total bus length.
[10] Center to center spacing requirement can be ignored for up to 10 mm of routed length to accommodate BGA escape.

2.4.3 High-speed UART interface

The high-speed UART interface for the JODY-W1 complies with the HCI UART Transport layer and uses the settings described in Table 22.

UART Settings	
baud rate default	115200 Baud
Data bits	8
Parity bit	No parity
Stop bit	1 stop bit
Flow Control	RTS/CTS

Table 22: HCI UART Transport layer settings

2.4.4 Other interfaces and notes

All pins have internal keeper resistors; leave it open if not used. All digital pins have internal keeper resistors and can be left open if they are not used.

2.5 General high speed layout guidelines

These general design guidelines are considered as best practices and are valid for any bus present in the JODY-W1 modules; the designer should prioritize the layout of higher speed busses. Low frequency signals are generally not critical for layout.

⚠ One exception is represented by High Impedance traces (such as signals driven by weak pull resistors) that may be affected by crosstalk. For those traces, a supplementary isolation of four times the trace width from other busses is recommended.

2.5.1 General considerations for schematic design and PCB floor planning

- Verify which signal bus requires termination and add series resistor terminations to the schematics.
- Carefully consider the placement of the module with respect to antenna position and host processor; RF trace length should be minimized first, followed by PCIe/SDIO bus length.
- PCIe/SDIO bus routing should be planned to minimize layer-to-layer transition to a minimum.
- Verify with PCB manufacturer allowable stack-ups and controlled impedance dimensioning for antenna traces and busses.
- Verify that the power supply design and power sequence are compliant with JODY-W1 specification. See also Supply interfaces.

2.5.2 Component placement

- Accessory parts like bypass capacitors should be placed as close as possible to the module to improve filtering capability, prioritizing the placement of the smallest size capacitor close to module pins.
- Particular care should be taken not to place components close to the antenna area. The designer should carefully follow the recommendations from the antenna manufacturer about the distance of the antenna vs. other parts of the system. The designer should also maximize the distance of the antenna to Hi-frequency busses like DDRs and related components or consider an optional metal shield to reduce interferences that could be picked up by the antenna thus reducing the module's sensitivity.

2.5.3 Layout and manufacturing

- Avoid stubs on high-speed signals. Test points or component pads should be placed over the PCB trace.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length; longer traces will degrade signal performance. Ensure that maximum allowable length for high-speed busses is not exceeded.
- Ensure to track your impedance matched traces. Consult early with your PCB manufacturer for proper stack-up definition.
- RF, analog and digital sections should have dedicated and clearly separated areas on the board.
- No digital routing is allowed in the GND reference plane area of RF traces (ANT pin and Antenna).
- It is strongly recommended to avoid digital routing beneath all layers of RF traces.
- Ground cuts or separation is not allowed below the module and sensitive lines (high speed signals, RF, CLK).
- Minimize the length of the RF traces as first priority. Then, minimize bus length to reduce potential EMI issues from digital busses.
- All traces (Including low speed or DC traces) must couple with a reference plane (GND or power), Hi-speed busses should be referenced to the ground plane. In this case, if the designer needs to change the ground reference, an adequate number of GND vias must be added in the area of transition to provide a low impedance path between the two GND layers for the return current.
- Hi-Speed busses are not allowed to change reference plane. If a reference plane change is unavoidable, some capacitors should be added in the area to provide a low impedance return path through the different reference planes.
- Trace routing should keep a distance greater than 3w from the ground plane routing edge.
- Power planes should keep a distance from the PCB edge sufficient to route a ground ring around the PCB, the ground ring must then be connected to other layers through vias.

⚠ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application baseboard below the JODY-W1 series modules. Avoid placing temperature sensitive devices close to the module and provide adequate grounding to transfer the generated heat to the PCB.

2.5.4 Layout considerations to reduce spurious emissions

Careful considerations must be taken while designing the product integration to minimize the spurious emission. It is recommended that the integrator checks the performance in early design-in to comply with RED (EN 301 893, EN 300 440). The RED directive is applicable on the end product and any further system shield apart from the module's shield will improve end product emission.

It is recommended to implement the following guidelines:

- Route GPIOs and power lines in a strip-line layer with a GND layer above.
- Place decoupling capacitors, as best practice, as close as possible to the module.
- Implement thin dielectrics thickness to the surrounding layers. This shall be as thin as possible, preferably less than 100 µm (4 mils).
- Route power interconnects as wide as possible.
- Place vias with narrow distribution along the path of the GPIO interconnects.
- Avoid large dielectric cavities in the PCB.
- Stitch the outside edge of the system board with GND vias.

☞ Especially note the first harmonic of the local oscillator (LO) frequency (11–12 GHz range).

2.6 Module footprint and stencil design

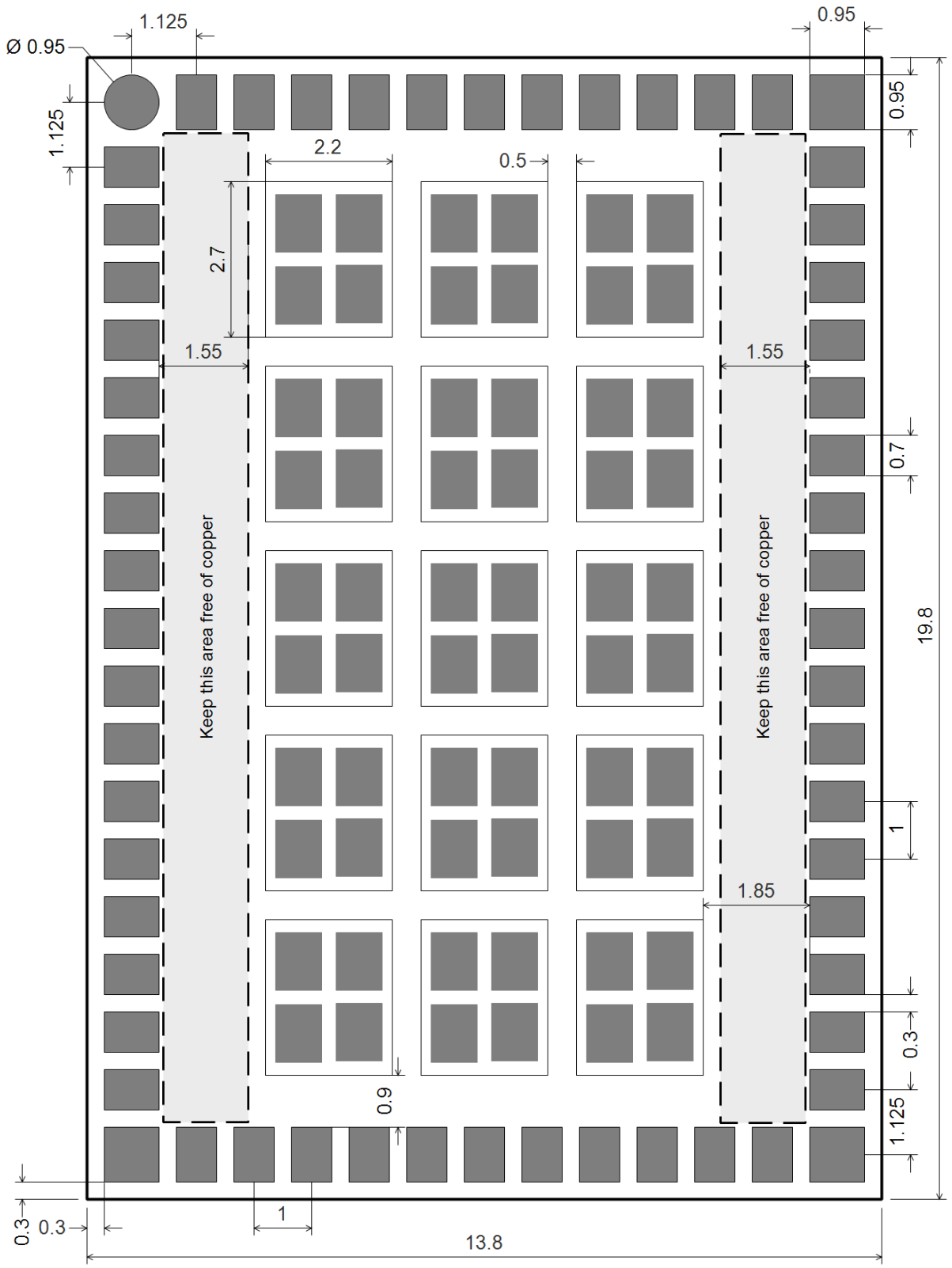

Figure 10: Recommended footprint and stencil opening (grey) for JODY-W1 module (dimensions in mm)

⚠ Future variants of JODY-W1 can have more pins in the area enclosed with dotted lines. To ensure compatibility, keep this area free of copper.

Figure 10 describes the pad layout for the JODY-W1 series module. The proposed land pattern layout reflects the pin layout of the module. Both Solder Mask Defined (SMD) and Non Solder Mask Defined (NSMD) pads can be used with the following considerations:

- Pins from 1 to 60 should be NSMD
- Inner pads must have a good thermal bonding to PCB ground planes to help spreading the heat generated by the module.
- If NSMD design is chosen for inner pads, thermal reliefs should be considered and 4 or 9 vias per pad must be added for heat sink. Those vias may require copper capping.
- If SMD design is chosen for inner pads, the land pattern can be flooded on a ground plane beneath the module and vias added around the pads for heat sinking.

The suggested stencil layout for the JODY-W1 series module follows exactly the copper outer pad layout as described in Figure 10. The central pads should be implemented with a special solder paste pattern.

Figure 11 shows a suggested stencil opening implementation with the following characteristics:

- Solder paste area should be split into several smaller parts, typically four to nine, depending on the copper pad area.
- Total solder paste area should cover about 50% to 60% of copper thermal pad area.
- Total solder paste area must not exceed 65% of copper thermal pad area.

Missing to consider solder paste optimization may lead to poor soldering quality in production.

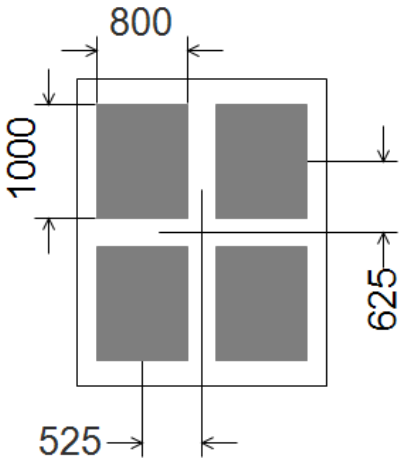

Figure 11: Stencil opening example for inner thermal pads (dimensions in µm)

⚠ The exact mask geometries, distances and stencil thicknesses must be adapted to the specific production process of the customer.

2.7 Thermal guidelines

JODY-W1 series modules have been successfully tested from -40 °C to +85 °C ambient temperature. The board generates heat during high loads that must be dissipated to sustain the lifetime of the components.

The improvement of module's thermal dissipation decreases its internal temperature, which increases the long-term reliability of the device for applications that operate at high ambient temperature.

For best performance, the layout design should embrace the following guidelines:

- Vias specification for ground filling: $300/600\mu m$, no thermal reliefs are allowed on vias.
- Ground vias density under the module: Thermal $50\ vias/cm^2$ can be placed in the gaps between module's thermal pads.
- Minimum layer count and copper thickness: $4\ layers$, $35\ \mu m$.
- Power planes and signal traces should not cross the layers beneath the module to maximize heat flow from the module.

☞ For information about the thermal parameters, see also the JODY-W1 series data sheet [2].

The following additional hardware techniques can be used to improve the thermal performance of the module in customer's applications:

- Maximize antenna's return loss to reduce reflected RF power to the module.
- Improve the efficiency and the thermal design of any component that generates heat in the application, including power supplies and processor, to spread the generated heat distribution over the application device.
- Properly design the mechanical enclosure of the application device to provide ventilation and good thermal dissipation.
- For continuous operation at high temperatures, high power density applications or reduced PCB size, the designer may consider a heat sink on main PCB's bottom side, connected through electrically insulated / high thermal conductivity adhesive[11].

2.8 ESD guidelines

In compliance with the following European regulations, designers must implement proper measures to protect the module from ESD events on any pin that may be exposed to the end user.

- ESD testing standard CENELEC EN 61000-4-2 [3]
- Radio Equipment standard ETSI EN 301 489-1 [4]

The minimum requirements of these regulations are summarized in Table 23:

Application	Category	Immunity level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration of the end product.	Contact Discharge	4 kV
	Air Discharge	8 kV

Table 23: Minimum ESD immunity requirements based on EN 61000-4-2

Compliance with standard protection levels defined in EN 61000-4-2 [3] can be satisfied by including proper ESD protection in parallel to the line – close to areas accessible by the end user.

⚠ Special care should be taken to protect the antenna pins. It is advisable to choose an ESD absorber with adequate parasitic capacitance for this purpose. For 5 GHz operation, protection that offers a maximum internal capacitance of 0.1 pF is recommended.

The maximum ESD ratings for JODY-W1 modules are described in the datasheet [2].

[11] Typically not required.

2.9 Design-in checklist

2.9.1 Schematic checklist

- ☐ JODY-W1 module pins are properly numbered and designated on the schematic (including thermal pins).
- ☐ Power supply design complies with the specification.
- ☐ The power sequence (including **WL_EN** and **BT_EN** signal handling) is properly implemented.
- ☐ Adequate bypassing is present in front of each power pin.
- ☐ Each signal group is consistent with its own power rail supply or proper signal translation has been provided.
- ☐ Configuration pins are properly set at bootstrap.
- ☐ SDIO bus includes series resistors and pull-ups.
- ☐ SDIO signal voltage matches VIO_SD and bootstrap configuration.
- ☐ Unused pins are properly terminated.
- ☐ Recommended to use of a pi-filter in front of each antenna for final matching.
- ☐ RF co-location additional filters have been considered in the design.

2.9.2 Layout checklist

- ☐ PCB stack-up and controlled impedance traces follow PCB manufacturer's recommendation.
- ☐ All pins are properly connected, and the package follows u-blox recommendations for pin design.
- ☐ Proper clearance has been provided between RF section and digital section.
- ☐ There is proper isolation between Antennas (RF co-location, diversity, or multi-antenna design).
- ☐ Bypass capacitors are placed close to the module.
- ☐ Low impedance power path has been provided to the module.
- ☐ Controlled impedance traces are properly implemented on the layout (both RF and digital) and follow PCB manufacturer recommendations.
- ☐ 50Ω RF traces and connectors follow the rules for Antenna interfaces.
- ☐ Antenna design has been reviewed by the antenna manufacturer.
- ☐ The module has proper grounding for low impedance return path and heat sink.
- ☐ Reference plane skipping has been minimized for high frequency busses.
- ☐ All traces and planes are routed inside the area defined by the main ground plane.
- ☐ u-blox has reviewed and approved the PCB[12].

[12] This is applicable only for end-products based on the u-blox reference designs.

3 Software

This chapter provides information on how to set up the JODY-W1 series module on a Linux operating system. It describes the available driver packages and shows how they can be compiled and deployed into the target system. Additionally, typical usage examples are presented.

This manual is mainly based on the proprietary automotive software release ('DHD' driver) for the Infineon CYW8x359 chipsets in JODY-W16x. An Apalis TK1 development board from Toradex, running on kernel version 3.10.40, is used as the host platform, which connects to the JODY-W1 series module through either a PCI express or SDIO host interface. A USB host interface is used to connect to the module's Bluetooth UART via a USB-to-UART adapter.

3.1 Available software packages

Software support for the JODY-W1 series modules is provided by the proprietary automotive Linux/Android software releases ('DHD') and the Linux open-source software release ('FMAC'). Refer to the release notes included with each driver release for a list of supported features.

☞ The proprietary automotive Android/Linux DHD drivers for JODY-W1 series modules are distributed by Infineon directly under the terms of a software license agreement. To get the driver package contact your local u-blox support team.

☞ The open-source Linux FMAC drivers can be obtained from the Infineon Linux community page or through u-blox support.

☞ Recipes for integrating the drivers into Yocto-based projects can be provided on request by u-blox.

For QNX support, contact QNX or a QNX development partner directly. Microsoft Windows OS is not supported.

3.1.1 Supported kernel versions

Due to constant changes in the kernel subsystem APIs for different kernel releases, the reference drivers provided must be modified for each major and minor kernel release.

The DHD driver packages have been verified on the following platforms and kernel versions:

Platform	SoC	Kernel Version
i.MX 6SoloX Sabre board (smart devices)	NXP i.MX 6SoloX	3.14.52 4.1.15
i.MX 6Q Sabre development board	NXP i.MX 6 series	4.1.15
Toradex IXORA Apalis TK1	NVIDIA Tegra K1	3.10.40
Core i5 Brix Lubuntu 15	Intel i686	4.2.0
i.MX MCIMX8M-EVK	NXP i.MX8M	Android 8.1.0, kernel 4.9.78 [14]

Table 24: Tested platforms and Linux kernel versions for JODY-W1 series modules reference drivers

The provided software packages might support the latest kernel versions if there is no change in the used kernel API. If there are any changes to the used kernel APIs, then make necessary changes using patches of the provided software packages.

☞ The current automotive Infineon software release supports Linux kernel versions up to 5.4 and Android 7.0/8.0. For additional information, contact your local support team.

3.2 Software package content

Separate DHD software releases are available for different chipsets used in JODY-W1 series and PCIe or SDIO Wi-Fi host interfaces. Normally, a software package from Infineon contains the following items:

- PCIe/SDIO driver sources (DHD)
- Backports package including PCIe/SDIO driver sources (FMAC)
- CYW8x359/CYW8x459 PCIe/SDIO firmware images
- hostapd and wpa_supplicant sources or patches, including chipset specific enhancements
- Pre-compiled drivers and tools (see the attached release notes for details)
- A document with details on driver compilation, system bring-up and use case examples is provided together with the software release package.
- Android reference Hardware Abstraction Layer (HAL)

⚠ The included nvram.txt file is for example purposes only. Use the specific NVRAM file for the JODY-W1 series module variant, which is provided separately by u-blox.

☞ The NVRAM file includes the basic configuration settings and calibration data for JODY-W1 series modules. Some NVRAM settings are already stored in the OTP memory of the module.

The software package includes a reference Country Locale Map (CLM) file that defines the regulatory behavior for supported countries. These definitions provide the valid channels and maximum transmit power settings of each rate and channel. The product specific regulatory requirements can be fulfilled by changing the regulatory definitions in the CLM file. See also Regulatory configuration.

3.2.1 Wi-Fi firmware images

The software packages contain different firmware images that are chosen to support the use case. These are downloaded to the module after each power cycle.

Table 25 lists the available firmware images for JODY-W1 series modules in the DHD and FMAC software packages.

Firmware image	Module variant	Description
fw_bcmdhd.bin	JODY-W16x	DHD PCIe/SDIO firmware without RSDB support (generally for Rear Seat Entertainment). Supports MIMO and DFS master[13] operation.
fw_bcmdhd_RSDB.bin	JODY-W16x	DHD PCIe/SDIO f irmware with RSDB support (generally for Head Unit). Supports MIMO in non-RSDB mode. No DFS master support.
fw_bcmdhd_mfg.bin	JODY-W16x	DHD PCIe/SDIO MFG firmware for testing and certification.
brcmfmac4359-pcie.bin	JODY-W16x	FMAC PCIe firmware
brcmfmac4359-sdio.bin	JODY-W16x	FMAC SDIO firmware
brcmfmac89459-pcie.bin	JODY-W17x	FMAC PCIe firmware
firmware_pcie.bin	JODY-W17x	DHD PCIe firmware
firmware_pcie_mfgtest.bin	JODY-W17x	DHD PCIe MFG firmware for testing and certification.

Table 25: Description of Wi-Fi firmware images

☞ JODY-W16x series modules must use PCIe Wi-Fi firmware version 9.40.117.24 (based on 'Clutch' release) or SDIO Wi-Fi firmware version 9.40.112.17 (based on “Brakepad” release), or a later firmware version.

[13] JODY-W1 has not been certified to operate as DFS master.

3.2.2 Additional u-blox software deliverables

The following deliverables are provided separately by u-blox for JODY-W1 series modules:

- A module variant and host interface specific NVRAM file
- A “patchram” firmware file, required for Bluetooth operation
- Yocto/OpenEmbedded recipes that serve as an integration example of the driver package

☞ The Yocto/OpenEmbedded recipes provided by u-blox for JODY-W1 series modules already contain the NVRAM and patchram files for the JODY-W1 series module variants.

☞ Contact your local u-blox support team to get specific deliverables for JODY-W1 series modules.

3.3 Software architecture overview

From the software perspective, JODY-W1 series modules contain only calibration data, basic operation settings, and MAC addresses in an on-board OTP memory. This means that the modules need a host-side driver and a device firmware to operate.

At startup, and at every reset or power cycle, the Wi-Fi driver must download the firmware file to enable Wi-Fi operation of the module. The Wi-Fi driver interfaces with the bus drivers and upper layer protocol stacks of the Linux system. The `patchram` file is required for Bluetooth operation of the module.

Figure 12 shows the software components required for the operation of JODY-W1 series modules.

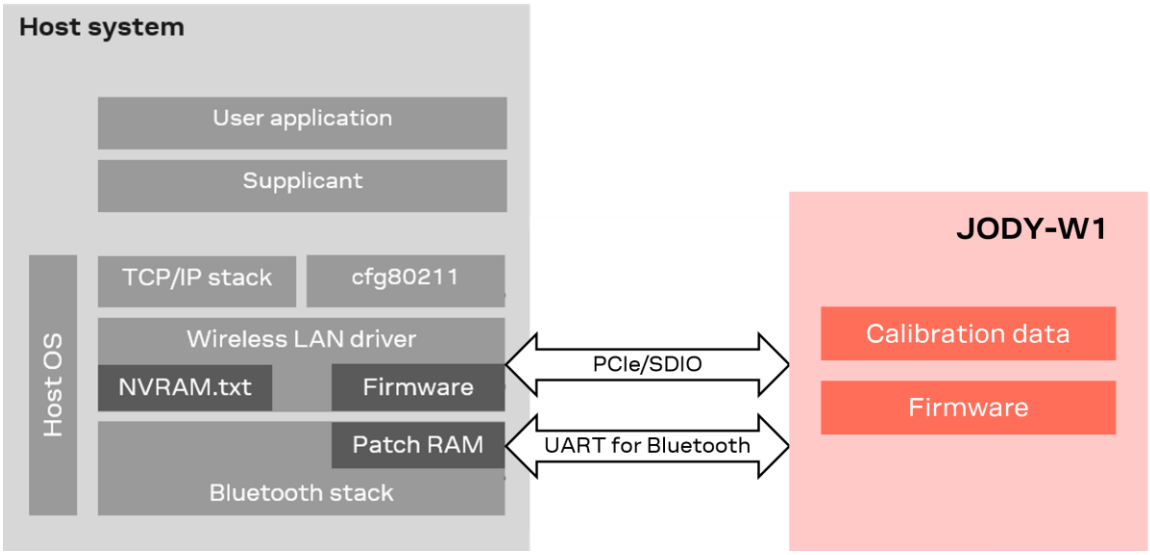

Figure 12: Basic software overview

3.3.1 Wi-Fi driver

The Wireless LAN driver for the JODY-W1 series module is a so-called FullMAC driver, as the 802.11 MAC management tasks are handled by the device firmware. Configuration management of the Wi-Fi device is handled by the cfg80211 subsystem of the Linux kernel and user-space configuration is managed through the nl80211 protocol.

3.3.2 Bluetooth host stack

The Bluetooth host stack is not part of the distributed driver package. JODY-W1 series modules are qualified as “Controller Sybsystem” and provide a dedicated UART interface for the Bluetooth Host Controller Interface (HCI) transport layer. The Bluetooth stack on the host attaches directly to the HCI UART transport layer.

The official implementation of the Bluetooth protocol stack in Linux is BlueZ. JODY-W1 series modules can work with any other Bluetooth protocol stack implementation, for example, *Blue SDK* from OpenSynergy.

3.4 Compiling the software

The software release package from Infineon includes documentation that describes the driver compilation procedures, system bring-up, and use case examples.

☞ The Yocto/OpenEmbedded recipes provided by u-blox can be used to integrate the software package into Yocto/OpenEmbedded projects. These recipes also serve as a useful reference for compiling and deploying the software package.

3.4.1 Prerequisites

The Wi-Fi driver for the JODY-W1 series modules is depending on the PCI or MMC/SDIO stack of the Linux kernel; thus this must be enabled in the target system's kernel configuration.

For configuration management, the driver supports the cfg80211 wireless configuration API, which needs to be selected via the `CONFIG_CFG80211` option.

In order to use Bluetooth with the Linux BlueZ stack, the kernel options `CONFIG_BT_HCIUART` and `CONFIG_BT_HCIUART_H4` and support for the various Bluetooth protocols must be enabled.

Prior to building the driver, the kernel needs to be prepared for the compilation of external kernel modules. For this, change to the kernel's source directory and run the following:

```
$ make modules_prepare
```

⚠ "`make modules_prepare`" will not build Module.symvers even if CONFIG_MODVERSIONS is set; therefore, a full kernel build must be executed to make module versioning work.

The included *wpa_supplicant* depends on the *libnl-3* and *openssl* packages. The libraries and header files need to be available at compile-time and the libraries need to be installed on the target system.

3.5 Deploying the software

The following steps briefly describe how to install the driver and firmware files on the target system:

1. The `bcmdhd.ko` kernel module should be copied to somewhere below the modules directory of the kernel, for example, `/lib/modules/<kernel-version>/updates/`. Run the `depmod` command afterwards to update the module dependencies and to have the modules findable by the *modprobe* utility.
2. Copy the respective firmware file, for example, `fw_bcmdhd.bin/fw_bcmdhd_RSDB.bin`, from the packages's `firmwares` directory and the separately provided NVRAM file for JODY-W1 series modules to the directory `/lib/firmware/brcm/` on the target file system. Copy the CLM and patchram files to the same directory.
3. Copy the supplicant binaries wpa_supplicant and wpa_cli to an appropriate location on the target file system and add it to the `$PATH` environment variable, if required.

An example deployment is shown below:

```
/
└── lib
    ├── firmware
    │   └── brcm
    │       ├── fw_bcmdhd_RSDB.bin
    │       ├── <module variant specific nvram file>
    │       ├── <customer specific clm_blob file>
    │       └── <patchram.hcd>
    ├── modules
    │   └── <kernel-version>
    │       └── updates
    │           └── bcmdhd.ko
    └── opt
        └── jody-w1
            ├── wpa_supplicant
            └── wpa_cli
```

Listing 1: Example target file system

3.5.1 Additional software requirements

Some additional packages that are recommended for installation on the target system are mentioned in Table 26.

Package	Comment
bluez4 or bluez5	Contains the user space parts of the Linux Bluetooth stack
wpa_supplicant	WPA supplicant. Handles key negotiation and roaming etc. on client side. Included in Infineon software package.
iw	CLI configuration utility for wireless devices
hostapd	User space daemon for access point and authentication servers. Included in Infineon software package.
crda	User space udev helper to handle regulatory domain

Table 26: Recommended additional software packages

3.6 Loading the Wi-Fi driver

If the Wi-Fi driver was installed correctly, you can load it by simply issuing the following command, which will load the *bcmdhd* kernel module and all its dependencies, such as *cfg80211*:

```
$ modprobe bcmdhd firmware_path=/lib/firmware/brcm/fw_bcmdhd_RSDB.bin
  nvram_path=/lib/firmware/brcm/<nvram.txt> clm_path=/lib/firmware/brcm/<clm_blob>
```

☞ The *nvram.txt* file contains basic configuration settings and calibration data for JODY-W1 series modules.

If the kernel module is automatically loaded by the kernel or a user-space helper, the options can be provided in a *modprobe* configuration file, for example:

```
options bcmdhd firmware_path=/lib/firmware/brcm/fw_bcmdhd_RSDB.bin
options bcmdhd nvram_path=/lib/firmware/brcm/<nvram.txt>
options bcmdhd clm_path=/lib/firmware/brcm/<clm_blob>
```

Listing 2: /etc/modprobe.d/bcmdhd.conf

If the driver was successfully loaded, you should see it in the list of loaded modules, as shown in the example below:

```
Module                  Size  Used by
bcmdhd                779445  0
```

Listing 3: lsmod output

The lspci command can be used to list the detected PCI devices in the system, for example:

```
$ lspci
01:00.0 Network controller: Broadcom Corporation Device 4355 (rev 05)
[…]
```

The following listing shows an example message from the kernel log, when the JODY-W1 series module is detected in SDIO mode:

```
mmc2: new ultra high speed SDR104 SDIO card at address 0001
```

When the module is detected on the PCI express or SDIO interface, the driver will automatically download the firmware to it, initialize the hardware, and register the network interfaces.

☞ The **WL_EN** pin of the module must be asserted to enable the Wi-Fi function.

```
$ dmesg
[…]
PCI_PROBE:  bus 1, slot 0,vendor 14E4, device 4355(good PCI location)
dhd_bus_download_firmware: firmware path=/lib/firmware/brcm/fw_bcmdhd_hu.bin, nvram
  path=/lib/firmware/brcm/nvram.txt
[…]
Firmware up: op_mode=0x0c05, MAC=00:90:4c:12:d0:01
Firmware version = wl0: Aug 10 2017 04:13:58 version 9.40.56 (@VC_VERSION_NUM CY) FWID 01-
  9469e017
Dongle Host Driver, version 1.363.30 (r)
Register interface [wlan0]  MAC: 00:90:4c:12:d0:01
```

Listing 4: Example of kernel log after loading the PCIe driver

Now you should be able to see a new *wlan0* network interface (for example using the '`ifconfig -a`' or '`iw dev`' commands).

To unload the driver, bring all the interfaces down first and then remove the module using:

```
$ rmmod bcmdhd
```

3.7 Bluetooth initialization

Do the following steps (as mentioned in the sequence below) to initialize the Bluetooth functionality on the JODY-W1 module:

1. Bluetooth enable pin: To enable the Bluetooth function on the JODY-W1 module, the Bluetooth power enable pin (**BT_EN**) must be asserted high. The pin can be statically asserted by the hardware or from the host during the boot sequence of the system; for example, during the kernel board initialization or in a Linux init script via the GPIO sysfs interface.
2. Firmware loading: After enabling the Bluetooth function of the module, the patchram firmware file must be downloaded to the module. This is done via the *brcm_patchram_plus* utility, which can be downloaded from [10] or obtained from u-blox support as part of the Yocto/OpenEmbedded recipes.

☞ The /dev/ttyUSB0 device is an example value that must be modified depending on the board that is being used.

```
$ brcm_patchram_plus --no2bytes --tosleep 50000 --baudrate 3000000 --
  use_baudrate_for_download --patchram /lib/firmware/brcm/<patchram.hcd> /dev/ttyUSB0
```

3. Load HCI UART kernel module. If HCI UART support in the kernel is compiled as a module, this needs to be loaded.

```
$ modprobe hci_uart
```

4. HCI attach: The serial interface, where the JODY-W1 module's Bluetooth UART is connected to, must be bound via UART HCI to the BlueZ stack. This is done using the *hciattach* tool, which is part of the BlueZ stack. The following example command shows how to attach to the JODY-W1 through the /dev/ttyUSB0 serial device.

```
$ hciattach /dev/ttyUSB0 any 3000000 flow
Device setup complete
```

5. Configure the HCI interface: Before using the module from user space, the Bluetooth HCI interface must be set up using the *hciconfig* command. The interface index depends on the number of Bluetooth devices in the system.

```
$ hciconfig hci0 up
```

6. Run the Bluetooth daemon: Finally, the Bluetooth daemon should be started to enable Bluetooth services.

```
$ bluetoothd
```

3.8 Usage examples

This section provides some typical usage examples for JODY-W1 series modules. The examples use *wpa_*supplicant for managing the module in Access Point (AP) and Station (STA) mode. The configuration files for *wpa_supplicant* are shown below. The configuration files and *wpa_supplicant* binaries are assumed to be installed in the `/opt/jody-w1` directory.

```
update_config=1
ctrl_interface=/var/run/wpa_supplicant
eapol_version=1
ap_scan=1
fast_reauth=1
driver_param=use_p2p_group_interface=1p2p_device=1
device_name=JODY1
device_type=10-0050F204-5
config_methods=virtual_push_button physical_display keyboard
interworking=1
```

Listing 5: wpa_supplicant.conf

```
ctrl_interface=/var/run/wpa_supplicant
update_config=1
p2p_disabled=1
```

Listing 6: wpa_supplicant_ap.conf

Once the driver has been loaded, start *wpa_supplicant* using the following command:

```
$ ./wpa_supplicant -i wlan0 -D nl80211 -c wpa_supplicant.conf -g /var/run/wpa_wlan0_cmd -B
```

Start *wpa_cli* to issue commands to the supplicant:

```
$ ./wpa_cli -i wpa_wlan0_cmd -p /var/run
```

3.8.1 5G SoftAP + 2G SoftAP

This example shows how to start two concurrent Aps in the 2.4 GHz and 5 GHz bands in RSDB mode.

☞ When creating an AP+AP configuration, the 5 GHz AP should be started first, since Bluetooth is connected to core0 of the JODY-W1 series module. If the 2.4 GHz AP is started first, it will come up on core0 instead and might cause interferences with 2.4 GHz Bluetooth.

First, create the 5 GHz AP:

```
wpa_cli> IFNAME=wlan0 DRIVER interface_create bcm0
wpa_cli> interface_add bcm0 /opt/jody-w1/wpa_supplicant_ap.conf nl80211
wpa_cli> IFNAME=bcm0 remove_net all
wpa_cli> IFNAME=bcm0 add_net
wpa_cli> IFNAME=bcm0 set_net 0 ssid "JODY-5G"
wpa_cli> IFNAME=bcm0 set_network 0 proto WPA2
wpa_cli> IFNAME=bcm0 set_network 0 key_mgmt WPA-PSK
wpa_cli> IFNAME=bcm0 set_network 0 pairwise CCMP
wpa_cli> IFNAME=bcm0 set_network 0 psk "12345678"
wpa_cli> IFNAME=bcm0 set_net 0 frequency 5180
wpa_cli> IFNAME=bcm0 set_net 0 mode 2
wpa_cli> IFNAME=bcm0 select_net 0
```

Listing 7: 5 GHz SoftAP on channel 36 with WPA2-PSK-AES security

Assign an IP address to the AP network interface and run a DHCP server:

```
$ cat udhcpd-bcm0.conf
start 192.168.9.8
end 192.168.9.255
interface bcm0
pidfile /var/run/udhcpd-bcm0.pid
lease_file /var/lib/misc/udhcpd-bcm0.leases
option subnet 255.255.255.0
option lease 864000 # default: 10 days

$ ifconfig bcm0 192.168.9.1
$ udhcpd -S udhcpd-bcm0.conf
```

Listing 8: 5 GHz AP IP configuration

Next, create a network interface for the 2.4 GHz AP and configure it:

```
wpa_cli> IFNAME=wlan0 DRIVER interface_create bcm1
wpa_cli> interface_add bcm1 /opt/jody-w1/wpa_supplicant_ap.conf nl80211
wpa_cli> IFNAME=bcm1 remove_net all
wpa_cli> IFNAME=bcm1 add_net
wpa_cli> IFNAME=bcm1 set_net 0 ssid "JODY-2G"
wpa_cli> IFNAME=bcm1 set_net 0 key_mgmt NONE
wpa_cli> IFNAME=bcm1 set_net 0 frequency 2437
wpa_cli> IFNAME=bcm1 set_net 0 mode 2
wpa_cli> IFNAME=bcm1 select_net 0
```

Listing 9: 2.4 GHz SoftAP on channel 6 without security

Assign an IP address to the AP network interface and run a DHCP server:

```
$ cat udhcpd-bcm1.conf
start 192.168.10.8
end 192.168.10.255
interface bcm1
pidfile /var/run/udhcpd-bcm1.pid
lease_file /var/lib/misc/udhcpd-bcm1.leases
option subnet 255.255.255.0
option lease 864000 # default: 10 days

$ ifconfig bcm1 192.168.10.1
$ udhcpd -S udhcpd-bcm1.conf
```

Listing 10: 2.4 GHz AP IP configuration

3.8.2 2G SoftAP + 2G Station

This example shows how to start concurrent AP and STA in the 2.4 GHz band.

☞ When creating an AP+STA configuration in the same band, both will be on the same channel. The AP follows the channel of the STA.

First, create the 2.4 GHz AP:

```
wpa_cli> IFNAME=wlan0 DRIVER interface_create bcm0
wpa_cli> interface_add bcm0 /opt/jody-w1/wpa_supplicant_ap.conf nl80211
wpa_cli> IFNAME=bcm0 remove_net all
wpa_cli> IFNAME=bcm0 add_net
wpa_cli> IFNAME=bcm0 set_net 0 ssid "JODY-2G"
wpa_cli> IFNAME=bcm0 set_network 0 key_mgmt NONE
wpa_cli> IFNAME=bcm0 set_net 0 frequency 2437
wpa_cli> IFNAME=bcm0 set_net 0 mode 2
wpa_cli> IFNAME=bcm0 select_net 0
```

Listing 11: 2.4 GHz SoftAP on channel 6 without security

Assign an IP address to the AP network interface and run a DHCP server:

```
$ cat udhcpd-bcm0.conf
start 192.168.9.8
end 192.168.9.255
interface bcm0
pidfile /var/run/udhcpd-bcm0.pid
lease_file /var/lib/misc/udhcpd-bcm0.leases
option subnet 255.255.255.0
option lease 864000 # default: 10 days

$ ifconfig bcm0 192.168.9.1
$ udhcpd -S udhcpd-bcm0.conf
```

Listing 12: 2.4 GHz AP IP configuration

Next, configure the station network interface to connect it to an AP:

```
wpa_cli> IFNAME=wlan0 disconnect
wpa_cli> IFNAME=wlan0 list_network
wpa_cli> IFNAME=wlan0 remove_network 0
wpa_cli> IFNAME=wlan0 add_network
wpa_cli> IFNAME=wlan0 set_network 0 ssid "testAP2"
wpa_cli> IFNAME=wlan0 set_network 0 key_mgmt NONE
wpa_cli> IFNAME=wlan0 save_config
wpa_cli> IFNAME=wlan0 enable_network 0
```

Listing 13: 2.4 GHz station without security

To configure the IP address through DHCP:

```
$ udhcpc -i wlan0
```

Listing 14: 2.4 GHz STA IP configuration

3.8.3 Country code selection

The country code for the operational region is selected with the `wl country` command. This enables the regulatory configuration from the CLM for the selected country. Type `wl country list [band(a or b)]` for the list of supported countries.

```
$ wl country DE
$ wl country
DE (DE/0) GERMANY
```

3.8.4 Bluetooth inquiry

To verify that Bluetooth is working, a Bluetooth inquiry can be issued to scan for remote devices. L2CAP echo requests can be used to ping the remote devices.

```
$ hcitool -i hci0 scan
Scanning ...
00:22:58:F8:86:BB ae-sho-bln-test
$ l2ping -i hci0 00:22:58:F8:86:BB
Ping: 00:22:58:F8:86:BB from 00:06:C6:46:DF:7B (data size 44) ...
4 bytes from 00:22:58:F8:86:BB id 0 time 69.75ms
4 bytes from 00:22:58:F8:86:BB id 1 time 56.76ms
[...]
```

3.9 Bluetooth vendor specific HCI commands

For the HCI vendor specific commands, the OGF is defined as 0x3F.

3.9.1 SCO/PCM interface configuration

The HCI command `Write_SCO_PCM_Int_Param` is used to configure the SCO routing and PCM interface parameters. SCO routing can be configured through the PCM or transport (UART) interface of JODY-W1 series modules. For I2S audio mode, SCO routing must be set to PCM with I2S_Enable=0x1. See also PCM/I2S audio interface configuration.

Command	OCF	Command parameters	Return parameters
Write_SCO_PCM_Int_Param	0x01C	SCO_Routing, PCM_Interface_Rate, Frame_Type, Sync_Mode, Clock_Mode	Status

Command parameters:

SCO_Routing	Specifies whether the SCO path is routed through PCM interface, I2S interface or transport interface.	Size: 1 Octet
Value	**Parameter description**	
0x00	PCM	
0x01	Transport	

PCM_Interface_Rate	Specifies the PCM clock frequency.	Size: 1 Octet
Value	**Parameter description**	
0x00	128 kbps	
0x01	256 kbps	
0x02	512 kbps	
0x03	1024 kbps	
0x04	2048 kbps	

Frame_Type	Specifies the PCM frame type; short frame or long frame.	Size: 1 Octet
Value	**Parameter description**	
0x00	Short	
0x01	Long	

Sync_Mode	Specifies whether the Bluetooth module is to be the master or slave for PCM_SYNC signal.	Size: 1 Octet
Value	**Parameter description**	
0x00	Slave	
0x01	Master	

Clock_Mode	Specifies whether the Bluetooth module is to be the master or slave for PCM_CLK signal.	Size: 1 Octet
Value	**Parameter description**	
0x00	Slave	
0x01	Master	

Return parameters:

Status	Error code as specified in Bluetooth Core Specification.	Size: 1 Octet
Value	**Parameter description**	
0x00	Command succeeded	
0x01-0xFF	Command failed	

3.9.2 PCM/I2S audio interface configuration

The PCM/I2S interface is configured with the `Write_I2SPCM_Interface_Param` HCI command. For I2S operation over the PCM interface of JODY-W1 series modules, you need to:

1. Configure SCO routing through PCM using the `Write_SCO_PCM_Int_Param` HCI command
2. Configure the operation mode of the PCM interface to I2S (set I2S_Enable parameter to 0x1)

Command	OCF	Command parameters	Return parameters
Write_I2SPCM_Interface_Param	0x06D	I2S_Enable, Is_Master, Sample_Rate, Clock_Rate	Status

Command parameters:

I2S_Enable	Enables or disables I2S mode for the PCM interface.	Size: 1 Octet
Value	**Parameter description**	
0x00	Disable	
0x01	Enable	

Is_Master	Select master or slave mode.	Size: 1 Octet
Value	**Parameter description**	
0x00	Slave	
0x01	Master	

Sample_Rate	Configures the sample rate.	Size: 1 Octet
Value	**Parameter description**	
0x00	8 kHz	
0x01	16 kHz	
0x02	4 kHz	

Clock_Rate	Configures the I2S interface clock rate.	Size: 1 Octet
Value	**Parameter description**	
0x00	128 kHz	
0x01	256 kHz	
0x02	512 kHz	
0x03	1024 kHz	
0x04	2048 kHz	

Return parameters:

Status	Error code as specified in Bluetooth Core Specification.	Size: 1 Octet
Value	**Parameter description**	
0x00	Command succeeded	
0x01-0xFF	Command failed	

3.9.3 PCM loopback mode

PCM loopback mode for testing is enabled with the HCI command `Write_PCM_Loopback_Mode`.

Command	OCF	Command parameters	Return parameters
Write_PCM_Loopback_Mode	0x024	PCM_Loopback_Mode	Status

Command parameters:

PCM_Loopback_Mode	Enables or disables PCM loopback mode.	Size: 1 Octet
Value	**Parameter description**	
0x00	Loopback off	
0x01	Loopback on	

Return parameters:

Status	Error code as specified in Bluetooth Core Specification.	Size: 1 Octet
Value	**Parameter description**	
0x00	Command succeeded	
0x01-0xFF	Command failed	

3.9.4 Set sleep mode parameters

Low power sleep mode with out-of-band control signals is configured with the `Set_Sleepmode_Param` HCI command. It uses the following out-of-band control signals on each side of the UART HCI transport to notify the other side about the availability of data.

- **BT_DEV_WAKE** (input on host controller)
  - Host asserts the line when it has data for the host controller
- **BT_HOST_WAKE** (output on host controller)
  - Host controller asserts the line when it has data for the host
  - Normally connected to an interrupt source on the host for wake-up

Each side of the HCI UART transport still utilizes the existing UART flow control line (RTS/CTS) to notify the other side whether it is ready to receive the data as shown in Table 27.

Signal (when asserted)	Host	Host controller (JODY-W1)
BT_DEV_WAKE	Host wants to transmit	N/A
BT_HOST_WAKE	N/A	Host controller wants to transmit
BT_UART_RTS	N/A	Host controller is ready to receive
BT_UART_CTS (HOST_UART_RTS)	Host is ready to receive	N/A

Table 27: Bluetooth sleep mode signals indication

The required host side implementations are listed below:

- Configure interrupt source to be triggered by **BT_HOST_WAKE**
- Activate low-power sleep mode on host controller by issuing `Set_Sleepmode_Param` command
- Assert **BT_DEV_WAKE** before transmitting any HCI packets
- Deassert **BT_DEV_WAKE** if no more packets are to be sent
- Before the host enters sleep mode, suspend UART and hold flow-off by keeping host's **UART_RTS** pin deasserted
- When woken up by the **BT_HOST_WAKE** signal, resume UART and assert host's **UART_RTS** pin to release flow-off

Command	OCF	Command parameters	Return parameters
Set_Sleepmode_Param	0x027	Sleep_Mode, Idle_Threshold_Host, Idle_Threshold_HostController, BT_DEV_WAKE_Active_Polarity, BT_HOST_WAKE_Active_Polarity, Allow_Host_Sleep_During_SCO, Combine_Sleep_Mode_And_LPM, Enable_Tristate_Control_Of_UART_Tx_Line, Reserved (3), Pulsed_HOST_WAKE	Status

Command parameters

Sleep_Mode	Sleep mode algorithm selection.	Size: 1 Octet
Value	**Parameter description**	
0x00	No sleep mode	
0x01	UART with out-of-band signals	

Idle_Threshold_Host	Number of firmware loops executed with no 'activity' before Host Controller deasserts BT_HOST_WAKE line. 'Activity' includes HCI traffic and the presence of SCO connection if Allow_Host_Sleep_During_SCO is not set.	Size: 1 Octet
Value	**Parameter description**	
0x00-0xFF	Number of firmware loops, each roughly equivalent to 12.5 ms	

Idle_Threshold_HostController	Number of firmware loops executed with no 'activity' before Host Controller considers itself as in idle. 'Activity' includes HCI traffic and the presence of ACL/SCO connections.	Size: 1 Octet
Value	**Parameter description**	
0x00-0xFF	Number of firmware loops, each roughly equivalent to 12.5 ms	

BT_DEV_WAKE_Active_Polarity	This flag indicates whether the BT_DEV_WAKE line is active low or high.	Size: 1 Octet
Value	**Parameter description**	
0x00	Active low	
0x01	Active high	

BT_HOST_WAKE_Active_Polarity	This flag indicates whether the BT_HOST_WAKE line is active low or high.	Size: 1 Octet
Value	**Parameter description**	
0x00	Active low	
0x01	Active high	

Allow_Host_Sleep_During_SCO		Size: 1 Octet
Value	**Parameter description**	
0x00	Host is not allowed to sleep while SCO/eSCO connection is active. Host Controller keeps BT_HOST_WAKE line asserted during active SCO/eSCO	
0x01	Otherwise	

Combine_Sleep_Mode_And_LPM		Size: 1 Octet
Value	**Parameter description**	
0x00	Host Controller is allowed to sleep during sniff/hold/park regardless of BT_DEV_WAKE line state	
0x01	Host Controller is allowed to sleep during sniff/hold/park if BT_DEV_WAKE line is deasserted	

Enable_Tristate_Control_Of_UART_Tx_Line		Size: 1 Octet
Value	**Parameter description**	
0x00	Host Controller will not tristate its UART TX line during sleep	
0x01	Otherwise	

Reserved		Size: 3 Octets
Value	**Parameter description**	
0x00-0xFF	N/A	

Pulsed_HOST_WAKE		Size: 1 Octet
Value	**Parameter description**	
0x01	After asserting BT_HOST_WAKE, if HOST does not wake up, deassert BT_HOST_WAKE and retry assertion	
0x00	Otherwise	

Return parameters:

Status	Error code as specified in Bluetooth Core Specification.	Size: 1 Octet
Value	**Parameter description**	
0x00	Command succeeded	
0x01-0xFF	Command failed	

3.9.5 Enable wide band speech

Wide band speech application is enabled or disabled with the `Enable_WBS` HCI command.

Command	OCF	Command parameters	Return parameters
Enable_WBS	0x07E	Enable_WBS, UUID_WBS	Status

Command parameters:

Enable_WBS	Enables or disable wide band speech.	Size: 1 Octet
Value	**Parameter description**	
0x00	Disable wide band speech	
0x01	Enable wide band speech	

UUID_WBS	Sets the eSCO packet type.	Size: 2 Octets
Value	**Parameter description**	
0x0002	2-EV3	

Return parameters:

Status	Error code as specified in Bluetooth Core Specification.	Size: 1 Octet
Value	**Parameter description**	
0x00	Command succeeded	
0x01-0xFF	Command failed	

4 Handling and soldering

JODY-W1 series modules are Electrostatic Sensitive Devices that demand the observance of precautions against electrostatic discharge. Failure to observe precautions can result in severe damage to the product. Standard ESD safety practices must be applied.

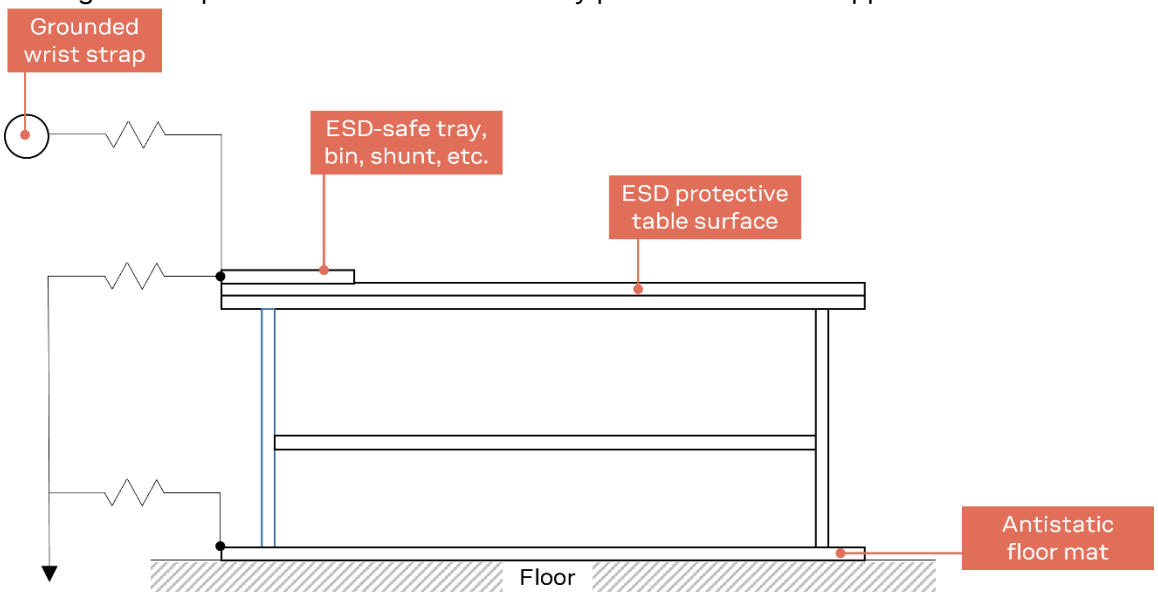

Figure 13: Standard workstation setup for safe handling of ESD-sensitive devices

4.1 Special ESD handling precautions

The risk of introducing electrostatic discharge in the RF transceiver through the RF pins is of special concern and the following bullets must carefully be observed:

- When connecting test equipment or any other electronics to the module (as a standalone or PCB-mounted device), the first point of contact must always be to local GND.
- Before mounting an antenna, connect the device to ground.
- When handling the RF pin, do not touch any charged capacitors. Be especially careful when handling materials like patch antennas (~10 pF), coaxial cables (~50-80 pF/m), soldering irons, or any other materials that can develop charges.
- To prevent electrostatic discharge through the RF input, do not touch any exposed antenna area. If there is any risk of the exposed antenna being touched in an unprotected ESD work area, be sure to implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the RF pin on the transceiver, be sure to use an ESD-safe soldering iron (tip).

4.2 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to reels, tapes, or trays, moisture sensitivity levels (MSL), storage, shipment, and drying preconditioning, see the JODY-W1 series modules data sheet [2] and Product packaging guide [1].

4.3 Reflow soldering process

JODY-W1 series modules are surface mount devices supplied in LGA package. The modules have a multi-layer FR4-type PCB with nickel/gold-plated solder pads and are produced in a lead-free process using lead-free soldering paste. The thickness of solder resist between the host PCB top side and the bottom side of JODY-W1 series modules must be considered for the soldering process.

JODY-W1 series modules are compatible with industrial reflow profile for RoHS solders, and "no-clean" soldering paste is strongly recommended.

Only a single-reflow soldering process is permitted for host boards that are integrated with JODY-W1 series modules.

☞ Although it is possible to manufacture host boards integrating JODY-W1 in two-reflow and mounted-upside-down reflow processes, these soldering practices are not recommended and are undertaken at the customer's own risk. For information about the testing results and recommendations concerning these reflow processes, see also information note [13] or contact your local u-blox technical support team.

The reflow profile used is dependent on the thermal mass of the entire populated PCB, the heat transfer efficiency of the oven, and the type of solder paste that is used. The optimal soldering profile must be trimmed for the specific process and PCB layout

⚠ The target values shown in Table 28 and Figure 14 are given as general guidelines for a Pb-free process only. For further information, see also the JEDEC J-STD-020E [6] standard.

Process parameter		Unit	Target
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_S (from 25°C)	s	150
	t_S (Pre-heat)	s	110
Peak	T_L	°C	217
	t_L (time above T_L)	s	90
	T_P (absolute max)	°C	260
	t_P (time above T_P -5°C)	s	30
Cooling	Ramp-down from T_L	K/s	6
General	$T_{to\ peak}$	s	300
	Allowed soldering cycles	-	1

Table 28: Recommended reflow profile

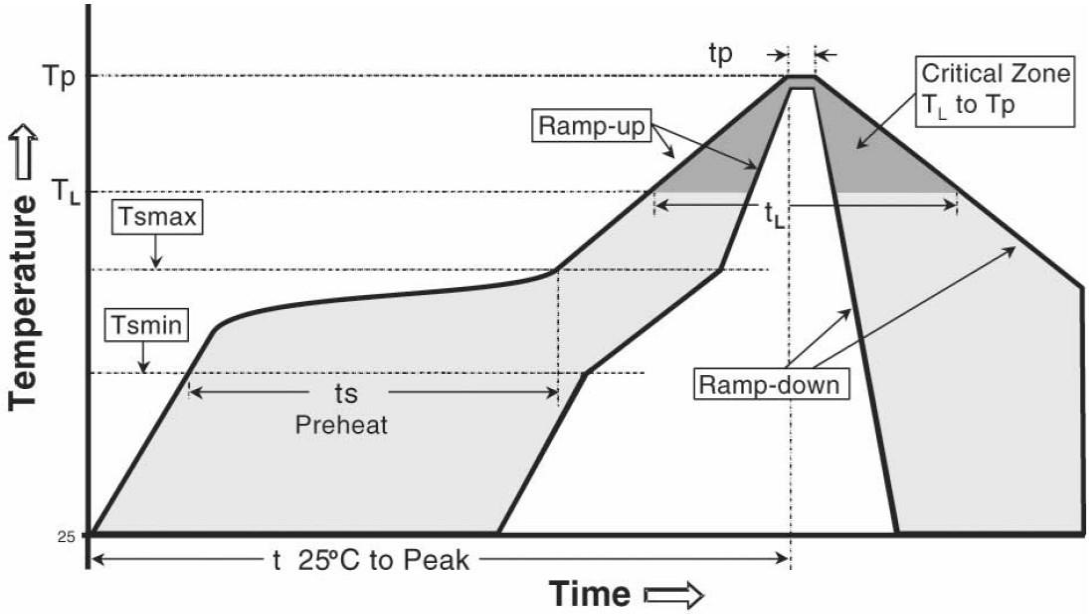

Figure 14: Reflow profile

☞ The lower value of T_P and slower ramp down rate is advised.

4.3.1 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pins. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housings that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module and the crystal oscillators in particular.

For best results use a "no clean" soldering paste and circumvent the need for a cleaning stage after the soldering process.

4.3.2 Other notes

- Only a single reflow soldering process is recommended for boards with a module populated on it.
- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices may require wave soldering to solder the THT components. Only a single wave soldering process is recommended for boards populated with the modules. Miniature Wave Selective Solder process is preferred over traditional wave soldering process.
- Hand soldering is not recommended.
- Rework is not recommended.
- Conformal coating can affect the performance of the module, which means that it is important to prevent the liquid from flowing into the module. The RF shields do not provide protection for the module from coating liquids with low viscosity; therefore, care is required while applying the coating. Conformal Coating of the module will void the warranty.

- Grounding metal covers: Attempts to improve grounding by soldering ground cables, wick, or other forms of metal strips directly onto the EMI covers is done at the customer's own risk and voids the module warranty. The numerous ground pins are adequate to provide optimal immunity to interferences.
- The modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding, etc.) may damage the module. Use of ultrasonic processes on an end product integrating this module will void the warranty.

5 Regulatory compliance

5.1 General requirements

The JODY-W1 series modules comply with the regulatory demands of Federal Communications Commission (FCC), Innovation, Science and Economic Development Canada (ISED)[14] and the CE mark. This section contains instructions on the process needed for an integrator when including the JODY-W1 series into an end-product.

- Any deviation from the process described may cause the JODY-W1 series module not to comply with the regulatory authorizations of the module and thus void the user's authority to operate the equipment.
- Any changes to hardware, hosts or co-location configuration may require new radiated emission and SAR evaluation and/or testing.
- The regulatory compliance of JODY-W1 series does not exempt the end-product from being evaluated against applicable regulatory demands; for example, FCC Part 15B criteria for unintentional radiators [8].
- The end-product manufacturer must follow all the engineering and operating guidelines as specified by the grantee (u-blox).
- The JODY-W1 series is for OEM integrators only.
- Only authorized antenna(s) may be used. See also the JODY-W1 series data sheet [2] for the list of authorized antennas. In the end-product, JODY-W1 must be installed in such a way that only authorized antennas can be used.
- The end-product must use the specified antenna trace reference design described in the JODY-W1 antenna reference design, application note [12].
- Any notification to the end user about how to install or remove the integrated radio module is NOT allowed.

⚠ If these conditions cannot be met or any of the operating instructions are violated, the u-blox regulatory authorization will be considered invalid. Under these circumstances, the integrator is responsible to re-evaluate the end-product including the JODY-W1 series module and obtain their own regulatory authorization, or u-blox may be able to support updates of the u-blox regulatory authorization. See also Antenna requirements.

5.2 FCC/ISED End-product regulatory compliance

u-blox represents that the modular transmitter fulfills the FCC/ISED regulations when operating in authorized modes on any host product given that the integrator follows the instructions as described in this document. Accordingly, the host product manufacturer acknowledges that all host products referring to the FCC ID or ISED certification number of the modular transmitter and placed on the market by the host product manufacturer need to fulfil all of the requirements mentioned below. Non-compliance with these requirements may result in revocation of the FCC approval and removal of the host products from the market. These requirements correspond to questions featured in the FCC guidance for software security requirements for U-NII devices, FCC OET KDB 594280 D02 [16].

⚠ The modular transmitter approval of JODY-W1, or any other radio module, does not exempt the end product from being evaluated against applicable regulatory demands.

[14] Formerly known as IC (Industry Canada).

The evaluation of the end product shall be performed with the JODY-W1 module installed and operating in a way that reflects the intended use case for the end product. The upper frequency measurement range of the end product evaluation is the 10th harmonic of 5.8 GHz, as described in KDB 996369 D04.

The following requirements apply to all products that integrate a radio module:

- Subpart B - UNINTENTIONAL RADIATORS
  To verify that the composite device of host and module comply with the requirements of FCC part 15B, the integrator shall perform sufficient measurements using ANSI 63.4-2014.
- Subpart C - INTENTIONAL RADIATORS
  To validate that the fundamental and out of band emissions of the transmitter part of the composite device complies with the requirements of FCC part 15C, it is required that the integrator carries out sufficient verification measurements using ANSI 63.10-2013.

When the above requirements are fulfilled the end product manufacturer can use the authorization procedures, shown in Table 1 of 47 CFR Part 15.101, before marketing the end product. This means that the customer has to market the end product under a *Suppliers Declaration of Conformity (SDoC)*. Alternatively, the product must be certified by accredited test lab.

The description of the FCC regulatory requirements in this document comprise a subset of applicable publications maintained by the FCC Office of Engineering and Technology (OET) Knowledge Database (KDB). We recommend that integrators read the following list of KDB reference documents:

- KDB 178919 D01 Permissive Change Policy
- KDB 447498 D01 General RF Exposure Guidance
- KDB 594280 D01 Configuration Control
- KDB 594280 D02 U-NII Device Security
- KDB 784748 D01 Labelling Part 15 18 Guidelines
- KDB 996369 D01 Module certification Guide
- KDB 996369 D02 Module Q&A
- KDB 996369 D04 Module Integration Guide

5.2.1 Referring to the u-blox FCC/ISED certification ID

If the conditions for General requirements, FCC/ISED End-product regulatory compliance, and all sub sections of the Antenna requirements are met, the u-blox modular FCC/ISED regulatory authorization is valid and the end-product may then refer to the u-blox FCC ID and ISED certification number. u-blox may be able to support updates to the u-blox regulatory authorization; for example, extending authorization to include new antennas. See also Antenna requirements.

⚠ To use the u-blox FCC / ISED grant and refer to the u-blox FCC ID / ISED certification ID, the integrator must confirm with u-blox that all requirements associated with the Configuration control and software security of end-products are fulfilled.

5.2.2 Obtaining own FCC/ISED certification ID

Integrators who do not want to refer to the u-blox FCC/ISED certification ID, or who do not fulfil all requirements to do so may instead obtain their own certification. With their own certification, the integrator has full control of the grant to make changes.

Integrators who want to base their own certification on the u-blox certification can do so via a process called “Change in ID” (FCC) / “Multiple listing” (ISED). With this, the integrator becomes the grantee of a copy of the u-blox FCC/ISED certification. U-blox will support with an approval letter that shall be filed as a Cover Letter exhibit with the application.

☞ For modules with the FCC ID / ISED certification ID printed on the label, the integrator must replace the module label with one that includes the new FCC/ISED ID. For a description of the labeling requirements, refer to the JODY-W1 series data sheet [2].

⚠ It is the responsibility of the integrator to comply with any upcoming regulatory requirements.

5.2.3 Antenna requirements

In addition to the general requirement to use only authorized antennas, the u-blox grant also requires a separation distance of at least 20 cm from the antenna(s) to all persons. The antenna(s) must not be co-located with any other antenna or transmitter (simultaneous transmission) as well. If this cannot be met, a Permissive Change as described below must be made to the grant.

☞ In order to support verification activities that may be required by certification laboratories, customers applying for Class-II Permissive changes must implement the setup described in Software and the JODY-W1 radio test guide, application note [11].

5.2.3.1 Separation distance

If the required separation distance of 20 cm cannot be fulfilled, a SAR evaluation must be performed. This consists of additional calculations and/or measurements. The result must be added to the grant file as a Class II Permissive Change.

5.2.3.2 Co-location (simultaneous transmission)

If the module is to be co-located with another transmitter, additional measurements for simultaneous transmission are required. The results must be added to the grant file as a Class II Permissive Change.

5.2.3.3 Adding a new antenna for authorization

If the authorized antennas and/or antenna trace design cannot be used, the new antenna and/or antenna trace designs must be added to the grant file. This is done by a Class I Permissive Change or a Class II Permissive Change, depending on the specific antenna and antenna trace design.

- Antennas of the same type and with less or same gain as an already approved antenna can be added under a Class I Permissive Change.
- Antenna trace designs deviating from the u-blox reference design and new antenna types are added under a Class II Permissive Change.
- For 5 GHz modules, the combined minimum gain of antenna trace and antenna must be greater than 0 dBi to comply with DFS testing requirements.

⚠ Integrators with the intention to refer to the u-blox FCC ID / ISED certification ID must contact their local u-blox support team to discuss the Permissive Change Process. Class II Permissive Changes will be subject to NRE costs.

5.2.4 Configuration control and software security of end-products

☞ Modular transmitter" hereafter refers to
JODY-W164-27A, JODY-W163-04A, JODY-W164-15A (FCC ID XPYJODYW164-07A),
JODY-W164-03A, JODY-W163-13A, JODY-W164-13A (FCC ID XPYJODYW164),
JODY-W167-00A, JODY-W167-03A (FCC ID XPYJODYW167),
JODY-W174-03A, JODY-W174-12A, JODY-W174-13A, JODY-W174-15A (FCC ID TBD.).

As the end-product must comply with the requirements addressed by the OET KDB 594280 [15], the host product integrating the JODY-W1 series must comply with the following requirements:

- Upon request from u-blox, the host product manufacturer will provide all of the necessary information and documentation to demonstrate how the requirements listed below are met.
- The host product manufacturer will not modify the modular transmitter hardware.
- The configuration of the modular transmitter when installed into the host product must be within the authorization of the modular transmitter at all times and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host product. The Wi-Fi Tx output power limits must be followed. In particular, the modular transmitter installed in the host product will not have the capability to operate on the operating channels/frequencies referred to in the section(s) below, namely one or several of the following channels: 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz). The channels 12 (2467 MHz), 13 (2472 MHz), 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz) are allowed to be used only for modules that are certified for the usage ("modular transmitter"). Customers must verify that the module in use is certified as supporting DFS client/master functionality.
- The host product uses only authorized firmware images provided by u-blox and/or by the manufacturer of the RF chipset used inside the modular transmitter.
- The configuration of the modular transmitter must always follow the requirements specified in Operating frequencies and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host product.
- The modular transmitter must when installed into the host product have a regional setting that is compliant with authorized US modes and the host product is protected from being modified by third parties to configure unauthorized modes of operation for the modular transmitter, including the country code.
- The host product into which the modular transmitter is installed does not provide any interface for the installer to enter configuration parameters into the end product that exceeds those authorized.
- The host product into which the modular transmitter is installed does not provide any interface to third parties to upload any unauthorized firmware images into the modular transmitter and prevents third parties from making unauthorized changes to all or parts of the modular transmitter device driver software and configuration.

☞ The OET KDB 594280 D01 [15] lists the topics that must be addressed to ensure that the end-product specific host meets the Configuration Control requirements.

☞ The OET KDB 594280 D02 [16] lists the topics that must be addressed to ensure that the end-product specific host meets the Software Security Requirements for U-NII Devices.

5.2.5 Operating frequencies

JODY-W1 802.11b/g/n operation outside the 2412–2462 MHz band is prohibited in the US and Canada and 802.11a/n/ac operation in the 5600–5650 MHz band is prohibited in Canada. Configuration of the module to operate on channels 12–13 and 120–128 must be prevented accordingly. The channels allowed while operating under the definition of a master or client device[15] are described in Table 29.

Channel number	Channel center frequency [MHz]	Master device	Client device	Remarks
1 – 11	2412 – 2462	Yes	Yes	
12 – 13	2467 – 2472	No	No	
36 – 48	5180 – 5240[16]	Yes	Yes	Canada (ISED): Devices are restricted to indoor operation only. The existing grant does not cover the usage in devices installed in vehicles.
52 – 64	5260 – 5320	No[17]	Yes	Canada (ISED): The existing grant does not cover the usage in devices installed in vehicles.
100 – 116	5500 – 5580	No[17]	Yes	
120 – 128	5600 – 5640	No	No	USA (FCC): Client device operation allowed under KDB 905462
132 – 140	5660 – 5700	No[17]	Yes	
149 – 165	5745 – 5825	Yes	Yes	

Table 29: Allowed channel usage under FCC/ISED regulation

☞ 15.407 (j) Operator Filing Requirement:
Before deploying an aggregate total of more than one thousand outdoor access points within the 5.15–5.25 GHz band, parties must submit a letter to the Commission acknowledging that, should harmful interference to licensed services in this band occur, they will be required to take corrective action. Corrective actions may include reducing power, turning off devices, changing frequency bands, and/or further reducing power radiated in the vertical direction. This material shall be submitted to Laboratory Division, Office of Engineering and Technology, Federal Communications Commission, 7435 Oakland Mills Road, Columbia, MD 21046. Attn: U-NII Coordination, or via Web site at https://www.fcc.gov/labhelp with the subject line: “U-NII-1 Filing”.

5.2.6 End product labeling requirements

For an end-product using the JODY-W1 series, there must be a label containing, at least, the following information:

This device contains
FCC ID: (XYZ)(UPN)
IC: (CN)-(UPN)

(XYZ) represents the FCC “Grantee Code”, this code may consist of Arabic numerals, capital letters, or other characters, the format for this code will be specified by the Commission’s Office of Engineering and Technology[18]. (CN) is the Company Number registered at ISED. (UPN) is the Unique Product Number decided by the grant owner.

[15] 47 CFR §15.202
[16] Under ISED regulations, operation in the band 5150–5250 MHz is for indoor use only and the end product must be labelled accordingly.
[17] JODY-W1 has not been certified to operate as DFS master.
[18] 47 CFR 2.926

The label must be affixed on an exterior surface of the end product such that it will be visible upon inspection in compliance with the modular labeling requirements of OET KDB 784748. The host user manual must also contain clear instructions on how end users can find and/or access the FCC ID of the end product.

The label on the JODY-W1 series module containing the original FCC ID acquired by u-blox can be replaced with a new label stating the end-product's FCC/ISED ID in compliance with the modular labeling requirements of OET KDB 784748.

FCC end product labeling

In accordance with 47 CFR § 15.19, the end product shall bear the following statement in a conspicuous location on the device:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: This device may not cause harmful interference, and This device must accept any interference received, including interference that may cause undesired operation.

ISED end product labeling

The end product shall bear the following statement in both English and French in a conspicuous location on the device:

Operation is subject to the following two conditions: this device may not cause interference, and this device must accept any interference, including interference that may cause undesired operation of the device.
Son utilisation est soumise aux deux conditions suivantes: Cet appareil ne doit pas causer d'interférences et il doit accepter toutes interférences reçues, y compris celles susceptibles d'avoir des effets indésirables sur son fonctionnement.

Labels of end products capable to operate within the band 5150–5250 MHz shall also include:

for indoor use only
Pour usage intérieur seulement

When the device is so small or for such use that it is not practicable to place the statements above on it, the information shall be placed in a prominent location in the instruction manual or pamphlet supplied to the user or, alternatively, shall be placed on the container in which the device is marketed. However, the FCC/ISED ID label must be displayed on the device as described above.

In case, where the final product will be installed in locations where the end-consumer is unable to see the FCC/ISED ID and/or this statement, the FCC/ISED ID and the statement shall also be included in the end-product manual.

5.2.7 Original FCC and ISED grant

The original grant and the FCC/ISED IDs of the JODY-W1 series module can be found in the JODY-W1 series data sheet [2].

5.3 CE end-product regulatory compliance

5.3.1 Safety standard

In order to fulfill the safety standard EN 60950-1 *[7]*, JODY-W1 series modules must be supplied with a Class-2 Limited Power Source.

5.3.2 CE Equipment classes

In accordance with Article 1 of Commission Decision 2000/299/EC[19], JODY-W1 series is defined as either Class-1 or Class-2 radio equipment, the end-product integrating JODY-W1 series inherits the equipment class of the module.

☞ Guidance on end product marking, according to the RED can be found at: http://ec.europa.eu/

☞ The restrictions for operating JODY-W1 series modules in Wi-Fi mode in European countries are described in the "European Union regulatory compliance" section of the data sheet [2].

⚠ The EIRP of the JODY-W1 module must not exceed the limits of the regulatory domain that the module operates in. Depending on the host platform's implementation and antenna gain, integrators have to limit the maximum output power of the module through the host software. Refer to the JODY-W1 series data sheet [2] for the module's approved antennas list and corresponding maximum transmit power levels.

5.4 Regulatory configuration

Regulatory configuration of JODY-W1 series modules is stored in a Country Local Map[20] (CLM) binary object (blob), which must be downloaded to the chipset during loading of the driver. See also Loading the Wi-Fi driver. The CLM defines the regulatory behavior for the set of supported countries. The definitions consist of:

- The set of valid channels
- The maximum output power for each data rate on each channel
- The type of the power limit (EIRP or conducted)
- DFS/TPC requirements (Radar sensitivity)

Each Infineon software release contains a reference CLM blob `4359b1.clm_blob` which can be used by customers for evaluation or initial development until the regulatory requirements for the end-product have been defined.

⚠ As the reference CLM blob does not take into account all the product specific regulatory requirements, it should not be used for production. Consequently, we recommend that you create your own product-specific CLM and integrate this into your application instead..

☞ On request, u-blox can provide CLM blobs with output power limits certified against JODY-W1 series modules, as described in Appendix A.

[19] 2000/299/EC: Commission Decision of 6 April 2000 establishing the initial classification of radio equipment and telecommunications terminal equipment and associated identifiers.
[20] Sometimes also called Country Locale Matrix

5.4.1 Overview of the regulatory CLM process

The overall regulatory approval process flow for end-products includes the following checkpoints:

1. Customer receives the MFG firmware for radio testing.
2. Customer creates the test plan and prepares the samples for regulatory testing. See also JODY-W1 radio test guide, application note [11].
3. Test lab takes measurements and records the maximum passing output powers.
4. Test lab creates a test report with passing output power and results.
5. Customer submits the list of countries and power tables to u-blox or Infineon.
6. Infineon creates the product specific CLM. This process typically takes around one week.
7. A new CLM will be released if changes to the power levels are needed or the country list is updated.

☞ For further information about the regulatory approval process with the JODY-W1 series modules, contact your local u-blox support team.

6 Product testing

6.1 u-blox in-line production testing

As part of our focus on high quality products, u-blox maintain stringent quality controls throughout the production process. This means that all units in our manufacturing facilities are fully tested and that any identified defects are carefully analyzed to improve future production quality.

The Automatic test equipment (ATE) deployed in u-blox production lines logs all production and measurement data – from which a detailed test report for each unit can be generated. Figure 15 shows the ATE typically used during u-blox production.

u-blox in-line production testing includes:

- Digital self-tests (firmware download, MAC address programming)
- Measurement of voltages and currents
- Functional tests (host interface communication)
- Digital I/O tests
- Measurement and calibration of RF characteristics in all supported bands, including RSSI calibration, frequency tuning of reference clock, calibration of transmitter power levels, etc.
- Verification of Wi-Fi and Bluetooth RF characteristics after calibration, like modulation accuracy, power levels, and spectrum, are checked to ensure that all characteristics are within tolerance when the calibration parameters are applied.

Figure 15: Automatic test equipment for module test

6.2 OEM manufacturer production test

As all u-blox products undergo thorough in-line production testing prior to delivery, OEM manufacturers do not need to repeat any firmware tests or measurements that might otherwise be necessary to confirm RF performance. Testing over analog and digital interfaces is also unnecessary during an OEM production test.

OEM manufacturer testing should ideally focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on the customer application board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

In addition to this testing, OEMs can also perform other dedicated tests to check the device. For example, the measurement of module current consumption in a specified operating state can identify a short circuit if the test result deviates that from that taken against a “Golden Device”.

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and perform basic RF performance testing.

Appendix

A Regulatory transmit output power limits

A.1 FCC/IC

Table 30 lists the maximum allowable conducted[21] output power limits for operation in the FCC/IC regulatory domains. The output power limits are applicable with an external antenna gain of 2 dBi.

Channel	Channel bandwidth	Data rates / modulation	Maximum power setting
1-11	20 MHz	802.11b	18 dBm
1, 11	20 MHz	802.11g/n	13 dBm
2-10	20 MHz	802.11g/n	15 dBm
36, 64	20 MHz	802.11a/n/ac	12 dBm
40-60, 104-136, 144	20 MHz	802.11a/n/ac	14 dBm
100, 140	20 MHz	802.11a/n/ac	11 dBm
149-165	20 MHz	802.11a/n/ac	17 dBm
38, 102	40 MHz	802.11n/ac	10 dBm
46, 54	40 MHz	802.11n/ac	13 dBm
62	40 MHz	802.11n/ac	12 dBm
110, 118, 126, 142	40 MHz	802.11n/ac	14 dBm
134	40 MHz	802.11n/ac	11 dBm
151, 159	40 MHz	802.11n/ac	17 dBm
42, 58	80 MHz	802.11ac	10 dBm
106, 122	80 MHz	802.11ac	9 dBm
138	80 MHz	802.11ac	12 dBm
155	80 MHz	802.11ac	15 dBm

Table 30: Wi-Fi output power table for FCC/IC

[21] Output power at the antenna connector, without antenna gain.

A.2 ETSI

Table 31 lists the maximum allowable conducted[21] output power limits for operation in the ETSI regulatory domain. The output power limits are applicable with an external antenna gain of 0 dBi.

Channel	Channel bandwidth	Data rates / modulation	Maximum power setting
1-13	20 MHz	802.11b/n	14 dBm
1-13	20 MHz	802.11g	15 dBm
36-64	20 MHz	802.11a	16 dBm
100-140	20 MHz	802.11a	14 dBm
36-64, 100-140	20 MHz	802.11n/ac	13 dBm
38-62, 102-138	40 MHz	802.11n/ac	14 dBm
42, 58, 106, 122	80 MHz	802.11ac	14 dBm
149-165	20 MHz	802.11a/n/ac	SISO: 12 dBm, MIMO: 9 dBm
151, 159	40 MHz	802.11n/ac	SISO: 12 dBm, MIMO: 9 dBm
155	80 MHz	802.11ac	SISO: 12 dBm, MIMO: 9 dBm

Table 31: Wi-Fi output power table for ETSI

B Glossary

Abbreviation	Definition
AEC	Automotive Electronics Council
AP	Access Point
API	Application Programming Interface
ATE	Automatic Test Equipment
BT	Bluetooth
CDM	Charged Device Model
CE	European Conformity
CTS	Clear to Send
DC	Direct Current
DDR	Double Data Rate
DFS	Dynamic Frequency Selection
DHCP	Dynamic Host Configuration Interface
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIRP	Equivalent Isotropic Radiated Power
ESD	Electro Static Discharge
FCC	Federal Communications Commission
GND	Ground
GPIO	General Purpose Input/Output
HBM	Human Body Model
HS	High Speed
HCI	Host Controller Interface
ISED	Innovation, Science and Economic Development Canada
I²C	Inter-Integrated Circuit
KDB	Knowledge Database
LAN	Local Area Network
LDO	Low Drop Out
LED	Light-Emitting Diode
LPO	Low Power Oscillator
LTE	Long Term Evolution
MAC	Medium Access Control
MMC	Multi Media Card
MWS	Mobile Wireless Standards
NRE	Non-recurring engineering
NSMD	Non Solder Mask Defined
OEM	Original equipment manufacturer
OET	Office of Engineering and Technology
OS	Operating System
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCM	Pulse-code modulation
PHY	Physical layer (of the OSI model)

Abbreviation	Definition
PMU	Power Management Unit
RF	Radio Frequency
RSDB	Real Simultaneous Dual Band
RST	Request to Send
SDIO	Secure Digital Input Output
SMD	Solder Mask Defined
SMPS	Switching Mode Power Supply
SMT	Surface-Mount Technology
SSID	Service Set Identifier
STA	Station
TBD	To be Decided
THT	Through-Hole Technology
UART	Universal Asynchronous Receiver-Transmitter
VCC	IC power-supply pin
VIO	Input offset voltage
VSDB	Virtual Simultaneous Dual Band
VSWR	Voltage Standing Wave Ratio
WFD	Wi-Fi Direct
WLAN	Wireless local area network
WPA	Wi-Fi Protected Access

Table 32: Explanation of the abbreviations and terms used

Related documents

[1] Product packaging guide, UBX-14001652
[2] JODY-W1 series data sheet, UBX-16013635
[3] IEC EN 61000-4-2 – Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
[4] ETSI EN 301 489-1 – Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
[5] IEC61340-5-1 – Protection of electronic devices from electrostatic phenomena – General requirements
[6] JEDEC J-STD-020E – Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices
[7] ETSI EN 60950-1:2006 – Information technology equipment – Safety – Part 1: General requirements
[8] FCC Regulatory Information, Title 47 – Telecommunication
[9] JESD51 – Overview of methodology for thermal testing of single semiconductor devices
[10] broadcom-bluetooth, https://code.google.com/archive/p/broadcom-bluetooth/source/default/source
[11] JODY-W1 radio test guide, application note, UBX-18022384
[12] JODY-W1 antenna reference design, application note, UBX-18017767
[13] JODY-W1 reflow mounted upside down, information note, UBX-18021974
[14] JODY-W1 Android integration, application note, UBX-19014806
[15] FCC guidance 594280 D01 Configuration Control v02 r01,
[16] FCC guidance 594280 D02 U-NII Device Security v01r03

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	22-July-2016	sbia	Initial release.
R02	3-Nov-2016	sbia, ishe, mzes, ddie, kgom	Added section 3. Removed USB support. Modified the block diagram for JODY-W165, key featuresand pin definition (Table 3). Changed configuration pin settings in section 1.4.4. Updated SDIO requirements in section 2.4.2.
R03	28-Feb-2017	sbia, mzes, kgom	Removed support for Professional grade and included information about JODY-W167 product variant (section 1). Added Bluetooth information in section 3. Modified Figure 3 (PCIe control pin assignment). Renamed some signals. Replaced Document status with Disclosure restriction on page 2.
R04	08-Sep-2017	shoe, ddie	Added information about JODY-W164-07A and updated the JODY-W164-A block diagram (Figure 1). Added information about tested kernel versions of the reference drivers (Section 3.2). Updated section 5.3.2 in regard of RED. Added Bluetooth trademark.
R05	27-Feb-2018	mzes, ddie	Removed the product variant – JODY-W165-A and modified the product status for most of the variants to Engineering Sample in the last table on page 2. Updated pin definition table (Table 3). Updated voltage supply requirements (Table 4). Updated footprint with area for future pins (Figure 10). Changed LPO to be mandatory. Added description for CLM file and firmware images in section 3. Added vendor specific HCI commands in section 3.9. Replaced references to IC by ISED.
R06	6-Mar-2018	mhei, kgom	Updated section 1.1 and the following figures: Pin assignment (top view) (Figure 3), Recommended footprint (Figure 10), Stencil opening example for inner thermal pads (Figure 11)
R07	11-Apr-2018	mzes, kgom	In Bluetooth vendor specific HCI commands: Updated the information in section 3.9.1. Added information about PCM/I2S audio interface configuration (section 3.9.2) and PCM loopback mode (section 3.9.3)
R08	2-Jul-2018	mzes	Updated document to reflect changes in the product portfolio for PCIe-only and SDIO-only host interface variants. Updated host interface configuration in section 1.4.4. Provided reference to the Antenna reference design document.
R09	27-Sep-2018	mzes, mhei	Changed the type of WL_DEV_WAKE (Input) and WL_HOST_WAKE (Output) pins in Table 3. Updated Figure 6 and Figure 9. Added information about regulatory power limits in Annex A.
R10	14-Dec-2018	mzes	Updated the product status for JODY-W163-A and JODY-W164-A to Initial Production. Updated description for WL_HOST_WAKE wakeup (section 1.4.3), antenna isolation requirements (Table 18) and FCC/IC power levels (Table 30). Modified the second footnote description in section 5.2.6.
R11	20-Mar-2019	lber	Added I/O pin states for Active and Power Down mode in Table 3. Added information about layout considerations to reduce spurious emissions (section 2.5.4).
R12	12-Apr-2019	lber	Included information that LPO clock is mandatory in section 1.5.6.
R13	13-May-2019	mzes, kgom	Added two new product variants – JODY-W164-13A and JODY-W164-15A.
R14	10-Jul-2019	mzes	Updated the product status for JODY-W163-13A, JODY-W164-13A, JODY-W164-15A and JODY-W167 to Initial Production. Added Enable_WBS command in section 3.9.5.
R15		lber, mzes, fkru	Added Figure 7 as example of U.FL connector layout in section 2.2.2.1. Added MCIMX8M-EVK Android 8 platform to table 26 in section 3.2. Updated section 5.2 FCC/ISED End-product regulatory compliance. Updated product status to Mass Production for JODY-W164-03A-01. Removed the product variant JODY-W167-00B.
R16	23-Apr-2020	mzes	Replaced product variant JODY-W164-07A with JODY-W164-27A. Updated allowed channel usage for FCC/ISED in Table 29. Added section 5.4 Regulatory configuration.

Revision	Date	Name	Comments
R17	28-May-2021	mzes	Updated product status described in document information. Removed references to JODY-W163-05A, JODY-W164-04A, and JODY-W164-05A product variants as these have now reached End of Life. Updated FMAC driver link in Available software packages .Revised the description of LTE Coexistence UART. Updated allowed channel usage for FCC/ISED in Table 29. Added a note about firmware versions in Firmware images.
R18	23-Aug-2022	mzes	Added JODY-W174-A product variants. Removed Wi-Fi and Bluetooth features previously duplicated in the data sheet. Updated Configuration control and software security of end-products. Revised Handling and soldering and Product testing information and included other minor editorial changes throughout the document. Updated disclaimer and contact information. Removed previously duplicated information in the data sheet describing Maximum ESD ratings.
R19	27-Feb-2023	frca	Added two new JODY-W174-A product variants (-W174-12A and -W174-15A) in Document information and Configuration control and software security of end-products. Updated RF transmission line design. Added Other interfaces and notes for data communication interfaces.

Contact

For further support and contact information, visit us at www.u-blox.com/support.